REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline letter U. Add vendor CAGE number 60395 to drawing. Editorial changes throughout.	89-08-07	M. A. Frye
B	Add device type 28 to drawing. Editorial changes throughout.	93-01-05	M. A. Frye
C	Add software data protect to drawing. Updated boilerplate.	97-04-06	Raymond Monnin
D	Changes in accordance with NOR 5962-R409-97	97-08-12	Raymond Monnin
E	Editorial correction to page 1, correction of number of pages. Figure 1 redrawn with 32 leads vs 44 leads and dimension table corrected. ksr	04-06-04	Raymond Monnin
F	Add vendor CAGE numbers 0C7V7 and 3DTT2 to drawing. Updated boilerplate as part of 5-year review. - glg	10-03-25	Charles Saffle

THE ORIGINAL FIRST PAGE OF THE DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	F	F	F	F	F	F	F	F	F											
SHEET	15	16	17	18	19	20	21	22	23											

REV STATUS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Kenneth Rice

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-07-01

REVISION LEVEL
F

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 8K X 8-BIT EEPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87514**

SHEET
1 OF 23

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-87514	01	X	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish per MIL-PRF-38535 appendix A

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time	Write speed	Write mode	End of write indicator	Endurance
01	(see 6.4)	(8K X 8 EEPROM)	350 ns	10 ms	byte/page	DATA polling	10,000 cycles
02			300 ns	10 ms	byte/page	DATA polling	10,000 cycles
03			250 ns	10 ms	byte/page	DATA polling	10,000 cycles
04			200 ns	10 ms	byte/page	DATA polling	10,000 cycles
05			250 ns	10 ms	byte/page	DATA polling	100,000 cycles
06			350 ns	2 ms	byte/page	DATA polling	10,000 cycles
07			300 ns	2 ms	byte/page	DATA polling	10,000 cycles
08			250 ns	2 ms	byte/page	DATA polling	10,000 cycles
09			200 ns	2 ms	byte/page	DATA polling	10,000 cycles
10			120 ns	2 ms	byte/page	DATA polling	10,000 cycles
11			90 ns	2 ms	byte/page	DATA polling	10,000 cycles
12			70 ns	2 ms	byte/page	DATA polling	10,000 cycles
13			350 ns	1 ms	byte	RDY/BUSY	10,000 cycles
14			300 ns	1 ms	byte	RDY/BUSY	10,000 cycles
15			250 ns	1 ms	byte	RDY/BUSY	10,000 cycles
16			200 ns	1 ms	byte	RDY/BUSY	10,000 cycles
17			150 ns	1 ms	byte	RDY/BUSY	10,000 cycles
18			350 ns	1 ms	byte	DATA polling	10,000 cycles
19			300 ns	1 ms	byte	DATA polling	10,000 cycles
20			250 ns	1 ms	byte	DATA polling	10,000 cycles
21			200 ns	1 ms	byte	DATA polling	10,000 cycles
22			150 ns	1 ms	byte	DATA polling	10,000 cycles
23			350 ns	10 ms	byte/page	RDY/BUSY	10,000 cycles
24			300 ns	10 ms	byte/page	RDY/BUSY	10,000 cycles
25			250 ns	10 ms	byte/page	RDY/BUSY	10,000 cycles
26			200 ns	10 ms	byte/page	RDY/BUSY	10,000 cycles
27			250 ns	10 ms	byte/page	RDY/BUSY	100,000 cycles
28			200 ns	200 µs	byte	RDY/BUSY	10,000 cycles

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	See figure 1	32	"J" leaded cerquad package
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Y	CQCC1-N32	32	Rectangular leadless chip carrier
Z	CDFP4-F28	28	Flat pack

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V dc to +6.25 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J) 2/	+175°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Input voltage range (V_{IL}, V_{IH})	-0.3 V dc to +6.25 V dc
Data retention	10 years (minimum)
Endurance:	
Device types 01 through 04, 06 through 26, and 28	10,000 cycles/byte (minimum)
Device types 05 and 27	100,000 cycles/byte (minimum)
Chip clear voltage (V_H)	13.0 V dc

1.4 Recommended operating conditions. 1/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input voltage, low range (V_{IL})	-0.1 V dc to +0.8 V dc
Input voltage, high range (V_{IH})	+2.0 V dc to V_{CC} +0.3 V dc
Chip clear voltage range (V_H)	12 V dc to 13 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ All voltages are referenced to V_{SS} (ground).
2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table for unprogrammed devices. The truth table for unprogrammed devices shall be as specified on figure 3.

3.2.3.1 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. Defense Supply Center Columbus, (DSCC), DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EEPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EEPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.1. Devices shall be shipped in the erased (logic "1's) and verified state unless otherwise specified.

3.10.2 Programmability of EEPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.4.

3.10.3 Verification of erasure or programmability of EEPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of reading the device in accordance with the procedures and characteristics specified in 4.4.2. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.12 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.13 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change, which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Devices shall be burned-in containing a checkerboard pattern or equivalent.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures, and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the truth table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ V_{SS} = 0 V 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current (active)	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH} All I/O's = open Inputs = V_{CC} = 5.5 V	1,2,3	01-05, 23-27		60	mA
				06-12		80	
				13-22,28		45	
Supply current (TTL standby)	I_{CC1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = open Inputs = X	1,2,3	All		3	mA
Supply current (CMOS standby)	I_{CC2}	$\overline{CE}$ = V_{CC} -0.3 V All I/O's = open Inputs = V_{IL} to V_{CC} -0.3 V	1,2,3	01-12, 23-27		250	µA
				13-22,28		150	
Input leakage (high)	I_{IH}	V_{IN} = 5.5 V	1,2,3	All	-10	10	µA
Input leakage (low)	I_{IL}	V_{IN} = 0.1 V	1,2,3	All	-10	10	µA
Output leakage 3/ (high)	I_{OHZ}	V_{OUT} = 5.5 V, $\overline{CE}$ = V_{IH}	1,2,3	All	-10	10	µA
Output leakage 3/ (low)	I_{OLZ}	V_{OUT} = 0.1 V, $\overline{CE}$ = V_{IH}	1,2,3	All	-10	10	µA
Input voltage low	V_{IL}		1,2,3	All	-0.1	0.8	V
Input voltage high	V_{IH}		1,2,3	All	2.0	V_{CC}+0.3	V
Output voltage low	V_{OL}	I_{OL} = 2.1 mA, V_{IH} = 2.0 V V_{CC} = 4.5 V, V_{IL} = 0.8 V	1,2,3	All		0.45	V
Output voltage high	V_{OH}	I_{OH} = -400 µA, V_{IH} = 2.0 V V_{CC} = 4.5 V, V_{IL} = 0.8 V	1,2,3	All	2.4		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance 4/ 5/	C_I	$V_I = 0$ V, $V_{CC} = 5.0$ V $T_A = +25°C$, f = 1 MHz See 4.3.1c	4	All		10	pF
Output capacitance 4/ 5/	C_O	$V_O = 0$ V, $V_{CC} = 5.0$ V $T_A = +25°C$, f = 1 MHz See 4.3.1c	4	All		10	pF
Functional tests		See 4.3.1d	7,8A,8B	All			
Read cycle time 6/	t_{AVAV}	See figure 4	9,10,11	01,06,13,18,23	350		ns
				02,07,14,19,24	300		
				03,05,08,15,20,25,27	250		
				04,09,16,21,26,28	200		
				17,22,	150		
				10	120		
				11	90		
				12	70		
Address access time	t_{AVQV}		9,10,11	01,06,13,18,23		350	ns
				02,07,14,19,24		300	
				03,05,08,15,20,25,27		250	
				04,09,16,21,26,28		200	
				17,22		150	
				10		120	
				11		90	
				12		70	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ V_{SS} = 0 V 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip enable access time	t_{ELQV}	See figure 4	9,10,11	01,06,13, 18,23		350	ns
				02,07,14, 19,24		300	
				03,05,08, 15,20,25, 27		250	
				04,09,16, 21,26,28		200	
				17,22		150	
				10		120	
				11		90	
				12		70	
Output enable access time	t_{OLQV}		9,10,11	01-05, 13-22, 23-28		100	ns
				06-12,		50	
Chip enable to 5/ output in low Z	t_{ELQX}		9,10,11	All	10		ns
Chip disable to 5/ output in high Z	t_{EHQZ}		9,10,11	01-08, 13-15, 18-20, 23-27		80	ns
				09-12,16, 17,21,22, 28		55	
Output enable to 5/ output in low Z	t_{OLQX}		9,10,11	All	10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0\ V$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output disable to output in high Z	t_{OHQZ} 5/	See figure 4	9,10,11	01-08, 13-15, 18-20, 23-27		80	ns
				09-12,16, 17,21,22, 28		55	
Output hold from 6/ address change	t_{AVQX}		9,10,11	All	0		ns
$\overline{CE}$ to power up 5/	t_{pu}		9,10,11	All		250	ns
$\overline{CE}$ to power down 5/	t_{pd}		9,10,11	All		50	ns
Write cycle time	t_{WHWL1} t_{EHEL1}	See figures 5 and 6	9,10,11	01-05, 23-27		10	ms
				06-12		2.0	
				13-22		1.0	
				28		0.2	
Address setup 6/ time	t_{AVEL} t_{AVWL}	See figures 5, 6, and 7	9,10,11	All	20		ns
Address hold 6/ time	t_{ELAX} t_{WLAX}		9,10,11	All	150		ns
Write setup time 6/	t_{WLEL} t_{ELWL}		9,10,11	All	0		ns
Write hold time 6/	t_{WHEH}		9,10,11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{OE}$ setup time 6/	t_{OHEL} t_{OHWL}	See figures 5, 6, or 7 as applicable	9,10,11	All	20		ns
$\overline{OE}$ hold time	t_{WHOL}		9,10,11	All	20		ns
$\overline{WE}$ pulse width 6/	t_{ELEH} t_{WLWH}		9,10,11	All	150		ns
Data setup time 6/	t_{DVEH} t_{DVWH}		9,10,11	All	50		ns
Data hold time 6/	t_{EHDX} t_{WHDX}		9,10,11	All	10		ns
Byte load cycle	t_{EHEL2} t_{WHWL2}	See figures 5 or 6	9,10,11	All	0.2	2	µs
Last byte loaded 6/ to data polling	t_{WHEL}	See figure 5	9,10,11	06-12, 18-22		200	ns
$\overline{CE}$ setup time 6/	t_{ELWL}	See figure 5	9,10,11	All	1		µs
Output setup 6/ time	t_{OVHWL}	See figure 8	9,10,11	All	1		µs
$\overline{CE}$ hold time 6/	t_{EHWH}	See figure 6	9,10,11	All	1		µs
$\overline{OE}$ hold time 6/	t_{WHOH}	See figure 8, configuration A or B	9,10,11	All	1		µs
Erase time 6/	t_{OHAV}		9,10,11	01-05, 23-27	200		ms

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip erase time 6/	t_{WLWH2} 6/	See figure 8, configuration A or B	9,10,11	01-05, 23-27	150		ns
				06-22,28	10		ms
High voltage 6/	V_H		9,10,11	All	12	13	V
Time to device busy	t_{EHRL}	See figures 6 and 7	9,10,11	13-17,28		50	ns
	t_{WHRL}			23-27		100	
Write cycle time RDY/BUSY	t_{ELRH}		9,10,11	13-17,28		1	ms
	t_{WLRH}			23-27		10	
Maximum time to 6/ valid data after WE/CE low	t_{WLDV}		9,10,11	13-22,28		1	µs
	t_{ELDV}						

1/ DC and read mode.
2/ Equivalent ac test conditions:

Device types: 01 through 09 and 13 through 28.	Device types: 10 through 12.
Output load: 1 TTL gate and C1 = 100 pF,	Output load: 1 TTL gate and C1 = 30 pF.
Input rise and fall times $\le$ 10 ns.	Input rise and fall times $\le$ 5 ns.
Input pulse levels: 0.4 V and 2.4 V.	Input pulse levels: 0.4 V and 2.4 V.
Timing measurements reference levels:	
Inputs 1 V and 2 V.	Inputs 1 V and 2 V.
Outputs 0.8 V and 2 V.	Outputs 0.8 V and 2 V.

3/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{OLZ} and I_{OHZ} with the output under test connected to V_{OUT}.
4/ All pins not being tested are to be open.
5/ Tested initially and after any design or process changes that affect that parameter, and therefore guaranteed to the limits specified in table I.
6/ Tested by application of specified timing signals and conditions, see footnote 2/.

Case U

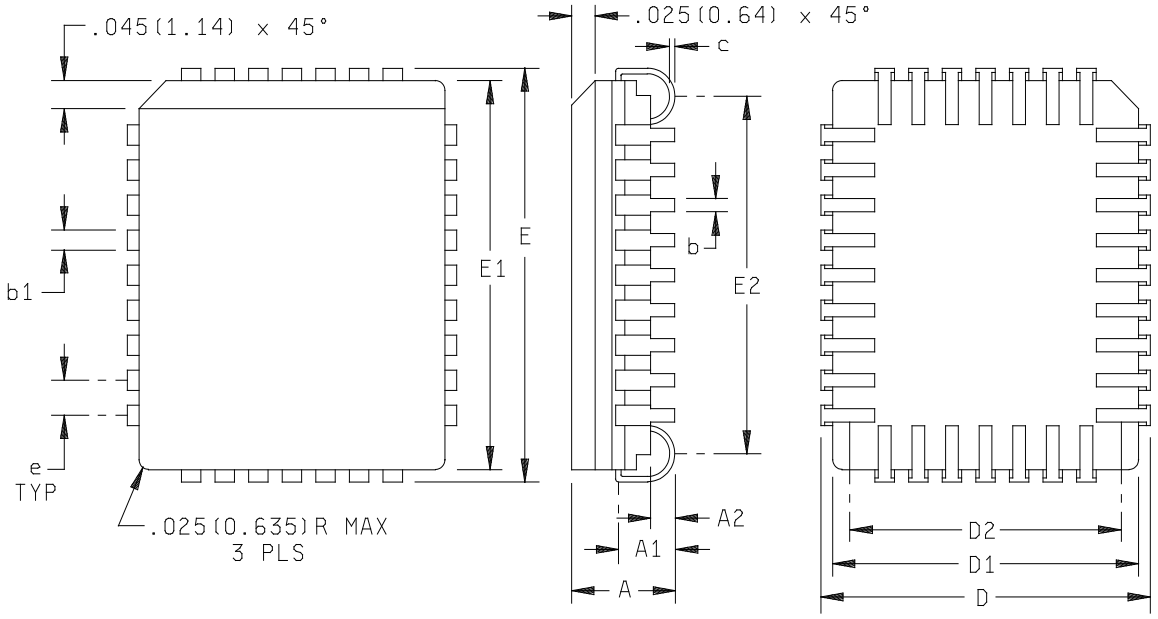


FIGURE 1. Case outline.

Case U

Dimensions				
Ltr	Inches		Millimeters	
	Min	Max	Min	Max
A	.140	.167	3.56	4.24
A_1	.073	.103	1.85	2.62
A_2	.027	.045	0.69	1.14
c	.006	.010	0.15	0.25
D	.485	.495	12.32	12.57
D_1	.445	.465	11.30	11.81
D_2	.390	.430	9.91	10.92
E	.585	.595	14.86	15.11
E_1	.545	.565	13.84	14.35
E_2	.490	.530	12.45	13.46
e	.050 TYP		1.27 TYP	
b	.017	.021	0.43	0.53
b_1	.026	.032	0.66	0.81
N	32			

NOTES:
1. Controlling dimensions are inches, metric provided for convenience.
2. Dimensions D_1 and E_1 do not include glass protrusion. Glass protrusion to be .010 inch (0.25 mm) maximum.
3. All dimensions and tolerances include lead trim offset and lead finish.

FIGURE 1. Case outline - Continued.

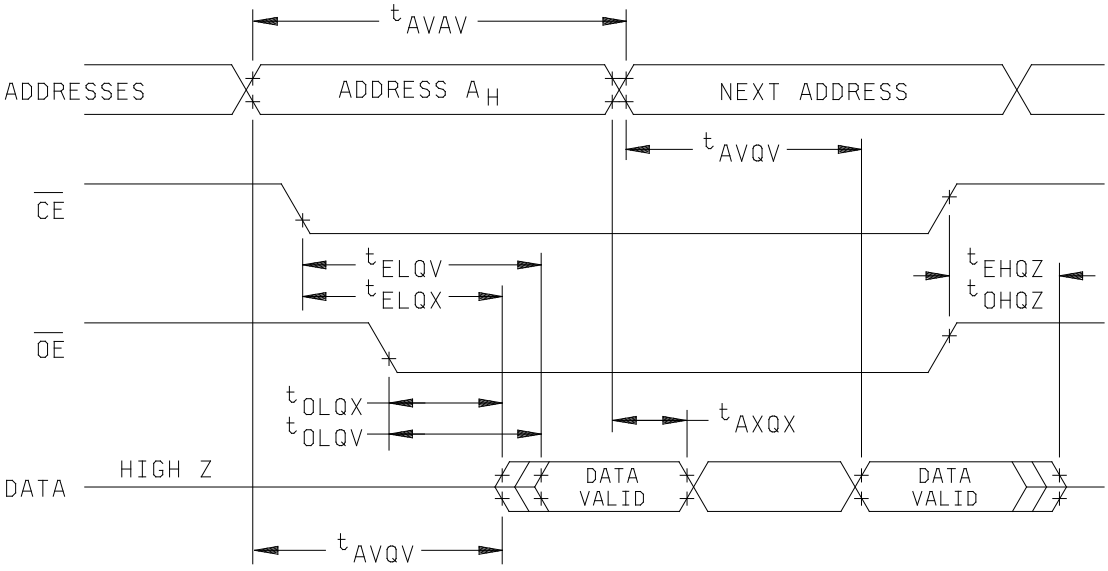
Device types	01 through 28	
Case outlines	X and Z	U and Y
Terminal number	Terminal symbol	
1	NC (See note)	NC
2	A_{12}	NC (See note)
3	A_7	A_{12}
4	A_6	A_7
5	A_5	A_6
6	A_4	A_5
7	A_3	A_4
8	A_2	A_3
9	A_1	A_2
10	A_0	A_1
11	I/O_0	A_0
12	I/O_1	NC
13	I/O_2	I/O_0
14	GND	I/O_1
15	I/O_3	I/O_2
16	I/O_4	GND
17	I/O_5	NC
18	I/O_6	I/O_3
19	I/O_7	I/O_4
20	$\overline{CE}$	I/O_5
21	A_{10}	I/O_6
22	$\overline{OE}$	I/O_7
23	A_{11}	$\overline{CE}$
24	A_9	A_{10}
25	A_8	$\overline{OE}$
26	NC	NC
27	$\overline{WE}$	A_{11}
28	V_{CC}	A_9
29	---	A_8
30	---	NC
31	---	$\overline{WE}$
32	---	V_{CC}

NOTE: For device types 13 through 17 and 23 through 28, this NC is replaced by RDY/$\overline{BUSY}$.

FIGURE 2. Terminal connections.

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Device types
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	All
Chip clear	V_{IL}	V_H	V_{IL}	X	All
Byte write	V_{IL}	V_{IH}	V_{IL}	Data in	All
Write inhibit	X	V_{IL}	X	High Z/D_{OUT}	All
Write inhibit	X	X	V_{IH}	High Z/D_{OUT}	All
Standby	V_{IH}	X	X	High Z	All

FIGURE 3. Truth table.

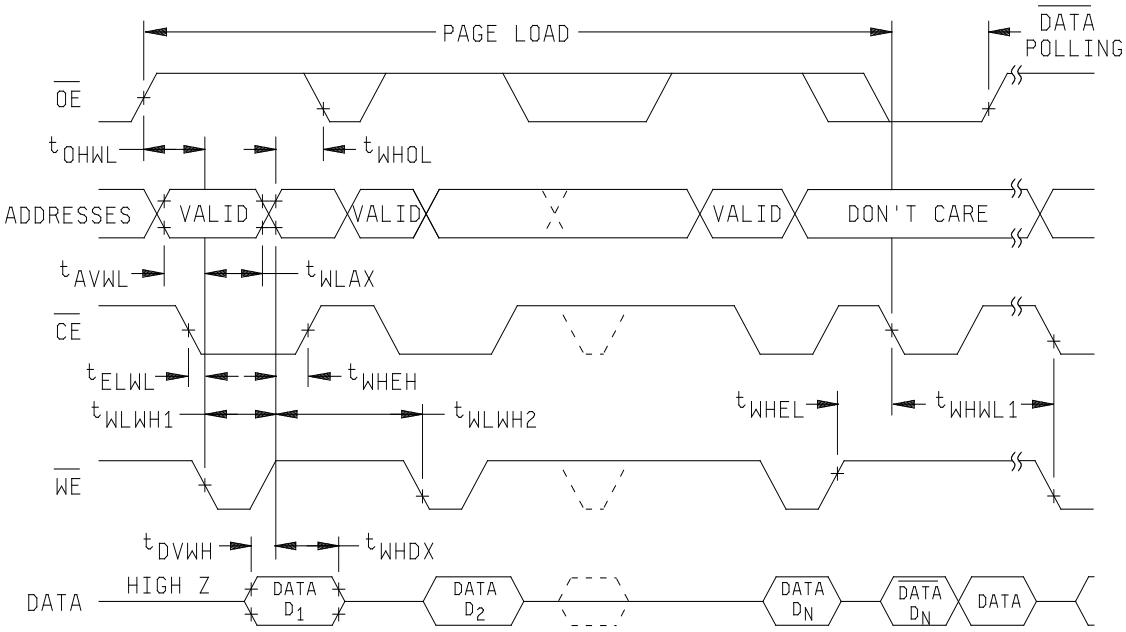


NOTES:

1. V_{CC} shall be applied simultaneously or after $\overline{WE}$ and removed simultaneously or before $\overline{WE}$.
2. See footnote 2 of table I.

FIGURE 4. Read cycle timing.

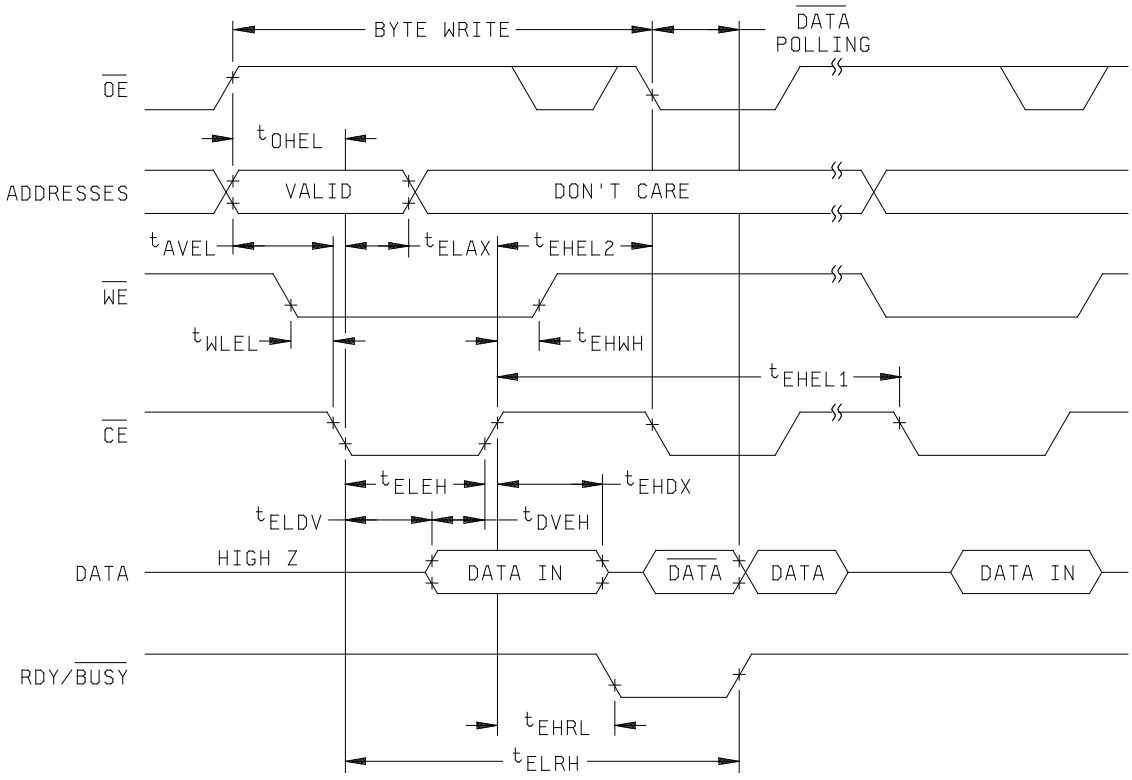
DEVICE TYPES 01 THRU 12 AND 23 THRU 27



NOTES:

1. See footnote 2 of table I.
2. Program verify equivalent to the read mode.
3. Page load is 1 to 64 bytes of data for device types 01 through 12, and 23 through 27.
4. $\overline{WE}$ is noise protected. Less than 20 ns write pulse will not activate a write cycle.
5. $\overline{WE}$ and $\overline{CE}$ both must be active to initiate a write cycle; therefore, the sequence of $\overline{WE}$ or $\overline{CE}$ (e.g., for $\overline{WE}$ or $\overline{CE}$ controlled write) is verified interchangeable without duplicate testing.

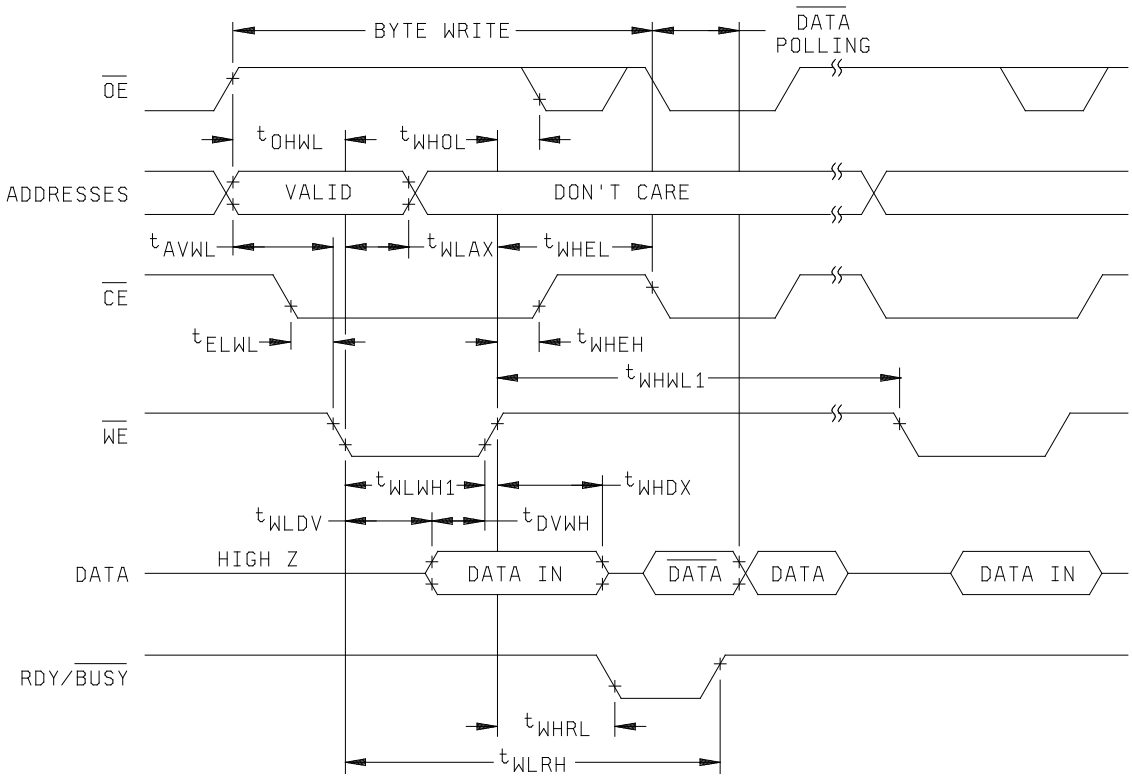
FIGURE 5. Page write programming waveforms.



NOTES:

1. See footnote 2 of table I.
2. Program verify equivalent to the read mode.
3. $\overline{WE}$ and $\overline{CE}$ both must be active to initiate a write cycle; therefore, the sequence of $\overline{WE}$ and $\overline{CE}$ (e.g., for $\overline{WE}$ or $\overline{CE}$ controlled write) is verified interchangeable without duplicate testing.

FIGURE 6. $\overline{CE}$ controlled byte write programming waveforms.

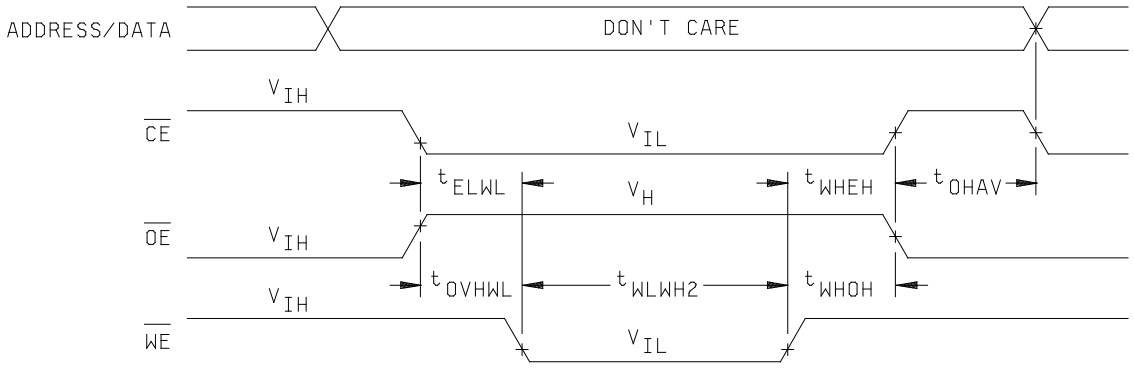


NOTES:

1. See footnote 2 of table I.
2. Program verify equivalent to the read mode.
3. $\overline{WE}$ and $\overline{CE}$ both must be active to initiate a write cycle; therefore, the sequence of $\overline{WE}$ and $\overline{CE}$ (e.g., for $\overline{WE}$ or $\overline{CE}$ controlled write) is verified interchangeable without duplicate testing.

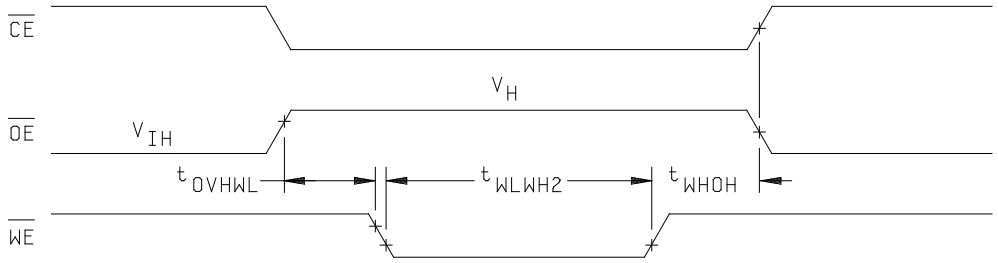
FIGURE 7. $\overline{WE}$ controlled byte write programming waveforms.

DEVICE TYPES 01 THRU 05 AND 23 THRU 27



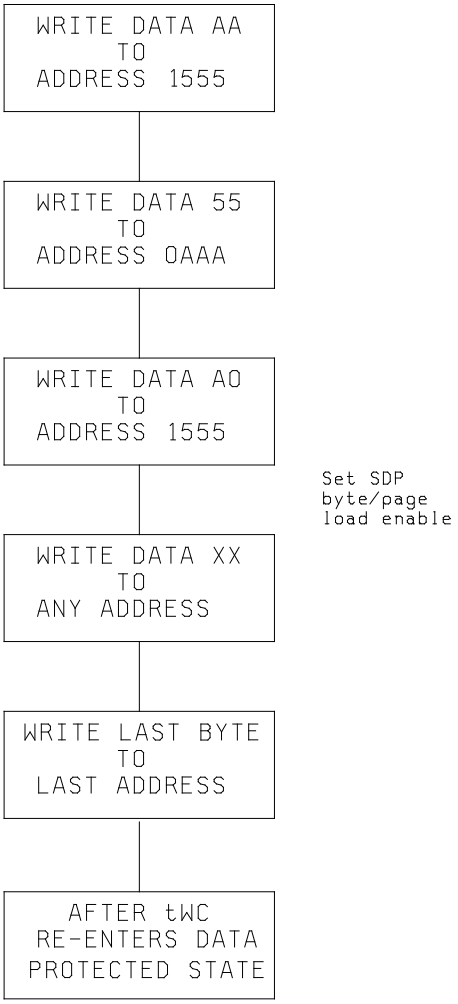
CONFIGURATION A

DEVICE TYPES 06 THRU 22 AND 28



CONFIGURATION B

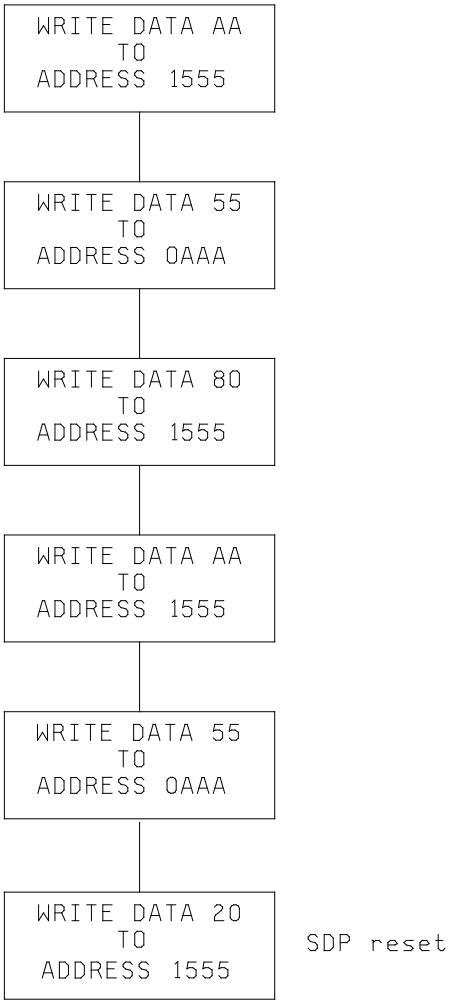
FIGURE 8. Chip clear waveforms.



NOTES:

1. Set software data protection timings are referenced to $\overline{WE}$ or $\overline{CE}$ inputs, whichever is last to go low, and the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is first to go high.
2. The command sequence must conform to the page write timing.
3. The command sequence and subsequent data must conform to the page write timing.

FIGURE 9. Set software data protect and software protected write algorithm (device types 01- 05 and 08 - 12).



NOTES:

1. Reset software data protection timings are referenced to $\overline{WE}$ or $\overline{CE}$ inputs, whichever is last to go low, and the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is first to go high.
2. The command sequence must conform to the page write timing.

FIGURE 10. Reset software data protect algorithm (device types 01- 05 and 08 - 12).

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups 1/ 2/ (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1, 7, 9, or 2, 8A, 10
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11 3/
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11 4/ 5/
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8, 9, 10, 11

1/ Any or all subgroups may be combined when using multifunction testers.
2/ For all electrical tests, the device shall be programmed to the data pattern specified.
3/ (*) Indicates PDA applies to subgroups 1 and 7.
4/ Subgroups 7 and 8 shall consist of writing and reading the data pattern specified in accordance with the limits of table I subgroups 9, 10, and 11.
5/ (**) Indicates that subgroup 4 will only be performed during initial qualification and after design or process changes (see 4.3.1c).

4.3.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. The following additional criteria shall apply.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4 Programming procedure. The following procedure shall be followed when programming (Write) is performed. The waveforms and timing relationships shown on figure 5 (per appropriate device type) and the conditions specified in table I shall be adhered to. Information is introduced by selectively programming a TTL low or TTL high on each I/O of the address desired. Functionality shall be verified at all temperatures (group A, subgroups 7 and 8) by programming all bytes of each device and verifying the pattern used.

4.4.1 Erasing procedure. There are two forms of erasure, chip and byte, whereby all bits or the address selected will be erased to a TTL high.

a. Chip erase is performed in accordance with the waveforms and timing relationships shown on figure 8 (in accordance with appropriate device type) and the conditions specified in table I.

b. Byte erase is performed in accordance with the waveforms and timing relationships shown on figure 5 (in accordance with appropriate device type) and the conditions specified in table I.

4.4.2 Read mode operation. The waveforms and timing relationships shown on figure 4 and the conditions specified in table I shall be applied when reading the device. Pattern verification utilizes the read mode.

4.4.3 RDY/$\overline{\text{BUSY}}$. While the write operation is in progress, the RDY/$\overline{\text{BUSY}}$ output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the RDY/BUSY pin to a TTL high. The RDY/BUSY pin is an open drain output and a typical 3 kΩ pull-up resistor to V_{CC} is required. The pull-up resistor value is dependent on the number of OR-tied RDY/BUSY pins (applies to device types 13 through 17 and 23 through 28).

4.4.4 Set software data protection. Device types 01-05 and 08-12 software data protection offers a method of preventing inadvertent writes. These devices are placed in protected state by writing a series of instructions (see figure 9) to the device. Once protected, writing to the device may only be performed by executing the same sequence of instructions appended with either a byte write operation or page write operation. The waveforms and timing relationships shown on figures 4 - 8 and the test conditions and limits specified in table I shall apply.

4.4.4.1 Reset software data protection. Device types 01-05 and 08-12 protection feature is reset by writing a series of instructions (see figure 10) to the device. The waveforms and timing relationships shown on figures 4 - 8 and the test conditions and limits specified in table I shall apply.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-03-25

Approved sources of supply for SMD 5962-87514 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 3/
5962-8751401XA	2/	X28C64DMB-35
5962-8751401YA	2/	X28C64EMB-35
5962-8751401ZC	2/	X28C64FMB-35
5962-8751402XA	2/	X28C64DMB-30
5962-8751402YA	2/	X28C64EMB-30
5962-8751402ZC	2/	X28C64FMB-30
5962-8751403XA	2/ 3DTT2	X28C64DMB-25 PYX28C64-25CWMB
5962-8751403YA	2/ 3DTT2	X28C64EMB-25 PYX28C64-25L32MB
5962-8751403ZC	2/	X28C64FMB-25
5962-8751404XA	2/	X28C64DMB-20
5962-8751404YA	2/	X28C64EMB-20
5962-8751404ZC	2/	X28C64FMB-20
5962-8751405XA	2/	X28C64DMB-25
5962-8751405YA	2/ 3DTT2	X28C64EMB-25 PYX28C64X-25L32MB
5962-8751405ZC	2/	X28C64FMB-25
5962-8751406XA	0C7V7 3DTT2	AT28C64B-35DM/883 PYA28C64B-35CWMB
5962-8751406UA	2/	AT28PC64-35KM/883
5962-8751406YA	0C7V7 3DTT2	AT28C64B-35LM/883 PYA28C64B-35L32MB
5962-8751407XA	0C7V7 3DTT2	AT28C64B-30DM/883 PYA28C64B-30CWMB
5962-8751407UA	2/	AT28PC64-30KM/883
5962-8751407YA	0C7V7 3DTT2	AT28C64B-30LM/883 PYA28C64B-30L32MB
5962-8751408XA	0C7V7 3DTT2	AT28C64B-25DM/883 PYA28C64B-25CWMB
5962-8751408UA	2/	AT28PC64-25KM/883
5962-8751408YA	0C7V7 3DTT2	AT28C64B-25LM/883 PYA28C64B-25L32MB
5962-8751409XA	0C7V7 3DTT2	AT28C64B-20DM/883 PYA28C64B-20CWMB
5962-8751409UA	2/	AT28PC64-20KM/883
5962-8751409YA	0C7V7 3DTT2	AT28C64B-20LM/883 PYA28C64B-20L32MB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 3/
5962-8751410XA	0C7V7 3DTT2	AT28C64B-12DM/883 PYA28C64B-12CWMB
5962-8751410UA	2/	AT28HC64L-12KM/883
5962-8751410YA	0C7V7 3DTT2	AT28C64B-12LM/883 PYA28C64B-12L32MB
5962-8751411XA	0C7V7 3DTT2	AT28C64B-90DM/883 PYA28C64B-90CWMB
5962-8751411UA	2/	AT28HC64L-90KM/883
5962-8751411YA	0C7V7 3DTT2	AT28C64B-90LM/883 PYA28C64B-90L32MB
5962-8751412XA	2/	AT28HC64B-70DM/883
5962-8751412UA	2/	AT28HC64L-70KM/883
5962-8751412YA	2/	AT28HC64L-70LM/883
5962-8751413XA	0C7V7 3DTT2	AT28C64-35DM/883 PYA28C64-35CWMB
5962-8751413UA	2/	AT28C64-35KM/883
5962-8751413YA	0C7V7 3DTT2	AT28C64-35LM/883 PYA28C64-35L32MB
5962-8751413ZA	2/	AT28C64-35FM/883
5962-8751414XA	0C7V7 3DTT2	AT28C64-30DM/883 PYA28C64-30CWMB
5962-8751414UA	2/	AT28C64-30KM/883
5962-8751414YA	0C7V7 3DTT2	AT28C64-30LM/883 PYA28C64-30L32MB
5962-8751415XA	0C7V7 3DTT2	AT28C64-25DM/883 PYA28C64-25CWMB
5962-8751415UA	2/	AT28C64-25KM/883
5962-8751415YA	0C7V7 3DTT2	AT28C64-25LM/883 PYA28C64-25L32MB
5962-8751415ZA	2/	AT28C64-25FM/883
5962-8751416XA	0C7V7 3DTT2	AT28C64-20DM/883 PYA28C64-20CWMB
5962-8751416UA	2/	AT28C64-20KM/883
5962-8751416YA	0C7V7 3DTT2	AT28C64-20LM/883 PYA28C64-20L32MB
5962-8751417XA	0C7V7 3DTT2	AT28C64-15DM/883 PYA28C64-15CWMB
5962-8751417UA	2/	AT28C64-15KM/883
5962-8751417YA	0C7V7 3DTT2	AT28C64-15LM/883 PYA28C64-15L32MB
5962-8751418XA	2/ 3DTT2	AT28C64-35DM/883 PYA28C64X-35CWMB
5962-8751418UA	2/	AT28C64X-35KM/883
5962-8751418YA	2/ 3DTT2	AT28C64-35LM/883 PYA28C64X-35L32MB

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 3/
5962-8751419XA	2/ 3DTT2	AT28C64X-30DM/883 PYA28C64X-30CWMB
5962-8751419UA	2/	AT28C64X-30KM/883
5962-8751419YA	2/ 3DTT2	AT28C64X-30LM/883 PYA28C64X-30L32MB
5962-8751420XA	2/ 3DTT2	AT28C64X-25DM/883 PYA28C64X-25CWMB
5962-8751420UA	2/	AT28C64X-25KM/883
5962-8751420YA	2/ 3DTT2	AT28C64X-25LM/883 PYA28C64X-25L32MB
5962-8751420ZA	2/	AT28C64X-25FM/883
5962-8751421XA	2/ 3DTT2	AT28C64X-20DM/883 PYA28C64X-20CWMB
5962-8751421UA	2/	AT28C64X-20KM/883
5962-8751421YA	2/ 3DTT2	AT28C64X-20LM/883 PYA28C64X-20L32MB
5962-8751422XA	2/ 3DTT2	AT28C64X-15DM/883 PYA28C64X-15CWMB
5962-8751422UA	2/	AT28C64X-15KM/883
5962-8751422YA	2/ 3DTT2	AT28C64X-15LM/883 PYA28C64X-15L32MB
5962-8751423XA	2/	DM28C65-350/B
5962-8751423YA	2/	LM28C65-350/B
5962-8751423ZA	2/	FM28C65-350/B
5962-8751424XA	2/	DM28C65-300/B
5962-8751424YA	2/	LM28C65-300/B
5962-8751424ZA	2/	FM28C65-300/B
5962-8751425XA	2/	DM28C65-250/B
5962-8751425YA	2/	LM28C65-250/B
5962-8751425ZA	2/	FM28C65-250/B
5962-8751426XA	2/	DM28C65-200/B
5962-8751426YA	2/	LM28C65-200/B
5962-8751426ZA	2/	FM28C65-200/B
5962-8751427XA	2/	DM55C65-250/B
5962-8751427YA	2/	LM55C65-250/B
5962-8751427ZA	2/	FM55C65-250/B
5962-8751428XA	2/	AT28C64F-20DM/883
5962-8751428YA	2/	AT28C64F-20LM/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Not available from an approved source.
3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3DTT2	Pyramid Semiconductor Corp. 1340 Bordeaux Drive Sunnyvale, CA 94089
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

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