REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline S to device type 01. Add device type 02 to drawing for case outlines R, S, and 2. Add vendors CAGE 75569 and 27014 to device type 01. Add vendors CAGE 61722 and 75569 to device type 02. Editorial changes to table I and throughout drawing.	89-12-07	Michael A. Frye
B	Add notes to figure 4, switching waveforms and test circuit. Update the boilerplate to current requirements as specified in MIL-PRF-38535. Editorial changes throughout. - jak	06-04-18	Thomas M. Hess
C	Add footnote 4/ to I_{CC} test in table I. – jak	10-01-06	Thomas M. Hess

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			C	C	C	C	C	C	C	C	C	C				
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10				

PMIC N/A

PREPARED BY
James E. Nicklaus

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Monica L. Poelking

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
87-11-16

MICROCIRCUIT, DIGITAL, FAST CMOS, OCTAL D-TYPE FLIP-FLOP WITH CLEAR, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
C	**A**	**67268**	**5962-87656**

SHEET 1 OF 10

DSCC FORM 2233
APR 97

5962-E075-10

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-87656	01	R	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54FCT273	Octal D-type flip-flop with clear, TTL compatible inputs
02	54FCT273A	Octal D-type flip-flop with clear, TTL compatible inputs

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC input diode current (I_{IK}) ..... -20 mA
DC output diode current (I_{OK}) ..... -50 mA
DC output current (I_{OUT}) ..... $\pm$100 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Maximum power dissipation (P_D) ..... 500 mW
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Maximum low level input voltage (V_{IL}) ..... 0.8 V
Minimum high level input voltage (V_{IH}) ..... 2.0 V
Case operating temperature range (T_C) ..... -55°C to +125°C
Minimum setup time, high or low, data to CP (t_s):
  Device type 01 ..... 3.5 ns
  Device type 02 ..... 3.0 ns
Minimum hold time, high or low, data to CP (t_h):
  Device type 01 ..... 2.5 ns
  Device type 02 ..... 2.0 ns
Minimum CP pulse width, high or low (t_{w1}):
  Device type 01 ..... 7.0 ns
  Device type 02 ..... 6.0 ns
Minimum removal time, $\overline{MR}$ to CP (t_{REM}):
  Device type 01 ..... 5.0 ns
  Device type 02 ..... 3.0 ns
Minimum $\overline{MR}$ pulse width, low (t_{w2}):
  Device type 01 ..... 7.0 ns
  Device type 02 ..... 6.0 ns

1/ Unless other wise specified, all voltages are referenced to ground.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ± 10% unless otherwise specified		V_{CC}	Device type	Group A subgroups	Limits		Unit
							Min	Max	
High level output voltage	V_{OH}	V_{IL} = 0.8 V V_{IH} = 2.0 V	I_{OH} = -300 µA	4.5 V	All	1, 2, 3	4.3		V
			I_{OH} = -12 mA				2.4		
Low level output voltage	V_{OL}	V_{IL} = 0.8 V V_{IH} = 2.0 V	I_{OL} = +300 µA	4.5 V	All	1, 2, 3		0.2	V
			I_{OL} = +32 mA					0.5	
Input clamp voltage	V_{IK}	I_{IN} = -18 mA		4.5 V	All	1		-1.2	V
High level input current	I_{IH}	V_{IN} = 5.5 V		5.5 V	All	1, 2, 3		5.0	µA
Low level input current	I_{IL}	V_{IN} = GND		5.5 V	All	1, 2, 3		-5.0	µA
Short circuit current	I_{OS} 1/	V_{OUT} = GND		5.5 V	All	4	-60		mA
Quiescent power supply current (CMOS inputs)	I_{CCQ}	$V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V $f_i = f_{CP}$ = 0 MHz		5.5 V	All	1, 2, 3		1.5	mA
Quiescent power supply current (TTL inputs)	ΔI_{CC} 2/	V_{IN} = 3.4 V		5.5 V	All	1, 2, 3		2.0	mA
Dynamic power supply current	I_{CCD} 3/ 4/	$\overline{MR} = V_{CC}$ Outputs open One bit toggling, 50% duty cycle $V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V		5.5 V	All	3/		0.25	mA/ MHz
Total power supply current	I_{CC} 4/ 5/	$V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V f_{CP} = 10 MHz Outputs open One bit toggling at f_i = 5 MHz 50% duty cycle $\overline{MR} = V_{CC}$		5.5 V	All	1, 2, 3		4.0	mA
		V_{IN} = 3.4 V or V_{IN} = GND f_{CP} = 10 MHz Outputs open eight bits toggling at f_i = 2.5 MHz 50% duty cycle $\overline{MR} = V_{CC}$		5.5 V	All	1, 2, 3		6.0	mA
Input capacitance	C_{IN}	See 4.3.1c			All	4		10	pF
Input capacitance	C_{OUT}	See 4.3.1c			All	4		12	pF
Functional tests		See 4.3.1d		4.5 V	All	7, 8			
Propagation delay time, CP to On	t_{PHL1}, t_{PLH1} 6/	C_L = 50 pF ±10% R_L = 500Ω ±5% R_T = 50Ω See figure 4		4.5 V	01	9, 10, 11	2.0	15.0	ns
				4.5 V	02	9, 10, 11	2.0	8.3	
Propagation delay time, $\overline{MR}$ to On	t_{PHL2} 6/			4.5 V	01	9, 10, 11	2.0	15.0	ns
				4.5 V	02	9, 10, 11	2.0	8.3	

1/ Not more than one output should be shorted at one time, and the duration of the short circuit condition should not exceed 1 second.

2/ For TTL driven inputs, V_{IN} = 3.4 V; all other inputs are equal to V_{CC} or GND.

3/ This parameter is not directly testable, but is derived for use in total power supply calculations.

4/ For I_{CC} tests, in an ATE environment, the effect of parasitic output capacitive loading from the test environment must be taken into account,as its effect is not intended to be included in the test results. The impact must be characterized and appropriate offset factors must be applied to the test result."

5/ $I_{CC} = I_{CCQ} + (\Delta I_{CC} D_H N_T) + I_{CCD}(f_{CP}/2 + f_i N_i)$, where: D_H = duty cycle for TTL input high; N_T = number of TTL inputs at D_H; f_i = input frequency in MHz; N_i = number of inputs at f_i; f_{CP} = clock frequency in MHz.

6/ The minimum limits are guaranteed, if not tested, to the specified limits in table I.

Device types	01 and 02
Case outlines	R, S, and 2
Terminal number	Terminal symbol
1	$\overline{MR}$
2	O0
3	D0
4	D1
5	O1
6	O2
7	D2
8	D3
9	O3
10	GND
11	CP
12	O4
13	D4
14	D5
15	O5
16	O6
17	D6
18	D7
19	O7
20	V_{CC}

FIGURE 1. Terminal connections.

Operating mode	Inputs			Outputs
	$\overline{MR}$	CP	Dn	On
Reset (clear)	L	X	X	L
Load “1”	H	↑	h	H
Load “0”	H	↑	l	L

L = Low voltage level
H = High voltage level
↑ = Low-to-high transition of the clock
h = High voltage level one setup time prior to the low-to-high clock transition
l = Low voltage level one setup time prior to the low-to-high clock transition
X = Don’t care

FIGURE 2. Truth table.

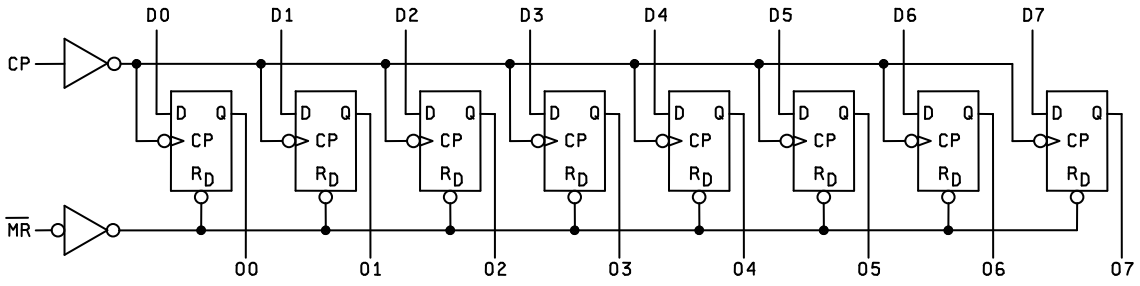
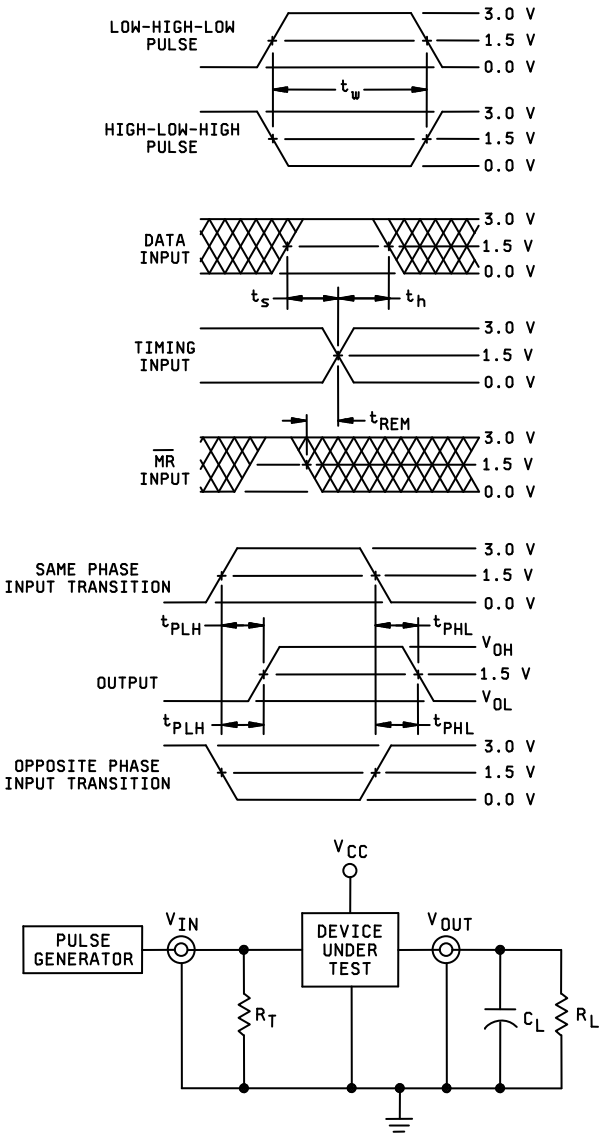


FIGURE 3. Logic diagram.



NOTES:

1. R_L = 500Ω or equivalent.
2. R_T = 50Ω or equivalent, terminal resistance which should be equal to Z_{OUT} of the pulse generator.
3. C_L = 50 pF or equivalent (includes test jig and probe capacitance).
4. Pulse generator for all pulses: $t_f \leq 2.5$ ns; $t_r \leq 2.5$ ns.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Test all applicable pins on 5 devices with zero failures.

d. Subgroup 7 and 8 tests shall include verification of the truth table as specified on figure 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-01-06

Approved sources of supply for SMD 5962-87656 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8765601RA	0C7V7	54FCT273DMQB
5962-8765601SA	0C7V7	54FCT273FMQB
5962-87656012A	0C7V7	54FCT273LMQB
5962-8765602RA	3/	54FCT273A
5962-8765602SA	3/	54FCT273A
5962-87656022A	3/	54FCT273A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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