REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R005-91.	91-09-24	M. A. Frye
B	Changed the minimum clock period for device 02 from 45 to 40 ns. Boilerplate update. ksr	99-07-28	Raymond Monnin
C	Boilerplate update, part of 5 year review. ksr	05-09-29	Raymond Monnin
D	Boilerplate update, part of 5 year review. ksr	10-11-10	Charles F. Saffle

REV																			
SHEET																			
REV																			
SHEET																			

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Rick Officer

DLA LAND AND MARITIME

COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Raymond Monnin

APPROVED BY
D. A. DiCenzo

DRAWING APPROVAL DATE
88-07-28

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, FIELD PROGRAMMABLE GATE ARRAY, MONOLITHIC SILICON

REVISION LEVEL
D

SIZE	CAGE CODE	
A	**67268**	**5962-88637**

SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962- 88637	01	L	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	t_{PD}
01	20G10	24 Pin Generic CMOS PLD	40 ns
02	20G10	24 Pin Generic CMOS PLD	30 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	flat package
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line package
3	CQCC1-N28	28	square leadless chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
DC voltage applied to Outputs in High Z state range	-0.5 V dc to +7.0 V dc
DC Input voltage	-3.0 V dc to +7.0 V dc
DC program voltage	+14.0 V dc
Maximum power dissipation 1/	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	See MIL-STD-1835
Junction temperature (T_J) 2/	+150°C
Storage temperature range	-65°C to +150°C
Temperature under bias range	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
High level input voltage range (V_{IH})	2.0 V dc to V_{CC}
Low level input voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2/ Maximum junction temperature may be increased to 175°C during burn-in and steady state life.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturer's approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table (unprogrammed devices). The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.4 Programmed devices. The truth table for programmed devices shall be specified by an altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, Appendix A.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime 's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 4.4). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowed.

e. For unprogrammed devices, 10 devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

f. Subgroups 7 and 8 shall consist of verifying the pattern specified.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type	Group A sub-groups	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.0 mA, $V_{IN} = V_{IH}$ or V_{IL}	All	1,2,3	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 12 mA, $V_{IN} = V_{IH}$ or V_{IL}	All	1,2,3		0.5	V
Input high voltage 1/	V_{IH}		All	1,2,3	2.0		V
Input low voltage 1/	V_{IL}		All	1,2,3		0.8	V
Input current	I_{IX}	V_{IN} = 5.5 V to GND	All	1,2,3	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V V_{OUT} = 5.5 V and GND	All	1,2,3	-100	+ 100	µA
Output short circuit current 2/ 3/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V	All	1,2,3		-90	mA
Power supply current	I_{CC}	V_{CC} = 5.5 V, I_{OUT} = 0 mA V_{IN} = 2.0 V	All	1,2,3		80	mA
Input capacitance	C_{IN}	f = 1.0 Mhz; V_{IN} = 0.0 V; T_A = +25°C	All	4		10	pF
Output capacitance	C_{OUT}	V_{CC} = 5.0V (see 4.3.1c); V_{OUT} = 0.0 V	All	4		10	pF
Functional tests		See 4.3.1d V_{IL} = 0.0 V, V_{IH} = 3.0 V	All	7, 8			
Input or feedback to non-registered output 4/	t_{PD}		01	9,10,11		40	ns
			02			30	
Input to output enable 3/ 4/	t_{EA}		01	9,10,11		40	ns
			02			30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type	Group A sub-groups	Limits Min	Limits Max	Unit
Input to output disable 3/ 5/	t_{ER}		01	9,10,11		40	ns
			02			30	
$\overline{OE}$ to output enabled 5/	t_{PZX}		All	9,10,11		25	ns
$\overline{OE}$ to output disabled 3/ 5/	t_{PXZ}		All	9,10,11		25	ns
Clock to output 4/	t_{CO}		01	9,10,11		25	ns
			02			20	
Input or feedback setup time 4/	t_S		01	9,10,11	35		ns
			02		20		
Hold time 4/	t_H		All	9,10,11	0		ns
Clock period 3/ 4/	t_P		01	9,10,11	60		ns
			02		40		
Clock width 3/ 4/	t_W		01	9,10,11	25		ns
			02		20		
Maximum frequency 3/ 4/	f_{MAX}		01	9,10,11		16.5	MHz
			02			25	

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

2/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed one second.

3/ If not tested, shall be guaranteed to the values specified in table I.

4/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, output loading of the specified I_{OL}/I_{OH} and 50 pF load capacitance. (See figures 3a and 4).

5/ Transition is measured at steady state high level -500 mV or steady state low level +500 mV on the output from the 1.5 V level on the input and 5 pF load capacitance. (See figures 3b and 4).

Device	Terminal	
	01, 02	
Case	K, L	3
Terminal number		
1	CP/I	CP/I
2	I	I
3	I	I
4	I	NC
5	I	I
6	I	I
7	I	I
8	I	I
9	I	I
10	I	I
11	I	NC
12	GND	I
13	I/$\overline{OE}$	I
14	I/O	GND
15	I/O	I/$\overline{OE}$
16	I/O	I/O
17	I/O	I/O
18	I/O	NC
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	V_{CC}	I/O
25	---	NC
26	---	I/O
27	---	I/O
28	---	V_{CC}

FIGURE 1. Terminal connections.

Truth table																					
Input pins												Output pins									
CP/I	I/$\overline{OE}$	I	I	I	I	I	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

NOTES:
1. Z = 3-state
2. X = Don't care

FIGURE 2. Truth table (unprogrammed).

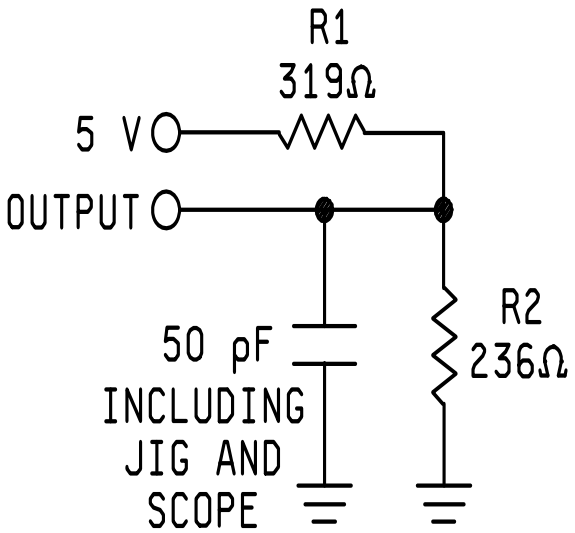

FIGURE 3a. Output load circuit (CL = 50 pF)

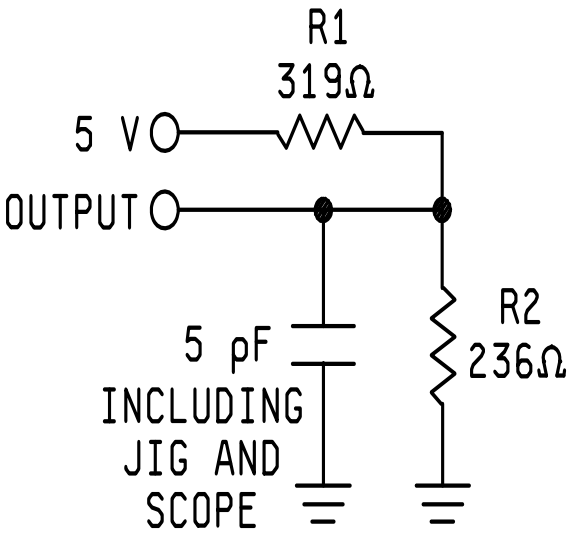

FIGURE 3b. Output load circuit (CL = 5 pF)

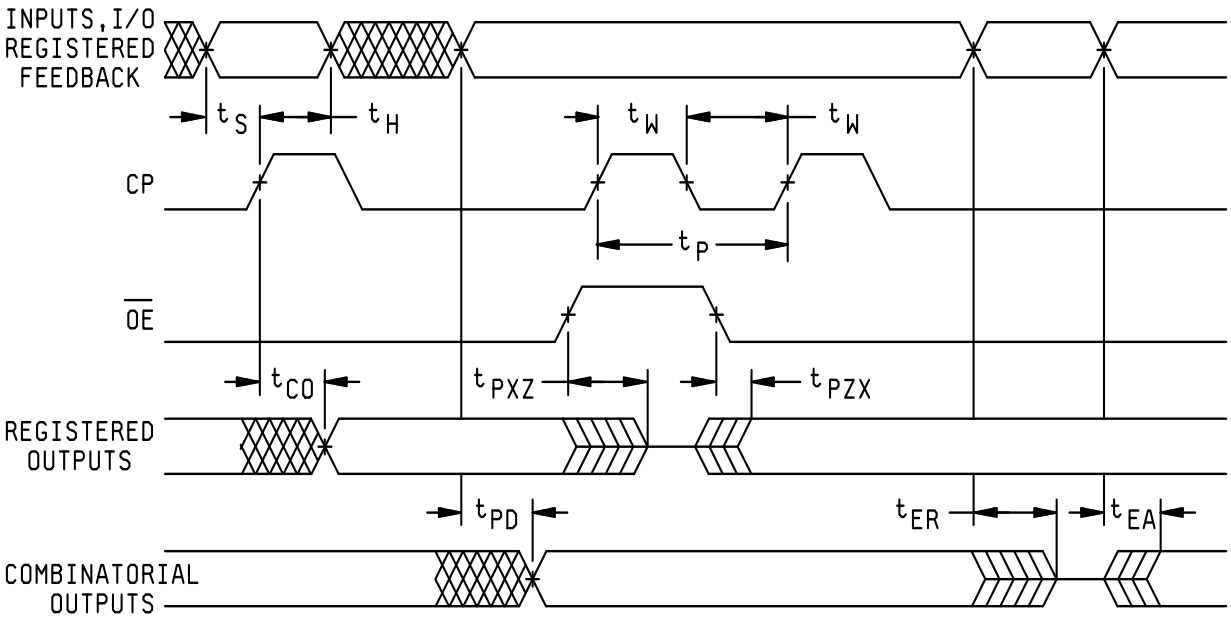

FIGURE 4. Switching waveforms.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I) 1/
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7*,8A, 8B,9,10,11
Final electrical test parameters (method 5004) for unprogrammed devices	1*,2,3,7*,8A,8B
Group A test requirements (method 5005)	1,2,3,4**,7***,8A***, 8B***,9,10,11
Group C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B

1/ Any or all subgroups may be combined when using high speed testers.
* PDA applies to subgroups 1 and 7.
** For subgroup 4, see 4.3.1c
*** See 4.3.1f.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) All devices shall be programmed with a pattern that assures all inputs and I/O's are dynamically switched.

c. For quality conformance inspections, the programmability sample (see 4.3.1e) shall be included in the subgroup 1 test.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available to the user on request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-11-10

Approved sources of supply for SMD 5962-88637 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standardized military drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8863701KA	0C7V7	PLDC20G10-40KMB
5962-8863701LA	0C7V7	PLDC20G10-40DMB
5962-88637013A	0C7V7	PLDC20G10-40LMB
5962-8863702KA	0C7V7	PLDC20G10-30KMB
5962-8863702LA	0C7V7	PLDC20G10-30DMB
5962-88637023A	0C7V7	PLDC20G10-30LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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