REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add CAGE number 50364 as a supplier for 02 and 03 device types. Add 04 device type. Add CAGE number 1FN41 as a supplier of the K package. Editorial changes throughout entire document. Remove C as a test condition option.	89-08-23	M. A. Frye
B	Change C_I and C_O values in Table I. Incorporate power reset feature. Add 05 device. Add CAGE number 65786 for 04K, 04L and 043 devices. Add footnote 7/ to Table I. Editorial changes throughout entire document.	91-11-06	M. A. Frye
C	Update drawing to current requirements. Editorial changes throughout. - gap	01-11-02	Raymond Monnin
D	Boilerplate update part of 5 year review. ksr	06-08-18	Raymond Monnin
E	Corrected I_{IL} and I_{IH} parameters in Table I. ksr	10-03-29	Charles F. Saffle

THE ORIGINAL FRONT PAGE HAS BEEN REPLACED.

REV																				
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REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

PREPARED BY
Jeffery D. Bowling

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-07-27

REVISION LEVEL
E

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, ONE-TIME PROGRAMMABLE, PROGRAMMABLE ARRAY LOGIC, MONOLITHIC SILICON

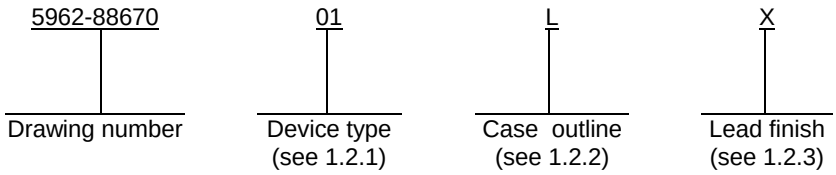
SIZE	CAGE CODE	
A	**67268**	**5962-88670**

SHEET 1 OF 11

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	C22V10	22-input 10-output and-or-logic array	25 ns
02	C22V10	22-input 10-output and-or-logic array	30 ns
03	C22V10	22-input 10-output and-or-logic array	40 ns
04	C22V10	22-input 10-output and-or-logic array	20 ns
05	C22V10	22-input 10-output and-or-logic array	15 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	Flat package
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range ..... -0.5 V dc to +7.0 V dc
Input voltage range ..... -2.0 V dc to +7.0 V dc 2/
Output voltage applied range ..... -0.5 V dc to +7.0 V dc 2/
Output sink current ..... 16 mA
Thermal resistance, junction-to-case (θ_{JC}): ..... See MIL-STD-1835
Maximum power dissipation (P_D) 3/ ..... 1.2 W
Maximum junction temperature (T_J) ..... +175°C
Lead temperature (soldering, 10 seconds maximum) ..... +260°C
Storage temperature range ..... -65°C to +150°C
Temperature under bias ..... -55°C to +125°C

1/ All voltages referenced to V_{SS}.
2/ Minimum voltage is -0.6 V dc which may undershoot to -2.0 V dc for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75 V dc which may overshoot to +7.0 V dc for pulses of less than 20 ns.
3/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) ..... 4.5 V dc to 5.5 V dc
High level input voltage (V_{IH}) ..... 2.0 V dc minimum
Low level input voltage (V_{IL}) ..... 0.8 V dc maximum
Case operating temperature range (T_C) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, C, or D (see 4.3), the devices shall be programmed by the manufacturer prior to test with a minimum of 50 percent of the total number of gates programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.3.2 Programmed devices. The truth tables for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.10.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 7/ V_{SS} = 0 V, -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_O = -2.0 mA V_{IH} = 2.0 V V_{IL} = 0.8 V	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	I_O = 12.0 mA V_{IH} = 2.0 V V_{IL} = 0.8 V	1, 2, 3	All		0.5	V
High impedance output leakage current 2/	I_{OZ}	V_{CC} = 5.5 V	1, 2, 3	All	-40	40	µA
High level input current	I_{IH}	V_{IH} = 5.5 V (excludes I/O pins)	1, 2, 3	All	-10	+10	µA
Low level input current	I_{IL}	V_{IL} = GND (excludes I/O pins)	1, 2, 3	All	-10	+10	µA
Standby power supply current	I_{CC}	V_{CC} = 5.5 V, V_{IN} = GND	1, 2, 3	01-03		100	mA
				04, 05		120	mA
Output short circuit current 3/ 4/	I_{OS}	V_{CC} = 5.5 V, V_O = 0.5 V Outputs open for unprogrammed device	1, 2, 3	All	-30	-90	mA
Input capacitance 4/ 5/	C_I	V_I = 0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz, (see 4.3.1c)	4	All		10	pF
Output capacitance 4/ 5/	C_O	V_O = 0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz, (see 4.3.1c)	4	All		10	pF
Functional test		See footnote 4/ of Table IIA	7,8A,8B	All			
Input to output enable	t_{EA}	V_{CC} = 4.5 V, C_L = 5 pF, See figure 3 (circuit A) and figure 4	9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
				05		15	
Input to output disable	t_{ER}		9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
				05		15	
Input or feedback to nonregistered output	t_{PD}	V_{CC} = 4.5 V, C_L = 50 pF, See figure 3 (circuit B) and figure 4	9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
				05		15	
Clock to output	t_{CO}		9, 10, 11	01, 04		15	ns
				02		20	
				03		25	
				05		10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 7/ V_{SS} = 0 V, -55°C ≤ T_C ≤ +125°C 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock period (t_{co} + t_s)	t_P	V_{CC} = 4.5 V, C_L = 50 pF, See figure 3 (circuit B) and figure 4	9, 10, 11	01	33		ns
				02	40		
				03	55		
				04	32		
				05	22		
Clock pulse width 4/ 6/	t_W		9, 10, 11	01, 04	15		ns
				02	20		
				03	27		
				05	6		
Setup time 4/ 6/	t_S		9, 10, 11	01	18		ns
				02	20		
				03	30		
				04	17		
				05	12		
Hold time 4/ 6/	t_H		9, 10, 11	All	0		ns
Maximum clock frequency 4/ 6/	f_{MAX}		9, 10, 11	01	30		MHz
				02	25		
				03	18		
				04	31		
				05	45		
Asynchronous reset pulse width	t_{AW}		9, 10, 11	01	25		ns
				02	30		
				03	40		
				04	20		
				05	15		
Asynchronous reset recovery time	t_{AR}		9, 10, 11	01	25		ns
				02	30		
				03	40		
				04	20		
				05	15		
Asynchronous reset to registered output reset	t_{AP}		9, 10, 11	01, 04		25	ns
				02		30	
				03		40	
				05		20	
Power-up reset time 4/	t_{PR}	See figure 5	9, 10, 11	All		1	µs

1/ All voltages are referenced to ground.
2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZ}.
3/ Only one output shorted at a time.
4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ All pins not being tested are to be open.
6/ Test applies only to register outputs.
7/ AC testing. Input pulse levels are 0 to 3.0 V with transition times of 5ns or less. Timing reference levels are 1.5 V unless otherwise specified.

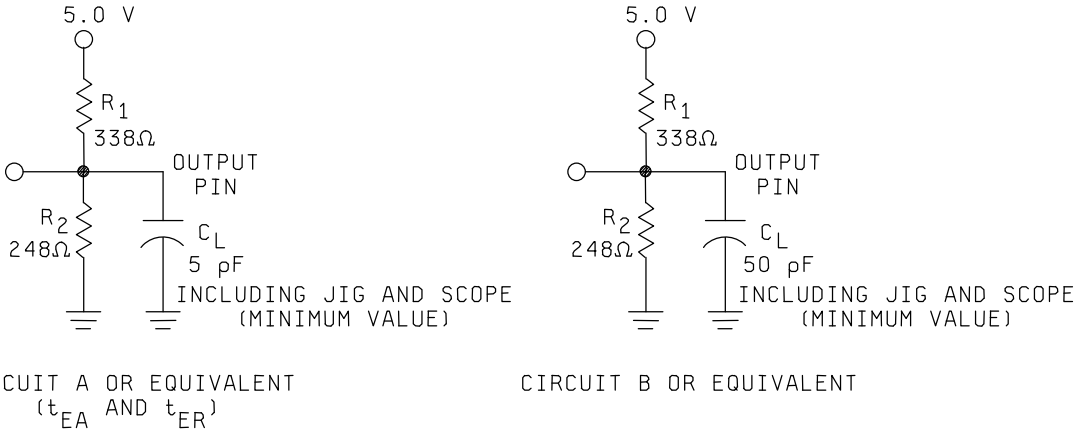
Device types	01, 02, 03, 04, 05	
Case outlines	K, L	3
Terminal number	Terminal symbol	
1	CP/I	NC
2	I	CP/I
3	I	I
4	I	I
5	I	I
6	I	I
7	I	I
8	I	NC
9	I	I
10	I	I
11	I	I
12	GND	I
13	I	I
14	I/O	GND
15	I/O	NC
16	I/O	I
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	NC
23	I/O	I/O
24	V_{CC}	I/O
25	---	I/O
26	---	I/O
27	---	I/O
28	---	V_{CC}

FIGURE 1. Terminal connections.

Truth table																					
Input pins												Output pins									
CP/I	I	I	I	I	I	I	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

NOTES:
1. Z = 3-state
2. X = don't care

FIGURE 2. Truth table (unprogrammed).



CIRCUIT A OR EQUIVALENT (t_{EA} AND t_{ER})

CIRCUIT B OR EQUIVALENT

NOTES:
1. AC testing. Inputs pulse levels are 0 to 3.0 V with transition times of 5 ns or less. Time reference levels are 1.5 V unless otherwise specified.
2. t_{EA} and t_{ER} transition are measured ±500 mV from steady state voltage.

FIGURE 3. Output test circuits.

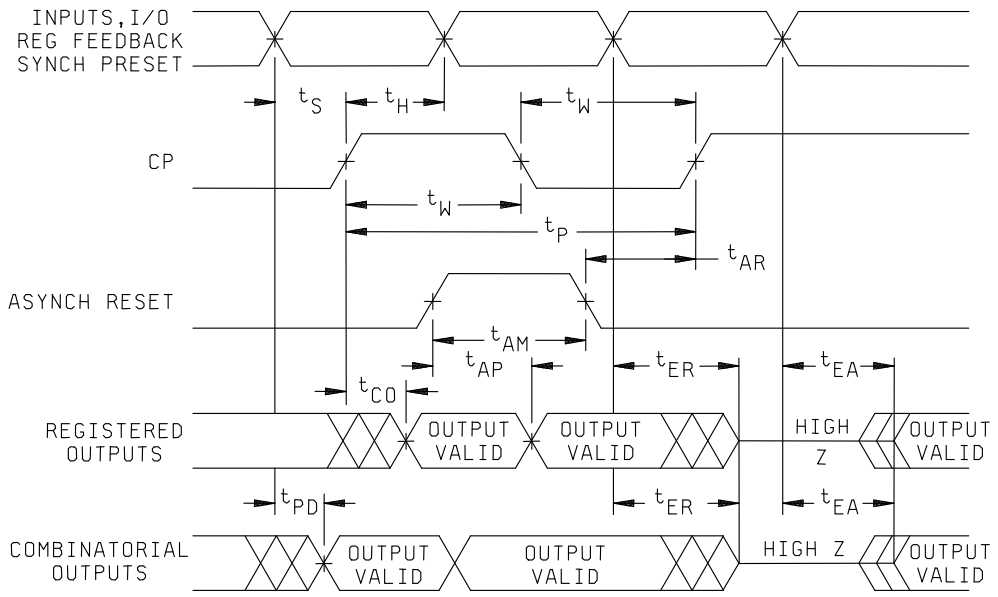
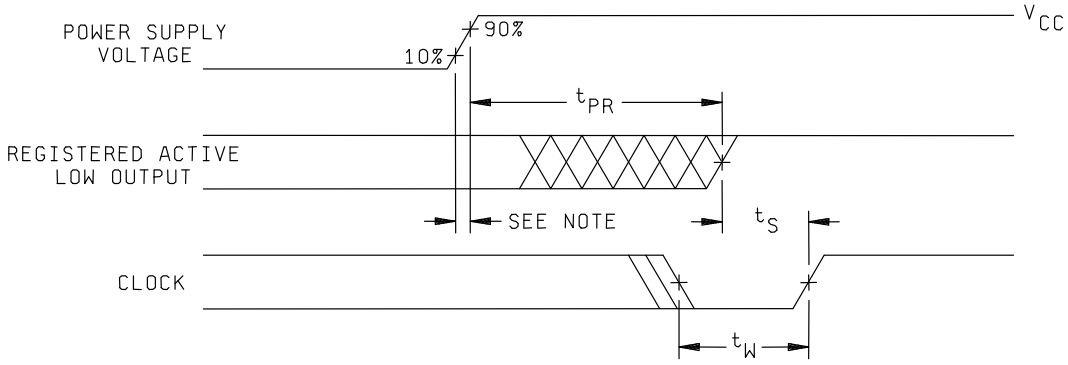


FIGURE 4. Switching waveforms.



NOTE: The power-up reset feature ensures that all flip-flops will be reset to low after the device has been powered up. The following conditions are required:

a) The V_{CC} rise must be monotonic.
b) After reset occurs, all applicable input and feedback setup times must be met before driving the clock pin high
c) The clock signal must remain stable beginning prior to the occurrence of the 10% level and continuing until the end of t_{PR}.

FIGURE 5. Power-up reset waveform.

TABLE II. Electrical test requirements. 1/, 2/, 3/, 4/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8A, 8B
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8A, 8B, 9
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ * indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ ** see 4.3.1c.
4/ Subgroups 7 and 8 functional tests shall also verify that no cells are programmed for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11.

(1) A sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.

(2) Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. For quality conformance inspection, the programmability sample (see 4.3.1d) shall be included in subgroup 1 test.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-03-29

Approved sources of supply for SMD 5962-88670 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8867001KA	0C7V7	PALC22V10-25KMB
	3/	AT22V10-25FM/883
5962-8867001LA	0C7V7	PALC22V10-25DMB
	3/	AT22V10-25GM/883
5962-88670013A	0C7V7	PALC22V10-25LMB
	3/	AT22V10-25NM/883
5962-8867002KA	0C7V7	PALC22V10-30KMB
	3/	AT22V10-30FM/883
5962-8867002LA	0C7V7	PALC22V10-30DMB
	3/	AT22V10-30GM/883
5962-88670023A	0C7V7	PALC22V10-30LMB
	3/	AT22V10-30NM/883
	3/	PALC22V10H-30ML883B
5962-8867003KA	0C7V7	PALC22V10-40KMB
	3/	AT22V10-40FM/883
5962-8867003LA	0C7V7	PALC22V10-40DMB
	3/	AT22V10-40GM/883
	3/	PALC22V10H-40MJS883B
5962-88670033A	0C7V7	PALC22V10-40LMB
	3/	AT22V10-40NM/883
5962-8867004KA	0C7V7	PALC22V10B-20KMB
	3/	AT22V10-20FM/883
5962-8867004LA	0C7V7	PALC22V10B-20DMB
	3/	AT22V10-20GM/883
5962-88670043A	0C7V7	PALC22V10B-20LMB
	3/	AT22V10-20NM/883
5962-8867005KA	0C7V7	PALC22V10B-15KMB
	3/	AT22V10-15FM/883
5962-8867005LA	0C7V7	PALC22V10B-15DMB
	3/	AT22V10-15GM/883
5962-88670053A	0C7V7	PALC22V10B-15LMB
	3/	AT22V10-15NM/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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