REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change to vendor similar part number. Change to table I. Removed programming procedures for method A, programming waveforms, table III, and ESDS from the drawing. Removed final electrical test from table II. Added device type 04. Editorial changes throughout.	90-02-26	M. A. Frye
B	Changes in accordance with NOR 5962-R059-96.	96-03-13	M. A. Frye
C	Update drawing to current requirements. Editorial changes throughout. - gap	01-11-05	Raymond Monnin
D	Boilerplate update, part of 5 year review. ksr	07-04-02	Robert M. Heber

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13		

PMIC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
88-09-09

REVISION LEVEL
D

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, DIGITAL, MEMORY, CMOS UV ERASABLE, PROGRAMMABLE LOGIC ARRAY, MONOLITHIC SILICON

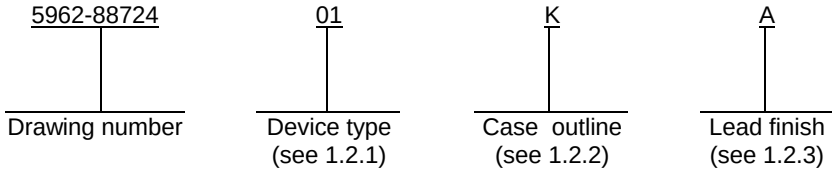
SIZE	CAGE CODE	
A	**67268**	**5962-88724**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	t_{PD}
01	C22V10L	22-input 10-output AND-OR-logic array	25 ns
02	C22V10L	22-input 10-output AND-OR-logic array	30 ns
03	C22V10L	22-input 10-output AND-OR-logic array	40 ns
04	C22V10L	22-input 10-output AND-OR-logic array	20 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	Flat package 1/
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line 1/
3	CQCC1-N28	28	Leadless chip carrier 1/

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 2/

Supply voltage range ..... -0.5 V dc to +7.0 V dc
Input voltage range ..... -2.0 V dc to +7.0 V dc 3/
Output voltage applied ..... -0.5 V dc to +7.0 V dc 3/
Output sink current ..... 16 mA
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Maximum power dissipation (P_D) 4/ ..... 1.2 W
Maximum junction temperature ..... +175°C
Lead temperature (soldering, 10 seconds maximum) ..... +300°C

1/ Lid shall be transparent to permit ultraviolet light erasure.

2/ All voltages referenced to V_{SS}.

3/ Minimum voltage is -0.6 V dc which may undershoot to -2.0 V dc for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75 V dc which may overshoot to +7.0 V dc for pulses of less than 20 ns.

4/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... 4.5 V dc to 5.5 V dc
High level input voltage (V_{IH}) ..... 2.0 V dc minimum
Low level input voltage (V_{IL}) ..... 0.8 V dc maximum
Case operating temperature range (T_C) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in group A, B, or C inspections (see 4.3), the devices shall be programmed by the manufacturer prior to test with a minimum of 50 percent of the total number of gates programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not part of this drawing.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPLDS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPLDS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.10.2 Programmability of EPLDS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.10.3 Verification of erasure of programmability of EPLDS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	I_O = -2.0 mA	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	I_O = 12.0 mA	1, 2, 3	All		0.5	V
High impedance output leakage current 2/	I_{OZ}	V_{CC} = 5.5 V and V_O = 5.5 V, V_O = GND	1, 2, 3	All	-10	10	µA
High level input current	I_{IH}	V_{IH} = 5.5 V	1, 2, 3	All		10	µA
		V_{IH} = 2.4 V	1, 2, 3	All		10	µA
Low level input current	I_{IL}	V_{IL} = 0.4 V	1, 2, 3	All		-10	µA
		V_{IL} = GND	1, 2, 3	All		-10	µA
Supply current	I_{CC}	V_{CC} = 5.5 V	1, 2, 3	All		15	mA
Output short circuit current 3/	I_{OS}	V_{CC} = 5.5 V	1, 2, 3	All	-30	-90	mA
Input capacitance	C_I 4/ 5/	V_I = 0 V, V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (see 4.3.1c)	4	All		10	pF
Output capacitance	C_O 4/ 5/	V_I = 0 V, V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (see 4.3.1c)	4	All		12	pF
Input or feedback to nonregistered output	t_{PD}	V_{CC} = 4.5 V, C_L = 50 pF See figure 4, circuit B and figure 5	9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
Clock to output	t_{CO}		9, 10, 11	01		15	ns
				02		20	
				03		25	
				04		15	
Input to output enable	t_{EA}	V_{CC} = 4.5 V, C_L = 5 pF See figure 4, circuit A and figure 5	9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
Input to output disable	t_{ER}		9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V -55°C ≤ T_C ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock pulse width 4/ 6/	t_W	V_{CC} = 4.5 V, C_L = 50 pF See figure 4, circuit B and figure 5	9, 10, 11	01	15		ns
				02	20		
				03	27		
				04	12		
Clock period	t_P		9, 10, 11	01	33		ns
				02	40		
				03	55		
				04	25		
Setup time 4/ 6/	t_S		9, 10, 11	01	18		ns
				02	20		
				03	30		
				04	17		
Hold time 4/ 6/	t_H		9, 10, 11	All	0		ns
Maximum clock frequency 4/ 6/	f_{MAX}		9, 10, 11	01	30		MHz
				02	25		
				03	18		
				04	40		
Asynchronous reset pulse width	t_{AW}		9, 10, 11	01	25		ns
				02	30		
				03	40		
				04	20		
Asynchronous reset recovery time	t_{AR}		9, 10, 11	01	25		ns
				02	30		
				03	40		
				04	20		
Asynchronous reset to registered output reset	t_{AP}		9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		22	

1/ All voltages are referenced to ground.
2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZ}.
3/ Only one output shorted at a time.
4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ All pins not being tested are to be open.
6/ Test applies only to registered outputs.

Device types	01 through 04	
Case outlines	L and K	3
Terminal number	Terminal symbol	
1	CK/I	NC
2	I	CK/I
3	I	I
4	I	I
5	I	I
6	I	I
7	I	I
8	I	NC
9	I	I
10	I	I
11	I	I
12	GND	I
13	I	I
14	I/O	GND
15	I/O	NC
16	I/O	I
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	NC
23	I/O	I/O
24	V_{CC}	I/O
25	---	I/O
26	---	I/O
27	---	I/O
28	---	V_{CC}

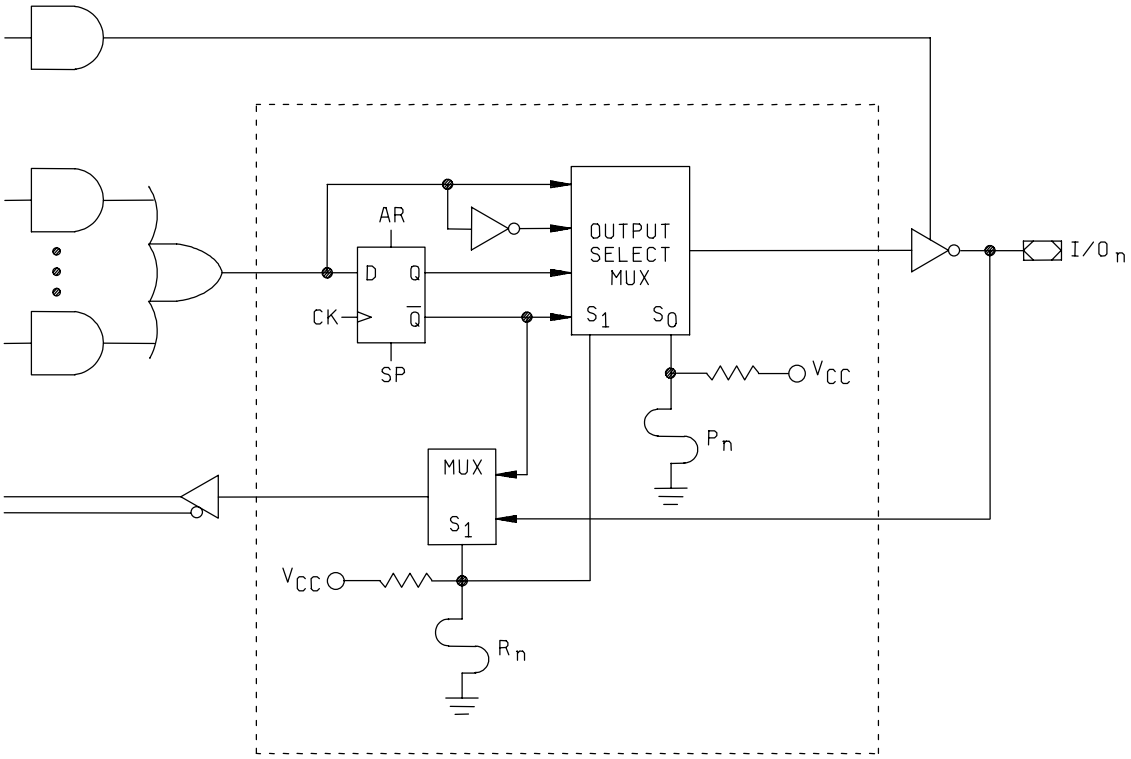
FIGURE 1. Terminal connections.

Truth table																					
Input pins												Output pins									
CK/I	I	I	I	I	I	I	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

NOTES:
1. Z = Three-state
2. X = Don't care

FIGURE 2. Truth table (unprogrammed).

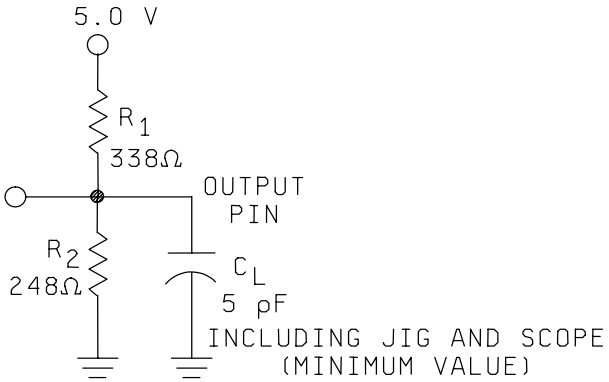
OUTPUT LOGIC MACROCELL



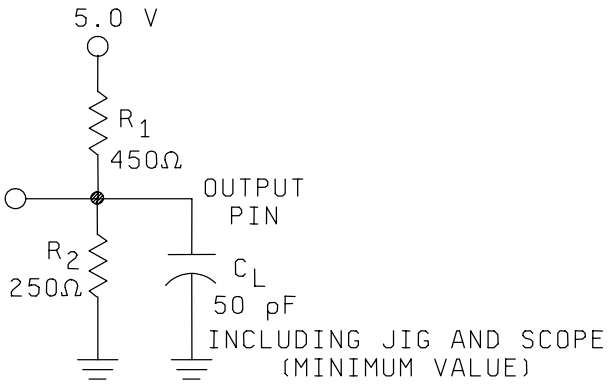
S1	S0	Output configuration
0	0	Registered/active low
0	1	Registered/active high
1	0	Combinatorial/active low
1	1	Combinatorial/active high

0 = Unblown fuse
1 = Blown fuse

FIGURE 3. Logic diagram (unprogrammed).

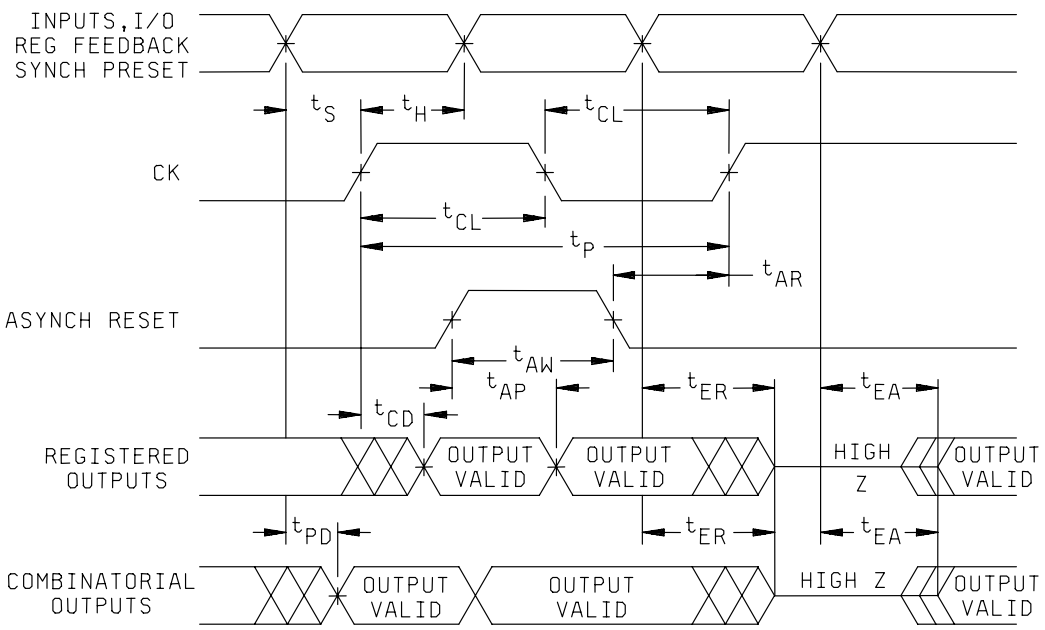


CIRCUIT A OR EQUIVALENT



CIRCUIT B OR EQUIVALENT

FIGURE 4. Output test circuit.



NOTE: Timing measurement reference is 1.5V. Input ac driving levels are 0.0 V and 3.0 V unless otherwise specified.

FIGURE 5. Switching waveforms.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method A.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell. The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using V_M = +5.8 V at +25°C using loose time (i.e., t_{ACC} = 1μs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Margin at V_M = 5.8 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 4.4), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.10.3).

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8

1/ (*) indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high speed testers.
3/ Subgroups 7 and 8 functional tests shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ (**) see 4.3.1c.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_I and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect input and output capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4 Erasing procedures. The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 1200 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990 or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-04-02

Approved sources of supply for SMD 5962-88724 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8872401KA	3/	AT22V10L-25YM/883
5962-8872401LA	1FN41	AT22V10L-25DM/883
	0C7V7	AT22V10L-25DM/883
	0EU86	AT22V10L-25DM/883
5962-88724013A	1FN41	AT22V10L-25LM/883
	0C7V7	AT22V10L-25LM/883
	0EU86	AT22V10L-25LM/883
5962-8872402KA	3/	AT22V10L-30YM/883
5962-8872402LA	0C7V7	AT22V10L-30DM/883
	0EU86	AT22V10L-30DM/883
5962-88724023A	0C7V7	AT22V10L-30LM/883
	0EU86	AT22V10L-30LM/883
5962-8872403KA	3/	AT22V10L-40YM/883
5962-8872403LA	0C7V7	AT22V10L-40DM/883
	0EU86	AT22V10L-40DM/883
5962-88724033A	0C7V7	AT22V10L-40LM/883
	0EU86	AT22V10L-40LM/883
5962-8872404KA	3/	AT22V10L-20YM/883
5962-8872404LA	1FN41	AT22V10L-20DM/883
	0C7V7	AT22V10L-20DM/883
	0EU86	AT22V10L-20DM/883
5962-88724043A	1FN41	AT22V10L-20LM/883
	0C7V7	AT22V10L-20LM/883
	0EU86	AT22V10L-20LM/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
1FN41	Atmel Corp. 2325 Orchard Parkway San Jose, CA 95131-1034
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051
0EU86	Austin Semiconductor Inc. 8701 Cross Park Dr. Austin, TX 78754-4566.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for EEPLD - Electronically Erasable Programmable Logic Devices ***category:***

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Other Similar products are found below :

ATF22V10C-10GM/883 ATF22V10C-7JU ATF16V8BQL15JU ATF22V10C-7PX ATF16V8BQL-15SU ATF22V10CQ-15JU ATF22V10CQZ-20XU ATF16V8B-15PC ATF16V8B-10JU ATF16V8B-15PU ATF16V8BQL-15PU ATF16V8BQL-15SU ATF22V10C-7SX ATF16V8B-15SU-T ATF16V8B-10JU ATF16V8B-15PU ATF22V10C-15PU ATF22V10C-10PU ATF22V10C-10SU ATF22V10CQZ-20JU ATF22V10C-10JU ATF22V10C-15JU ATF22V10CZ-15JC ATF22V10C-5JX ATF22V10CQZ-20SU ATF22V10C-7SX ATF22V10CQZ20PU ATF16V8B15SU