REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated boilerplate. Added device type 03. Moved endurance and data retention testing requirements from Section 4 of drawing to Section 3 of drawing. Converted case outline "Y" to standard package. Editorial changes throughout.	94-03-31	M. A. Frye
B	Boilerplate update, part of 5 year review. ksr	06-02-10	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
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SHEET																			

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B		
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Ray Monnin

APPROVED BY
D. R. Cool

DRAWING APPROVAL DATE
89-01-26

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUITS, MEMORY, DIGITAL, 16K X 8 UV EPROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89537**

SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-89537	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access time
01	(see 6.6)	16K x 8-bit UV EPROM	65 ns
02	(see 6.6)	16K x 8-bit UV EPROM	55 ns
03	(see 6.6)	16K x 8-bit UV EPROM	45 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style 1/
Y	CDIP3-T28 or GDIP4-T28	28	Dual-in-line
Z	GDFP2-F28	28	Flat package
U	CQCC1-N32	32	Rectangular leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC voltage range applied to the outputs in the high Z state	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
Maximum power dissipation	1.0 W 2/
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Storage temperature range (T_{STG})	-65°C to +150°C
Temperature under bias	-55°C to +125°C
Data retention	10 years, minimum
Endurance	25 cycles/byte, minimum

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C
Input high voltage range (V_{IH})	+2.0 V dc
Input low voltage range (V_{IL})	+0.8 V dc
Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc

1/ Lid shall be transparent to permit ultraviolet light erasure.

2/ Must withstand the added P_D due to short circuit test; e.g. , I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturer's approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When testing is required per 4.3 herein, the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be specified by an altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.6.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

3.6.3 Verification of state of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and shall be removed from the lot.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.10 Verification and review. DSCC, DSCC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.12 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output low voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL} , I_{OL} = 16 mA, V_{CC} = 4.5 V	1, 2, 3	All		0.5	V
Output high voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL} , I_{OH} = -4.0 mA, V_{CC} = 4.5 V	1, 2, 3	All	2.4		
Input high voltage 2/	V_{IH}		1, 2, 3	All	2.0		V
Input low voltage 2/	V_{IL}		1, 2, 3	All		0.8	
Input leakage current	I_{IX}	V_{IN} = GND to 5.5 V	1, 2, 3	All	-10	+10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, I_{OUT} = 0 mA V_{OUT} = GND and 5.5 V	1, 2, 3	All	-40	+40	µA
Output short circuit current	I_{OS} 3/ 4/	V_{CC} = 5.5 V, V_{OUT} =0.0 V	1, 2, 3	All	-20	-90	mA
Power supply current	I_{CC}	V_{CC} = 5.5 V, I_{OUT} = 0 mA f = 16.7 MHz Inputs cycling from 0 to 3 V	1, 2, 3	All		120	mA
Standby supply current	I_{SB}	V_{CC} = 5.5 V, I_{OUT} = 0 mA V_{IN} = 2.0 V	1, 2, 3	All		35	mA
Input capacitance	C_{IN} 4/	V_{IN} = 0 V, V_{CC} = 5.0 V f = 1 Mhz, T_A = +25°C See 4.3.1c	4	All		10	pF
Output capacitance	C_{OUT} 4/	V_{OUT} = 0 V, V_{CC} = 5.0 V f = 1 Mhz, T_A = +25°C See 4.3.1c	4	All		10	pF
Functional tests		See 4.3.1e	7, 8A, 8B	All			
Address to output valid	t_{AA}	See figure 4	9, 10, 11	01		65	ns
				02		55	
				03		45	
Chip select active to output valid 5/	t_{ACS1}		9, 10, 11	01		35	ns
				02		30	
				03		25	
Chip select active to output valid 6/	t_{ACS2}		9, 10, 11	01		70	ns
				02		60	
				03		50	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ 4.5 V dc $\le V_{CC} \le$ 5.5 V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Chip select active to power_up 4/ 6/ 7/	t_{PU}	See figure 4 V_{CC} = 4.5 V	9, 10, 11	All	0		ns
Chip select inactive to power_down 4/ 6/ 7/	t_{PD}		9, 10, 11	01		70	ns
				02		60	
				03		50	
Chip select inactive to high-Z 4/ 5/ 7/	t_{HZCS1}		9, 10, 11	01		35	ns
				02		30	
				03		25	
Chip select active to high-Z 4/ 6/ 7/	t_{HZCS2}		9, 10, 11	01		70	ns
				02		60	
				03		50	

1/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V, and the output load in figure 3, circuit A.

2/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

3/ For test purposes, not more than one output at a time may be shorted. Short circuit test duration should not exceed one second.

4/ Tested initially and after any design or process change which may affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

5/ Parameter applies to $\overline{CS}_2$, CS_3, and $\overline{CS}_4$.

6/ Parameter applies only to $\overline{CS}_1$.

7/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from 1.5 V level on the input and the output load in figure 3, circuit B.

Device types	01 - 03	
Case outlines	Y , Z	U
Terminal number	Terminal symbol	
1	A_9	A_9
2	A_8	A_8
3	A_7	A_7
4	A_6	A_6
5	A_5	A_5
6	A_4	A_4
7	A_3	A_3
8	A_2	A_2
9	A_1	A_1
10	A_0	A_0
11	O_0	NC
12	O_1	O_0
13	O_2	O_1
14	GND	O_2
15	O_3	NC
16	O_4	GND
17	O_5	O_3
18	O_6	NC
19	$\overline{O_7}$	O_4
20	CS_4	O_5
21	$\overline{CS_3}$	O_6
22	$\overline{CS_2}$	O_7
23	CS_1	$\overline{NC}$
24	A_{13}	CS_4
25	A_{12}	$\overline{CS_3}$
26	A_{11}	$\overline{CS_2}$
27	A_{10}	CS_1
28	V_{CC}	A_{13}
29	---	A_{12}
30	---	A_{11}
31	---	A_{10}
32	---	V_{CC}

NC = no connection

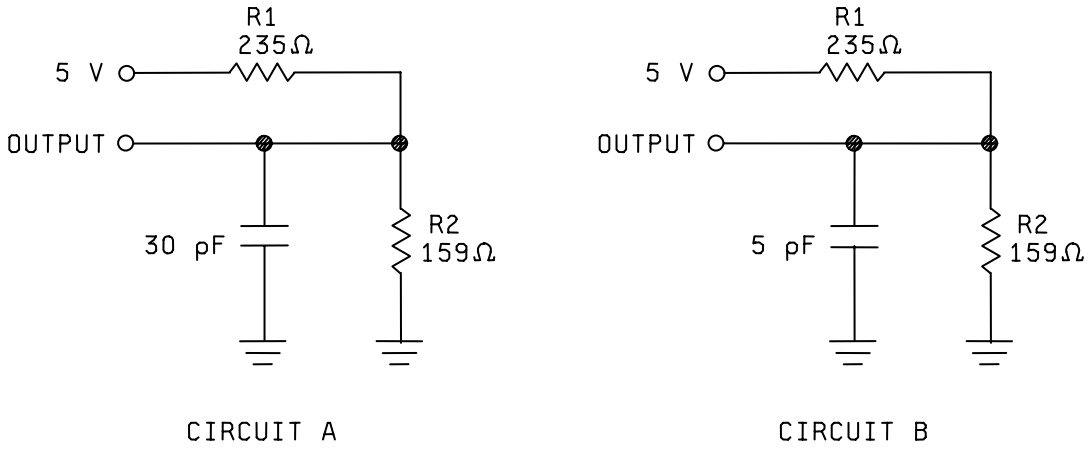
FIGURE 1. Terminal connections.

Mode	$\overline{CS}_4$	CS_3	$\overline{CS}_2$	$\overline{CS}_1$	A_{13} - A_0	Power	Outputs
Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	X	I_{CC}	D_{OUT}
Output disable	X	X	X	V_{IH}	X	I_{SB}	High Z
Output disable	X	X	V_{IH}	X	X	I_{CC}	High Z
Output disable	X	V_{IL}	X	X	X	I_{CC}	High Z
Output disable	V_{IH}	X	X	X	X	I_{CC}	High Z

1/ X can be either V_{IL} or V_{IH}.

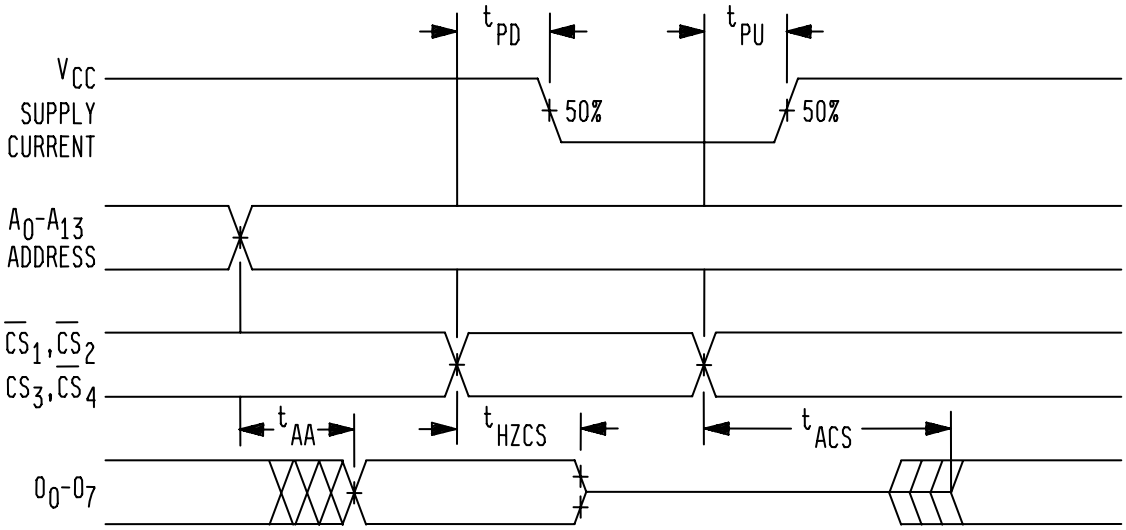
2/ For V_{PP} see 4.5.

FIGURE 2. Truth table.



Note: Including scope and jig capacitance.

FIGURE 3. Output load circuits.



Note: Power down controlled by $\overline{CS}_1$ only.

FIGURE 4. Switching waveforms.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or procuring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. All devices processed to an altered item drawing may be programmed either before or after burn-in at the discretion of the manufacturer. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial test and after any process or design changes which may affect input or output capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11. Either of two techniques is acceptable:

(1) Testing the entire lot using additional built-in test circuitry which allows the manufacturer to verify programmability and ac performance without programming the user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, and 11, group A testing in accordance with the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogrammed device, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

e. Subgroups 7 and 8 shall include verification of the pattern specified in 4.3.1d.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using an ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12000 $\mu W/cm^2$). Exposure of EPROMS to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (in accordance with 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8A, 8B
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8A, 8B, 9
Group A test requirements (method 5004)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Group C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ *Indicates PDA applies to subgroups 1 and 7.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ **See 4.3.1c.

4/ As a minimum, subgroups 7 and 8 shall consist of verifying the data pattern.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-02-10

Approved sources of supply for SMD 5962-89537 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8953701YA	0C7V7	CY7C251-65WMB
5962-8953701ZA	3/	CY7C251-65TMB
5962-8953701UA	0C7V7	CY7C251-65QMB
5962-8953702YA	0C7V7	CY7C251-55WMB
5962-8953702ZA	3/	CY7C251-55TMB
5962-8953702UA	0C7V7	CY7C251-55QMB
5962-8953703YA	0C7V7	CY7C251-45WMB
5962-8953703ZA	3/	CY7C251-45TMB
5962-8953703UA	0C7V7	CY7C251-45QMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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