REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add vendor CAGE 75569. Technical changes throughout. - mbk	92-02-10	M. A. Frye
B	Update the boilerplate to the current requirements of MIL-PRF-38535. - JAK	07-12-17	Thomas M. Hess
C	Correct test condition for total power supply current (I_{CC}) and add footnote 6/ in table I. Update boilerplate paragraphs to current MIL-PRF-38535 requirements. – MAA.	10-08-11	Thomas M. Hess

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Monica L. Poelking

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Monica L. Poelking

APPROVED BY
Wm J. Johnson

DRAWING APPROVAL DATE
90-03-13

REVISION LEVEL
C

MICROCIRCUIT, DIGITAL, FAST CMOS, 8-BIT LATCHED TRANSCEIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89730**

SHEET 1 OF 14

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89730	01	K	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54FCT543	8-bit octal latched transceiver, non-inverting, with three-state outputs, TTL compatible
02	54FCT543A	8-bit octal latched transceiver, non-inverting, with three-state outputs, TTL compatible

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDIP1-T24 or CDIP2-T24	24	Dual-in-line
L	GDFP1-F24 or CDFP2-F24	24	Flat pack
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
Output and I/O voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc 2/
DC input diode current (I_{IK})	–20 mA
DC output diode current (I_{OK})	–50 mA
DC output current	±100 mA
Maximum power dissipation (P_D)	500 mW 3/
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Output voltage range (V_{OUT})	0.0 V to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C

1/ All voltages are referenced to ground.
2/ For $V_{CC} \geq 6.5$ V dc, the upper bound is limited to V_{CC}.
3/ Must withstand the added P_D due to short circuit test, I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified 1/		Group A subgroups	Device types	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V V_{IH} = 2.0 V	I_{OH} = -300 µA	1, 2, 3	All	4.3		V
			I_{OH} = -12 mA			2.4		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V V_{IH} = 2.0 V	I_{OH} = 300 µA	1, 2, 3	All		0.2	V
			I_{OH} = 48 mA				0.55	
Input clamp voltage	V_{IK}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1	All		-1.2	V
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 5.5 V, (except I/O pins)		1, 2, 3	All		5.0	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V, (I/O pins only)		1, 2, 3	All		15.0	µA
Low level input current	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 5.5 V, (except I/O pins)		1, 2, 3	All		-5.0	µA
	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V, (I/O pins only)		1, 2, 3	All		-15.0	µA
Short circuit output current	I_{OS} 1/	V_{CC} = 4.5 V, V_{OUT} = GND		1, 2, 3	All	60		mA
Quiescent power supply current (CMOS inputs)	I_{CCQ}	$V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V V_{CC} = 5.5 V, $f_i = f_{CP}$ = 0 MHz		1, 2, 3	All		1.5	mA
Quiescent power supply current (TTL inputs)	ΔI_{CC} 2/	V_{CC} = 5.5 V V_{IN} = 3.4 V		1, 2, 3	All		1.5	mA
Dynamic power supply current	I_{CCD} 3/	V_{CC} = 5.5 V, $V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V Outputs open, One bit toggling, 50% duty cycle $\overline{CEAB}$ = $\overline{OEAB}$ = GND, $\overline{CEBA}$= V_{CC}		1, 2, 3	All		0.25	mA/ MHz
Total power supply current	I_{CC} 4/ 6/	V_{CC} = 5.5 V, f_{CP} = $\overline{LEAB}$ = 10 MHz Outputs open, 50% duty cycle One bit toggling at f_i = 5 MHz $\overline{CEAB}$ = $\overline{OEAB}$ = GND, $\overline{CEBA}$= V_{CC}	$V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V	1, 2, 3	All		4.0	mA
			V_{IN} =3.4 V or V_{IN} = GND	1, 2, 3	All		6.0	mA
		V_{CC} = 5.5 V, f_{CP} = $\overline{LEAB}$ = 10 MHz Outputs open, 50% duty cycle Eight bits toggling at f_i = 5 MHz $\overline{CEAB}$ = $\overline{OEAB}$ = GND, $\overline{CEBA}$= V_{CC}	$V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V	1, 2, 3	All		12.8 7/	mA
			V_{IN} =3.4 V or V_{IN} = GND	1, 2, 3	All		21.8 7/	mA

see footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Functional test		See 4.3.1d	7, 8	All			
Input capacitance	C_{IN}	See 4.3.1c	4	All		10	pF
I/O capacitance	$C_{I/O}$	See 4.3.1c	4	All		12	pF
Propagation delay time, transparent mode, An to Bn, Bn to An	t_{PHL1}, t_{PLH1} 5/	$R_L = 500\Omega$ $C_L = 50$ pF See figure 4	9, 10, 11	01	2.5	10.0	ns
				02	2.5	7.5	
Propagation delay time, $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn	t_{PHL2}, t_{PLH2}	$R_L = 500\Omega$ $C_L = 50$ pF See figure 4	9, 10, 11	01	2.5	14.0	ns
				02	2.5	9.0	
Output enable time, $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn, $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn	t_{PZH}, t_{PZL}	$R_L = 500\Omega$ $C_L = 50$ pF See figure 4	9, 10, 11	01	2.0	14.0	ns
				02	2.0	10.0	
Output disable time, $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn, $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn	t_{PHZ}, t_{PLZ}	$R_L = 500\Omega$ $C_L = 50$ pF See figure 4	9, 10, 11	01	2.0	13.0	ns
				02	2.0	8.5	
Setup time, An to $\overline{LEBA}$ to $\overline{LEAB}$, Bn to $\overline{LEBA}$ to $\overline{LEAB}$	t_s		9, 10, 11	01	3.0		ns
				02	2.0		
Hold time, An to $\overline{LEBA}$ to $\overline{LEAB}$, Bn to $\overline{LEBA}$ to $\overline{LEAB}$	t_h		9, 10, 11	01	2.0		ns
				02	2.0		
Pulse width $\overline{LEBA}$ to $\overline{LEAB}$	t_w		9, 10, 11	01	5.0		ns
				02	5.0		

1/ Not more than one output should be shorted at one time and the duration of the short circuit condition shall not exceed 1 second.

2/ TTL driven input, $V_{IN} = 3.4$ V, all other inputs at V_{CC} or GND.

3/ This parameter is not directly testable, but is derived for use in total power supply calculations.

4/ $I_{CC} = I_{CCQ} + (\Delta I_{CC} X D_H x N_T)+(I_{CCD} x f_i x N_i)$
Where: D_H = Duty cycle for TTL inputs high; N_T = Number of TTL inputs at D_H
f_i = Input frequency in MHz; N_i = Number of inputs at f_i

5/ The minimum limits for the propagation delay times are guaranteed, if not tested, to the limits specified in table I.

6/ For total current supply (I_{CCT}) test in an ATE environment, the effect of parasitic output capacitive loading from the test environment must be taken into account, as its effect is not intended to be included in the test results. The impact must be characterized and appropriate offset factors must be applied to the test result.

7/ These limits are guaranteed but not tested.

Device type	01 and 02	
Case outline	K and L	3
Terminal number	Terminal symbol	Terminal symbol
1	$\overline{\text{LEBA}}$	NC
2	$\overline{\text{OEBA}}$	$\overline{\text{LEBA}}$
3	A0	$\overline{\text{OEBA}}$
4	A1	A0
5	A2	A1
6	A3	A2
7	A4	A3
8	A5	NC
9	A6	A4
10	A7	A5
11	$\overline{\text{CEAB}}$	A6
12	GND	A7
13	$\overline{\text{OEAB}}$	$\overline{\text{CEAB}}$
14	$\overline{\text{LEAB}}$	GND
15	B7	NC
16	B6	$\overline{\text{OEAB}}$
17	B5	$\overline{\text{LEAB}}$
18	B4	B7
19	B3	B6
20	B2	B5
21	B1	B4
22	B0	NC
23	$\overline{\text{CEBA}}$	B3
24	V_{CC}	B2
25	- - -	B1
26	- - -	B0
27	- - -	$\overline{\text{CEBA}}$
28	- - -	V_{CC}

Terminal symbol	Terminal description
$\overline{\text{OEAB}}$	A-to-B output enable input (active low)
$\overline{\text{OEBA}}$	B-to-A output enable input (active low)
$\overline{\text{CEAB}}$	A-to-B enable input (active low)
$\overline{\text{CEBA}}$	B-to-A enable input (active low)
$\overline{\text{LEAB}}$	A-to-B latch enable input (active low)
$\overline{\text{LEBA}}$	B-to-A latch enable input (active low)
A0 - A7	A-to-B data inputs to B-to-A three-state outputs
B0 - B7	B-to-A data inputs to A-to-B three-state outputs

FIGURE 1. Terminal connections.

Inputs			Latch status	Output buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A to B	B0 - B7
H	X	X	Storing	High Z
X	H	-	Storing	-
X	-	H	-	High Z
L	L	L	Transparent	Current A inputs
L	H	L	Storing	*Previous A inputs

H = High voltage level
L = Low voltage level
X = Irrelevant
* = Before $\overline{LEAB}$ low-to-high transition.
A-to-B data flow shown: B-to-A flow control is the same except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

FIGURE 2. Truth table.

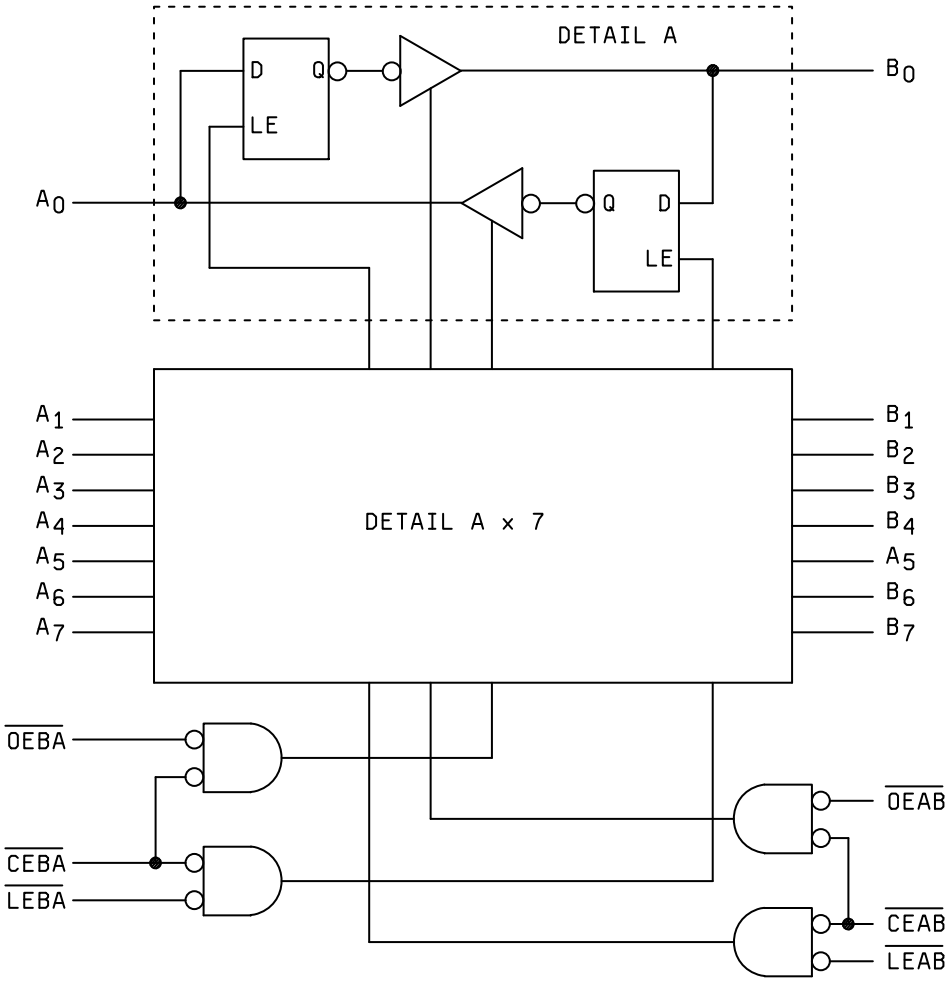


FIGURE 3. Logic diagram.

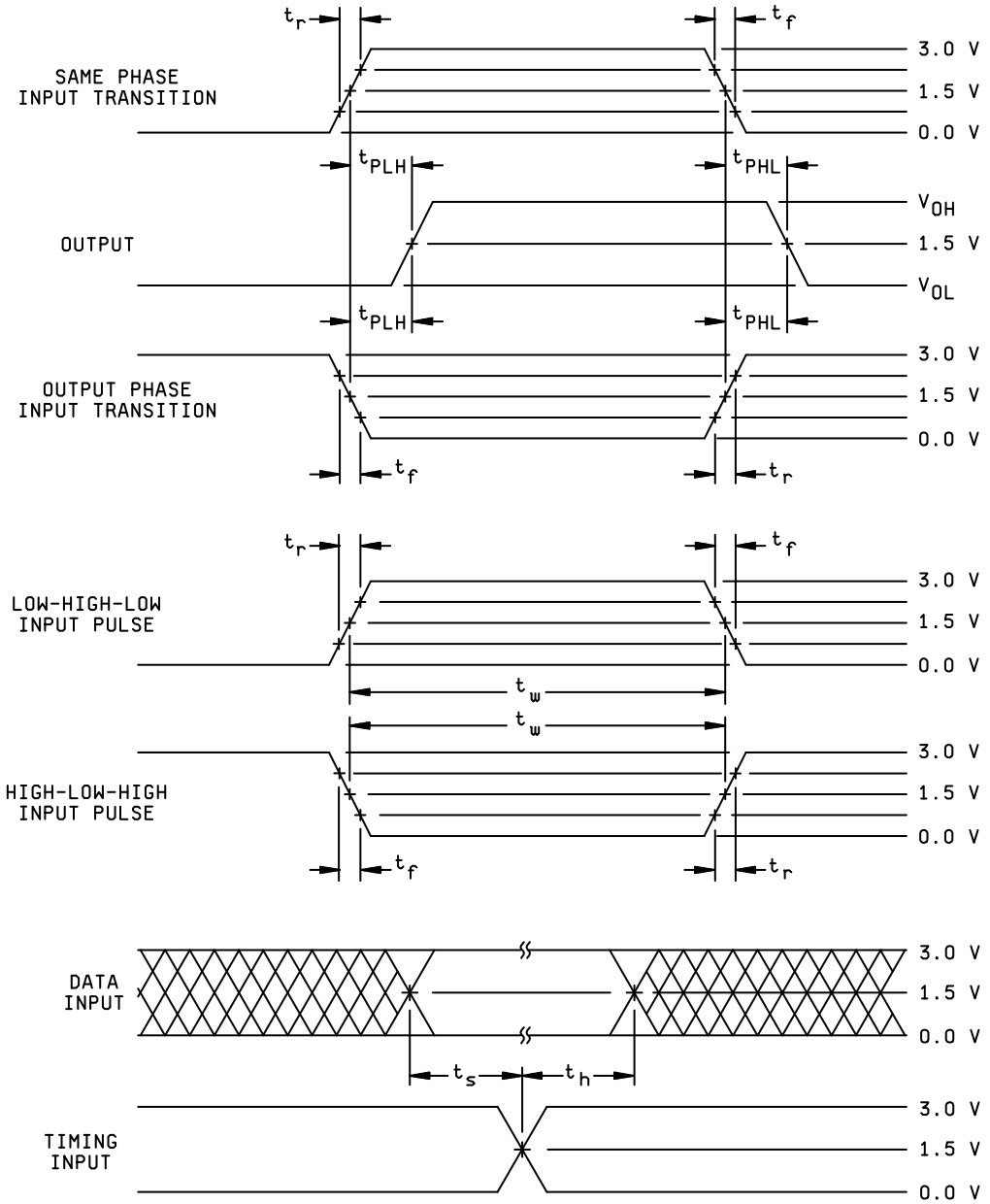


FIGURE 4. Test circuit and switching waveforms.

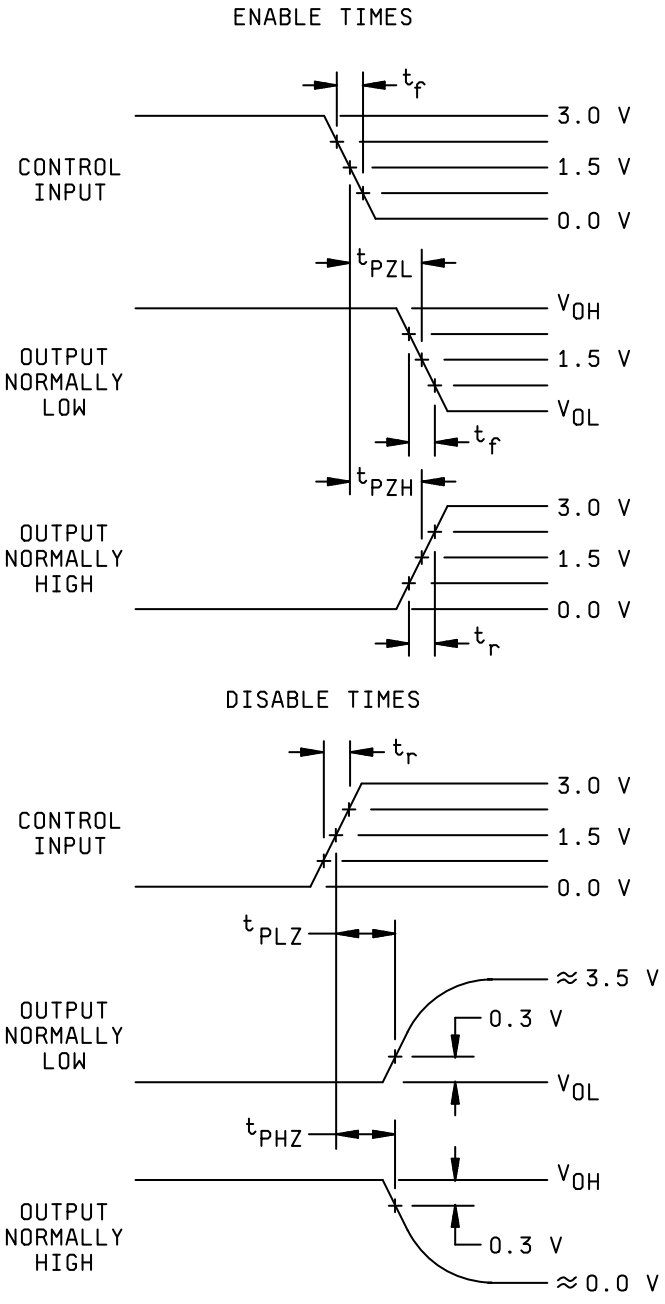
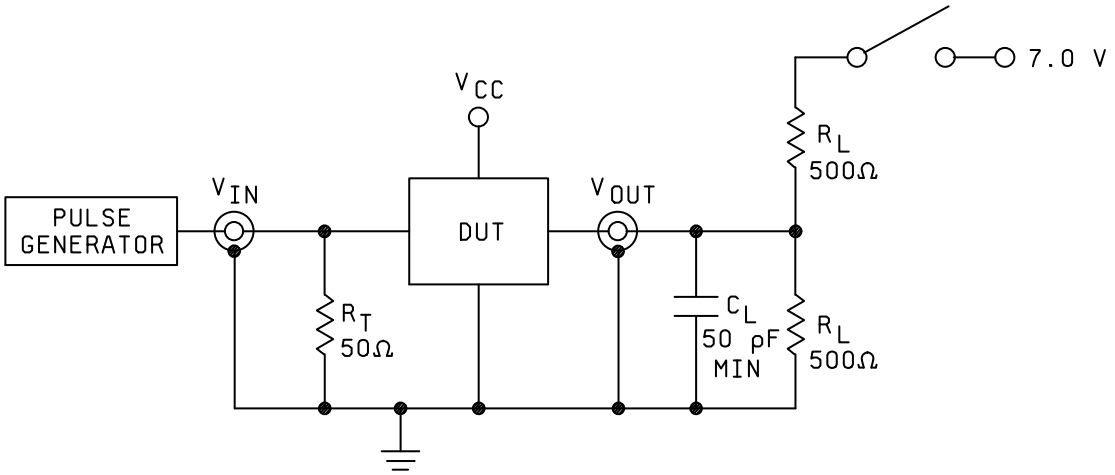


FIGURE 4. Test circuit and switching waveforms - Continued.



Test	Switch
t_{PLZ}	Closed
t_{PZL}	Closed
Open drain	Closed
All other	Open

1. C_L includes probe and jig capacitance.
2. R_T = termination resistance and should be equal to Z_{OUT} of the pulse generator.
3. $t_r = t_f = 2.5$ ns (10% to 90%), unless otherwise specified.

FIGURE 4. Test circuit and switching waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Test all applicable pins on 5 devices with zero failures.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-08-11

Approved sources of supply for SMD 5962-89730 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-89730013A	0C7V7	IDT54FCT543LB
5962-8973001KA	0C7V7	IDT54FCT543EB
5962-8973001LA	0C7V7	IDT54FCT543DB
5962-89730023A	0C7V7	IDT54FCT543ALB
5962-8973002KA	0C7V7	IDT54FCT543AEB
5962-8973002LA	0C7V7	IDT54FCT543ADB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Bus Transceivers ***category:***

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Other Similar products are found below :

74LS645N DS8838 FXL4TD245UMX IDT74CBTLV3257PGG 74LVT245BBT20-13 5962-8683401DA PCA9617ADMR2G 5962-8953501KA 5962-86834012A 5962-7802301Q2A 5962-7802002MFA 5962-7802001MFA 74VHCV245FT(BJ) NCV7349D13R2G TC74VCX164245(EL,F MC74LCX245MNTWG TC7WPB8306L8X,LF(S TC7WPB9307FC(TE85L 74FCT16245CTPVG8 74FCT16543CTPVG 74FCT245CTPYG8 MM74HC245AMTCX 74LVCH16245APVG 74LVX245MTC 5962-9221405M2A NTS0102DP-Q100H 74ALVC16245MTDX 74ALVCH32245BF 74FCT163245APVG 74FCT245ATPYG8 74FCT245CTQG 74FCT3245AQG 74LCXR162245MTX 74VHC245M 74VHC245MX TC7WPB9306FC(TE85L TC7WPB9306FK(T5L,F JM38510/65553BRA ST3384EBDR 74LVC1T45GF,132 74AVC4TD245BQ,115 PQJ7980AHN/C0JL,51 MC100EP16VBDG FXL2TD245L10X 74LVC1T45GM,115 TC74AC245P(F) PSB21150F S LLHR SNJ54LS245FK SNJ54AHC245J SNJ54ABT245AFK