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1. SCOPE 1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A. 1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example: 5962-89863 01 Device type Case outline Lead finish Drawing number (see 1.2.1) (see 1.2.2) (see 1.2.3) 1.2.1 Device type(s). The device type(s) identify the circuit function as follows: Generic number 1/ Circuit function Acess time Device type 80 ns 01 512 X 9 FIFO 02 512 X 9 FIFO 65 ns 03 512 X 9 FIFO 50 ns 04 40 ns 512 X 9 FIFO 05 512 X 9 FIFO 30 ns 06 512 X 9 FIFO 25 ns 1.2.2 <u>Case outline(s)</u>. The case outline(s) are as designated in MIL-STD-1835 and as follows: Outline letter Terminals Package style Descriptive designator Х GDIP1-T28 or CDIP2-T28 28 dual-in-line package Y CDIP3-T28 or GDIP4-T28 28 dual-in-line package Ζ CQCC1-N32 32 rectangular chip carrier package U GDFP2-F28 28 flat package 1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A. 1.3 Absolute maximum ratings. Supply voltage to ground potential ------0.5 V dc to +7.0 V dc DC voltage applied to outputs in high Z state -----DC input voltage ------DC output current ------0.5 V dc to +7.0 V dc -0.3 V dc to +7.0 V dc 20 mA Maximum power dissipation 2/ -----1.0 W Lead temperature (soldering, 10 seconds) -----+260°C See MIL-STD-1835 +150°C -65°C to +150°C -55°C to +125°C 1.4 <u>Recommended operating conditions</u>. Supply voltage (V_{CC})------Ground voltage (GND) -----+4.5 V dc to +5.5 V dc 0 V dc 2.2 V dc minimum 0.8 V dc maximum Case operating temperature range (T_c) ------55°C to +125°C Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and 1/ will also be listed in MIL-HDBK-103. Must withstand the added P_D due to short circuit test (e.g., I_{OS}). 2/ 3/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life. SIZE STANDARD 5962-89863 Α MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS **REVISION LEVEL** SHEET COLUMBUS, OHIO 43218-3990 2 Α

2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits. MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings. MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <u>http://assist.daps.dla.mil/quicksearch/</u> or <u>http://assist.daps.dla.mil</u> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 <u>Item requirements</u>. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 1.

3.2.2 <u>Truth table</u>. The truth table shall be as specified on figure 2.

3.2.3 <u>Case outlines</u>. The case outlines shall be in accordance with 1.2.2 herein.

3.2.4 <u>Die overcoat</u>. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-89863
DEFENSE SUPPLY CENTER COLUMBUS		REVISION LEVEL	SHEET
COLUMBUS, OHIO 43218-3990		A	3

		Conditions <u>1</u> /	Group A	Device	Lim	its	
Test	Symbol	$\begin{array}{c} -55^\circ C \leq T_A \leq +125^\circ C \\ 4.5 \ V \leq V_{CC} \leq 5.5 \ V \\ \text{unless otherwise specified} \end{array}$	subgroups	type	Min	Max	Unit
Output high voltage	V _{OH}	$\begin{array}{l} V_{CC}=4.5 \ V, \ I_{OH}=-2.0 \ mA \\ V_{IN}=V_{IH}, \ V_{IL} \end{array}$	1, 2, 3	All	2.4		V
Output low voltage	V _{OL}	$\begin{array}{l} V_{CC}=4.5 \ V, \ I_{OH}=8.0 \ mA \\ V_{IN}=V_{IH}, \ V_{IL} \end{array}$	1, 2, 3	All		0.4	V
Input high voltage	V _{IH} <u>2</u> /		1, 2, 3	All	2.2		V
Input low voltage	V _{IL} <u>2</u> /		1, 2, 3	All		0.8	V
Input leakage current	I _{IX}	V _{IN} = 5.5 V to GND	1, 2, 3	All	-10	+10	μA
Output leakage current	I _{OZ}	$V_{CC} = 5.5 V,$ $V_{OUT} = 5.5 V$ to GND	1, 2, 3	All	-10	+10	μA
Operating supply current	I _{CC1}	$V_{CC} = 5.5 \text{ V}, I_{OUT} = 0 \text{ mA}$ f = 1/t _{RC}	1, 2, 3	01, 02		115	mA
		\overline{W} , \overline{R} , D_0 - D_8 pins are toggling between 0 V and 3 V		03 04, 05		130 140	
		$\overrightarrow{FF}, \ \overrightarrow{XO} / \ \overrightarrow{HF} = 0 \text{ mA}$ $Q_0 - Q_8 = 0 \text{ mA}$ $\overrightarrow{MR}, \ \overrightarrow{FL} / \overrightarrow{RT} = 3.0 \text{ V}$		06		147	
Standby current	I _{CC2}	$\label{eq:V_CC} \begin{array}{l} V_{CC} = 5.5 \ V, \ I_{OUT} = 0 \ mA \\ \mbox{All inputs} = V_{IH} \\ \hline FF \ , \ \overline{XO} \ / \ \overline{HF} = 0 \ mA \\ \mbox{Q}_0 \ - \ \mbox{Q}_8 = 0 \ mA \end{array}$	1, 2, 3	All		30	mA
Power down current	I _{CC3}	$\begin{array}{l} V_{CC}=5.5 \text{ V}, \ I_{OUT}=0 \text{ mA} \\ \text{All inputs}=V_{CC} \text{ -}0.2 \text{ V} \\ \overline{FF}, \ \overline{XO} \text{ / } \overline{HF}=0 \text{ mA} \\ Q_0 \text{ - } Q_8=0 \text{ mA} \end{array}$	1, 2, 3	All		25	mA
Input capacitance	C _{IN} <u>3</u> /	$V_{CC} = 5.0 V$ $T_A = +25^{\circ}C, f = 1 MHz$ See 4.3.1c	4	All		8	pF
Output capacitance	С _{оит} <u>3</u> /	$V_{CC} = 5.0 V$ $T_A = +25^{\circ}C, f = 1 MHz$ See 4.3.1c	4	All		8	pF
Functional tests		See 4.3.1d	7,8	All			

TABLE I Electrical performance characteristics

STANDARD **MICROCIRCUIT DRAWING** DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990

SIZE A		5962-89863
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	TABL	E I. <u>Electrical performance chara</u>	<u>cteristics</u> - Co	ontinued.			
Test		Conditions <u>1</u> /	Group A	Device	Limits		Unit
	Symbol	$\begin{array}{l} -55^\circ C \leq T_A \leq +125^\circ C \\ 4.5 \ V \leq V_{CC} \leq 5.5 \ V \\ \text{unless otherwise specified} \end{array}$	subgroups	type	Min	Max	
			1	01	100		
Read cycle time	t _{RC}	See figure 3	9, 10, 11	02	80		ns
,	110	3	-, -,	03	65		-
				04	50		
				05	40		
		-		06	35		
				01		80	
Access time	t _A		9, 10, 11	02		65	ns
				03		50	
				04 05		40 30	
				05		30 25	
		1		00	20	20	
Read recovery time	t		9, 10, 11	02, 03	15		ns
Read recovery line	t _{RR}		9, 10, 11	04,05,06	10		115
		7		01	80		
Read pulse width	t _{PR}		9, 10, 11	02	65		ns
			-, -,	03	50		_
				04	40		
				05	30		
		_		06	25		
Read low to low Z	t _{LZR} <u>3/4</u> /		9, 10, 11	All	3		ns
Read high to data valid	t _{DVR}		9, 10, 11	All	3		ns
				01,02,03		30	
Read high to high Z	t _{HZR} <u>3</u> / <u>4</u> /		9, 10, 11	04		25	ns
	412K <u></u>		-,,	05		20	
				06		18	
				01	100		
Write cycle time	t _{WC}		9, 10, 11	02	80		ns
				03	65		
				04	50		
				05	40		
	1	4	}	06	35	<u> </u>	-
	1.		0 40 44	01	80		
Write pulse width	t _{PW}		9, 10, 11	02	65 50	1	ns
				<u>03</u> 04	50 40		
				05 06	30 25		
See footnotes at end of	table.						
MICRO	STANDARD CIRCUIT DR	AWING	ZE A			596	2-8986
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COLUMBUS, OHIO 43218-3990

Symbol t _{HWZ} <u>3/ 4/</u> t _{WR}	Conditions $\underline{1}/$ -55°C \leq T _A \leq +125°C 4.5 V \leq V _{CC} \leq 5.5 V unless otherwise specified See figure 3	Group A subgroups 9, 10, 11	Device type All 01	Limits Min 10	Max	Unit
	See figure 3					ns
t _{WR}			01	20		
t _{WR}				20		
		9, 10, 11	02.03	15		ns
			04.05.06	10		
			01	40		
t _{SD}		9, 10, 11	02.03	30		ns
			04	20		
1		0 10 11				
τ _{HD}		9, 10, 11				ns
+		0 10 11				ne
^I MRSC		9, 10, 11				ns
			01	80		
tome		9, 10, 11	02	65		ns
		-, -,	03	50		_
			04	40		4
			05	30		
			06			
t _{RMR}		9, 10, 11				ns
t _{RPW} <u>3</u> /		9, 10, 11				ns
						20
t _{WPW} <u>3</u> /		9, 10, 11				ns
			04	40		
				30		
			05	.30		
	t _{HD} t _{MRSC} t _{PMR} t _{RMR} t _{RPW} <u>3</u> /	t _{MRSC} t _{PMR} t _{RMR} t _{RPW} <u>3</u> /	t _{MRSC} 9, 10, 11 t _{PMR} 9, 10, 11 t _{RMR} 9, 10, 11 t _{RMR} 9, 10, 11 t _{RPW} <u>3</u> / 9, 10, 11	Image: height descent for the sector descent	Image: here in the image: he	the 0.5 1.8 0.06 1.5 0.06 the 0.1.02 1.0 0.0<

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TABLE L. Electrical performance characteristics - Continued.

DSCC FORM 2234 APR 97

MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43218-3990

Test Symbol Conditions (j) -55°C ≤ T_A ±12°C A 5V Voc ≤ 5.5 V unless otherwise specified Group A subgroups Device type Limits Unit Retransmit cycle time bcrc See figure 3 9, 10, 11 0.2 80 ns Retransmit pulse bcrc See figure 3 9, 10, 11 0.2 80 ns Retransmit pulse bcrc See figure 3 9, 10, 11 0.2 80 ns Retransmit pulse bcrc See figure 3 9, 10, 11 0.2 80 ns Master reset to empty tig tsit. 10 10 0.0 ns ns Master reset to half-full flag high tsit. 0, 10, 11 0.2 80 ns Master reset to full flag high tsit. 0, 10, 11 0.2 0.6 0.6 0.6 Master reset to full flag high tsit. 0, 10, 11 0.2 0.0 11 0.0 ns Master reset to full flag high tsit. 0, 10, 11 0.2 0.0 0.6 0.6 0.6 </th <th></th> <th>IAB</th> <th>LE I. Electrical performan</th> <th>ce characteristics</th> <th>- Contir</th> <th>nued.</th> <th></th> <th></th> <th></th>		IAB	LE I. Electrical performan	ce characteristics	- Contir	nued.			
Image: control	Test	Symbol	-55°C ≤ T _A ≤+125°	C subgro					Unit
Retransmit cycle time terro See figure 3 9, 10, 11 01 100 ns Retransmit pulse teer see 9, 10, 11 02 80 ns Retransmit pulse teer teer 9, 10, 11 02 80 ns Retransmit pulse teer teer ns ns ns ns Retransmit recovery time terr terr 01 20 66 ns Master reset to empty fing low terr terr 01 100 ns ns Master reset to hull full flag high terr terr ns ns ns Master reset to hull full flag high terr terr ns ns ns 9, 10, 11 02 80 ns ns ns Master reset to hull flag high terr ns ns ns 9, 10, 11 02 80 ns ns 03 65 40 ns ns ns							Min	Max	
Retransmit cycle time tsrc See figure 3 9, 10, 11 02 80 ns Retransmit cycle time torr see figure 3 9, 10, 11 02 80 ns Retransmit pulse torr torr 9, 10, 11 02 86 ns Retransmit recovery torr torr 9, 10, 11 02 86 ns Master reset to empty torr torr 9, 10, 11 02 80 ns Master reset to half-full flag high torr torr 01 02 80 ns Master reset to full treft torr 03 65 04 06 35 Master reset to full treft flag low torr 03 65 04 65 Master reset to full treft flag low torr 01 100 03 65 04 06 35 04 65 04 06 35 04 05 30 05 04 05			uniess otherwise sp	ecified		01	100		
Retransmit pulse tree See figure 3					⊢				
Standard Length 3 Odd Standard Retransmit pulse terr 0	Retransmit cycle time	t _{RTC}		9, 10	, 11 –				ns
Retransmit pulse tret Retransmit pulse tret 9, 10, 11 0.5 4.0 0.1 8.0 ns 0.2 6.5 1.0 0.3 5.0 0.0 0.4 4.0 0.2 0.5 4.0 0.2 0.6 2.5 0.1 0.6 2.5 0.1 0.6 2.5 0.1 0.1 2.0 1.5 ns Master reset to half- full flag high tern 0.1 100 0.0 9, 10, 11 0.2 8.0 ns 0.6 3.5 Master reset to hull flag high tern 0.1 100 0.2 8.0 ns 9, 10, 11 0.2 8.0 ns 0.6 3.5 0.0 Master reset to hull flag high tern 0.1 100 0.2 8.0 ns 9, 10, 11 0.2 8.0 ns 0.6 3.5 0.0			See figure 3						
Retransmit pulse width treft 06 35 1 Retransmit pulse width treft 9, 10, 11 02 65 03 Retransmit recovery time tarra 0 0.3 6.0 0.0 9, 10, 11 02 0.0 5.0 0.0 0.0 0.0 Master reset to empty flag low tarra 0 0.1 2.0 1 1.0 0.0 Master reset to half- full flag high tarra 0.1 1.00 0.3 6.6 0.6 3.6 Master reset to full flag high tarra 0.1 1.00 0.3 6.6 0.6 3.6 Master reset to full flag high tarra 0.1 1.00 0.3 6.6 0.6 3.5 0 0.6 3.5 0 0.6 3.5 0 0.6 0.6 3.5 0 0.6 3.5 0 0 0.6 3.5 0 0.6 3.5 0 0 0.6 3.5 0 0 0.									
Retransmit pulse width text 9, 10, 11 02 65 ns Retransmit recovery time tern 9, 10, 11 02,03 15 ns Master reset to empty flag low terL 9, 10, 11 02,03 15 ns Master reset to half- full flag high terH 01 100 ns ns Master reset to half- full flag high terH 01,011 02,03 15 ns Master reset to half- full flag high terH 01,011 03 66 36 Master reset to full flag high terH terH 9, 10, 11 02 80 ns 9, 10, 11 02 80 ns 01 100 03 66 04 50 04 50 04 50 04 50 04, 05, 06 15 ns 01 100 03 66 36 04, 05, 06 04 50 06 36 06 36 06 36 06 36 <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>									
No. 11 03 50 04 Retransmit recovery twrn 01 20 04 00 04 00 04 00 04 00 04 00 04 00 04 00 04 00 04 04 00 04 04 04 00 04 0						01	80		
width 03 50 Retransmit recovery time tern 01 20 Master reset to empty tlag low terL 9, 10, 11 02,03 15 Master reset to half- full flag high 01 100 02,03 15 Master reset to half- full flag high terH 9, 10, 11 02,03 66 Master reset to full flag high terH 9, 10, 11 03 66 04 50 01 100 03 66 04 50 01 100 03 66 04 50 01 100 03 66 04 9, 10, 11 03 66 04 50 06 04 50 04 50 06 35 04 50 06 04 50 05 40 01 100 03 66 06 35 06 06 35 06 06 35 06 06 06 35	Retransmit pulse	topт		9, 10	. 11				ns
Betransmit recovery term 06 26 07 Master reset to empty flag low tert. 9, 10, 11 02 80 ns Master reset to half- full flag high tert. 01 100 9, 10, 11 02 80 ns Master reset to half- full flag high tert. 01 100 03 65 04 Master reset to half- full flag high tert. 01 100 03 65 04 9, 10, 11 02 80 ns 03 65 04 06 35 04 06 35 04 06 35 04 06 35 04 06 35 04 06 35 04 06 35 04 06 35 04 06 35 04 06 35 04 06 35 05 04 06 35 05 04 06 35 04 06 35 05 04 06 35 </td <td></td> <td>TIN</td> <td></td> <td>-,</td> <td>,</td> <td></td> <td></td> <td></td> <td></td>		TIN		-,	,				
Retransmit recovery trrR ime 01 20 Master reset to empty tert. 01 000 flag low tert. 01 000 02 03 65 Master reset to half-full flag high tert. 01 000 03 65 04 65 04 65 04 65 04 65 04 66 35 04 56 04 56 04 56 04 56 04 56 04 56 04 56 04 56 04 56 04 56 04 56 04 56 04 56 04 56 04 56 04 56 04 56 04 56 04 06 35 04 56 04 06 35 04 56 04 06 35 04 06 35 04 06 35 03 06 25 04 35 <									
Retransmit recovery time tarra 01 20 315 ns Master reset to empty flag low ter. 01 100 02 80 ns Master reset to half-full flag high ter. 01 100 02 80 ns Master reset to half-full flag high ter. 01 100 03 65 04 56 04 56 04 56 04 56 04 56 04 56 04 56 04 50 05 40 06 35 01 100 03 65 40 06 35 01 100 03 65 40 06 35 05 40 06 35 05 40 06 35 05 40 06 35 05 40 06 35 05 40 06 35 05 05 40 06 35 05 05 40 06 35 05 30					-				
Retransmit recovery time term ns ns ns Master reset to empty flag low terL 9, 10, 11 02,03,-15 ns Master reset to half-full flag high terH 9, 10, 11 01 100 Master reset to half-full flag high terH 9, 10, 11 02 80 ns Master reset to half-full flag high terH 9, 10, 11 02 80 ns Master reset to full flag high terH 9, 10, 11 02 80 ns Master reset to full flag high terH 9, 10, 11 02 80 ns 9, 10, 11 03 65 40 06 35 04 50 04 50 06 35 04 50 06 35 04 50 04 50 06 35 06 25 Read low to empty terF 9, 10, 11 03 45 ns 9, 10, 11 03 45 ns 06 25			4						
No. 10. 11 04.05.06 10 Master reset to empty flag low terL 9, 10, 11 01 100 Master reset to half- full flag high turne 9, 10, 11 02 80 ns Master reset to half- full flag high turne 9, 10, 11 03 65 40 Master reset to full flag high turne 9, 10, 11 02 80 ns Master reset to full flag high term 9, 10, 11 02 80 ns 9, 10, 11 02 80 ns 06 35 04 9, 10, 11 02 80 ns 06 35 04 9, 10, 11 02 80 ns 06 35 04 9, 10, 11 02 80 ns 05 30 05 30 06 25 30 05 30 05 30 06 25 10 11 03 45 ns 05 30 06 25					-				
Master reset to empty flag low t _{EFL} 01 100 02 80 ns Master reset to half- full flag high t _{HPH} 03 65 04 50 Master reset to half- full flag high t _{HPH} 01 100 03 65 Master reset to full flag high t _{HPH} 03 65 04 50 Master reset to full flag high t _{FFH} 01 100 03 65 Master reset to full flag high t _{FFH} 01 02 80 ns 9, 10, 11 02 80 ns 06 35 04 50 04 550 04 50 04 50 04 50 05 40 06 35 ns 06 35 ns 10.02 60 06 35 ns 06 25 Read low to empty flag low t _{RFF} 9, 10, 11 03 45 ns 05 30 06 25 3		t _{RTR}		9, 10	, 11 –				ns
Master reset to empty flag low terL 9, 10, 11 02 80 ns Master reset to half- full flag high t _{HPH} 9, 10, 11 03 65 40 Master reset to half- full flag high t _{HPH} 9, 10, 11 02 80 ns Master reset to full flag high t _{HPH} 9, 10, 11 02 80 ns Master reset to full flag high t _{FFH} 9, 10, 11 02 80 ns Master reset to full flag high t _{FFH} 9, 10, 11 02 80 ns Read low to empty flag low t _{REF} 01 100 03 65 Read high to full flag high t _{REF} 9, 10, 11 03 45 ns StanDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS SIZE A 5962-89863 SHET						01		100	
Master reset to half- full flag high t _{HPH} 03 65 04 50 Master reset to half- full flag high t _{HPH} 9, 10, 11 03 65 01 100 Master reset to half- full flag high t _{HPH} 9, 10, 11 02 80 ns Master reset to full flag high t _{FFH} 9, 10, 11 03 65 40 06 35 04 50 05 40 06 35 Master reset to full flag high t _{FFH} 9, 10, 11 03 65 04 50 9, 10, 11 03 65 04 50 05 40 06 35 Read low to empty flag low t _{REF} 9, 10, 11 03 45 ns 06 25 05 30 06 25 05 30 06 25 05 30 06 25 05 30 06 25 05 30 06 25 05 30 06 25 06 2	Master reset to emoty	tee		a 10	11 L				ns
Master reset to half- full flag high tuffH 01 100 ns Master reset to half- full flag high tuffH 9, 10, 11 02 80 ns Master reset to full flag high trefH 9, 10, 11 02 80 ns Master reset to full flag high trefH 9, 10, 11 02 80 ns 9, 10, 11 02 80 ns 01 100 ns Read low to empty flag low trefF 9, 10, 11 03 65 40 06 35 0 0 0 100 ns Read low to empty flag low trefF 9, 10, 11 03 45 ns 06 25 30 06 25 06 25 StanDarD Microcircuit prawing DEFENSE supply centre columbus SiZE A 5962-89863 ShEET		4EFL		3, 10	,	03		65	
Master reset to half- full flag high tures 06 35 Master reset to full flag high term 9, 10, 11 02 80 ns Master reset to full flag high term 01 100 03 65 04 50 40 06 35 06 36 Master reset to full flag high term 01 100 03 65 04 50 06 35 04 50 05 Read low to empty flag low term 01.02 60 06 35 9, 10, 11 03 45 ns 06 25 06 04 35 30 06 25 06 25 06 9, 10, 11 03 45 ns 05 30 06 25 06 25 06 25 06 25 06 25 06 25 06 25 30 06 25 30 06 25 30	hag low				_	04		50	
Master reset to half- full flag high t _{HFH} 01 100 ns Master reset to full flag high t _{FFH} 9, 10, 11 02 80 ns Master reset to full flag high t _{FFH} 9, 10, 11 02 80 ns Master reset to full flag high t _{FFH} 9, 10, 11 02 80 ns Read low to empty flag low t _{REF} 9, 10, 11 03 45 ns Read high to full flag high t _{REF} 9, 10, 11 03 45 ns Standard t _{REF} 9, 10, 11 03 45 ns 06 25 30 06 25 06 06 25 30 06 25 06 06 25 30 06 25 06 25 See footnotes at end of table. SIZE 5962-89863 SP62-89863 DEFENSE SUPPLY CENTER COLUMBUS REVISION LEVEL SHEET									
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STANDARD A 5962-89863 MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS REVISION LEVEL SHEET	See footnotes at end of ta	able.							
DEFENSE SUPPLY CENTER COLUMBUS REVISION LEVEL SHEET								596	2-89863
	DEFENSE SUP	PLY CENTE	ER COLUMBUS		REVIS			SHEET	7

TABLE I. Electrical performance characteristics - Continued.

$-55^{\circ}C \le T_A \le +125^{\circ}C$ $4.5 \text{ V} \le V_{CC} \le 5.5 \text{ V}$ unless otherwise specified See figure 3	subgroups 9, 10, 11	type 01.02 03 04 05 06	Min	Max 60 45 35 30	ns
See figure 3	9, 10, 11	03 04 05		45 35	ns
See figure 3	9, 10, 11	04 05		35	ns
		05			
-				20	
		06			
				25	
		01.02		60	
	9, 10, 11	03		45	ns
		04		35	
4					
	0 10 11				~~
	9, 10, 11				ns
			1		
1					
	9, 10, 11	02		80	ns
	0, 10, 11	03		65	110
		04		50	
		05		40	
		06		35	
		01.02		60	
	9, 10, 11	03		45	ns
					-
4				25	
	9, 10, 11				ns
1			20	60	
	0 10 11				nc
	9, 10, 11				ns
J		06		25	
		01	80		
	9, 10, 11	02	65		ns
1		03	50		-
			-		
		04	40		
		04 05 06	40 30 25		
		9, 10, 11 9, 10, 11	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$

TABLE I. Electrical performance characteristics - Continued.

		Conditions <u>1</u> /	Group A	Device	Limits	1	Unit
Test	Symbol	$\begin{array}{l} -55^\circ C \leq T_A \leq +125^\circ C \\ 4.5 \ V \leq V_{CC} \leq 5.5 \ V \\ \text{unless otherwise specified} \end{array}$	subgroups	type	Min	Max	
Expansion out low	t _{XOL}		9, 10, 11	01		80	
delay from clock		See figure 3		02		65	ns
				03		50	
				04		40	
				05		30	
				06		25	
Expansion out high	t _{XOH}]	9, 10, 11	01		80	
delay from clock				02		65	ns
				03		50	
				04		40	
				05		30	1
				06		25	

TABLE I. Electrical performance characteristics - Continued.

1/ AC tests are performed with input rise and fall times of 5ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V, and the output load on figure 4.

- 2/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- 3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table1.
- <u>4</u>/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input.

3.5 <u>Marking</u>. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 <u>Certification/compliance mark</u>. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 <u>Notification of change</u>. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 <u>Verification and review</u>. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-89863
DEFENSE SUPPLY CENTER COLUMBUS		REVISION LEVEL	SHEET
COLUMBUS, OHIO 43218-3990		A	9

Device types	A	II
Case outlines	U, X, Y	Z
Terminal number	Tern sym	ninal nbol
1 2 3 4 5	W D ⁸ D ³ D ² D ¹	$\begin{array}{c} NC \\ \hline W \\ D_8 \\ D_3 \\ D_2 \end{array}$
6 7 8 9 10	D ₀ X FF Q ₀ Q ₁	$\begin{array}{c} D_1 \\ D_0 \\ \overline{XI} \\ \overline{FF} \\ Q_0 \end{array}$
11 12 13 14 15	Q ² Q ³ G R R	$\begin{array}{c} Q_1 \\ NC \\ Q_2 \\ Q_3 \\ Q_8 \end{array}$
16 17 18 19 20	$\begin{array}{c} Q_4 \\ Q_5 \\ Q_6 \\ Q_7 \\ \overline{XO}/\overline{HF} \end{array}$	$\begin{array}{c} \text{GND} \\ \text{NC} \\ \overline{\text{R}} \\ \text{Q}_4 \\ \text{Q}_5 \end{array}$
21 22 23 24 25		$\begin{array}{c} Q_6\\ Q_7\\ XO/HF\\ \overline{EF}\\ MR \end{array}$
26 27 28 29 30	D5 D4 V _{CC}	$\overline{FL/RT}$ NC D ₇ D ₆ D ₅
31 32	-	D ₄ V _{CC}

FIGURE 1. Terminal connections.

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COLUMBUS, OHIO 43218-3990		A	10

Reset and retransmit Single device configuration/width expansion mode

	Inputs		Internal status		Outputs			
Mode	MR	RT	XI	Read pointer	Write pointer	EF	FF	F
Reset Retransmit Read/Write	0 1 1	X 0 1	0 0 0	Location zero Location zero Increment <u>1</u> /	Location zero Unchanged Increment <u>1</u> /	0 X X	1 X X	1 X X

<u>1</u>/ Pointer will increment if flag is high.

Reset and first load truth table Depth expansion/compound expansion mode

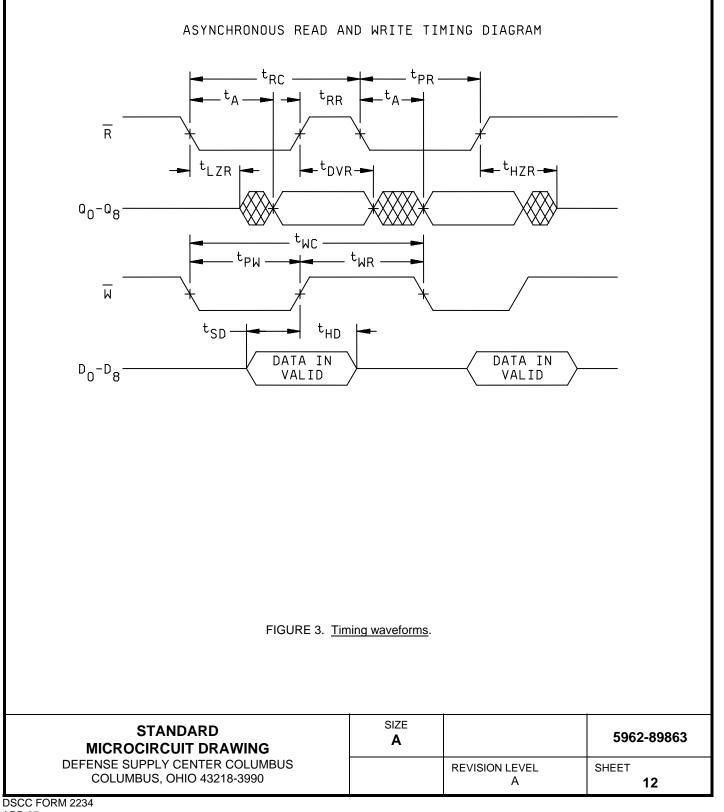
	Inputs			Internal	Outputs		
Mode	MR	FL	XI	Read pointer	Write pointer	EF	FF
Reset first device Reset all other devices Read/Write	0 0 1	0 1 X	<u>1/</u> <u>1/</u> <u>1</u> /	Location zero Location zero X	Location zero Location zero X	0 0 X	1 1 X

<u>1</u>/ \overline{XI} is connected to \overline{XO} of previous device.

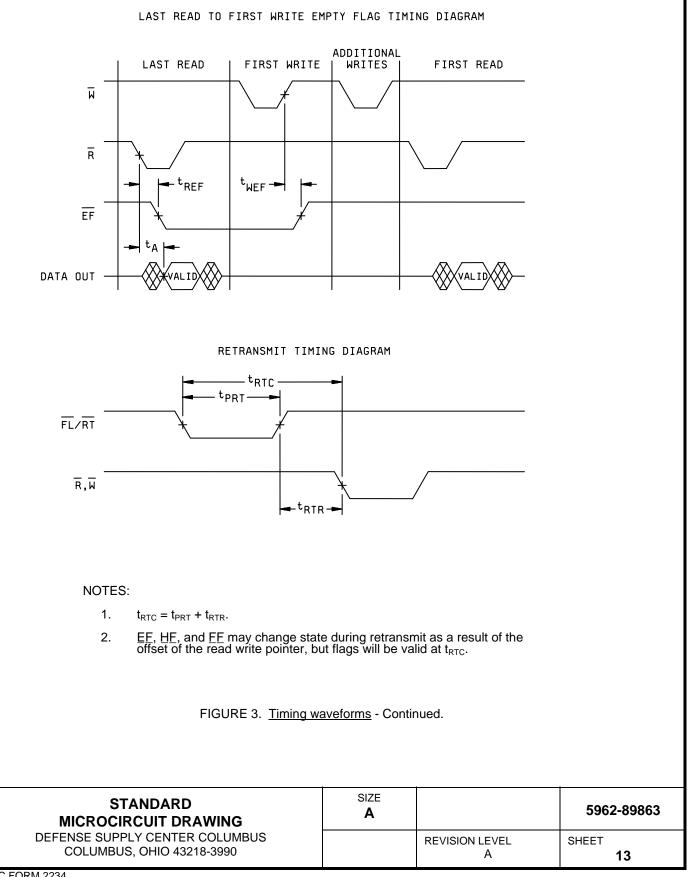
NOTE: \overline{MR} = Reset input, $\overline{FL}/\overline{RT}$ = First load/retransmit \overline{EF} = Empty flag output, \overline{FF} = Full flag output, \overline{XI} = Expansion input, and \overline{HF} = Half-full flag output

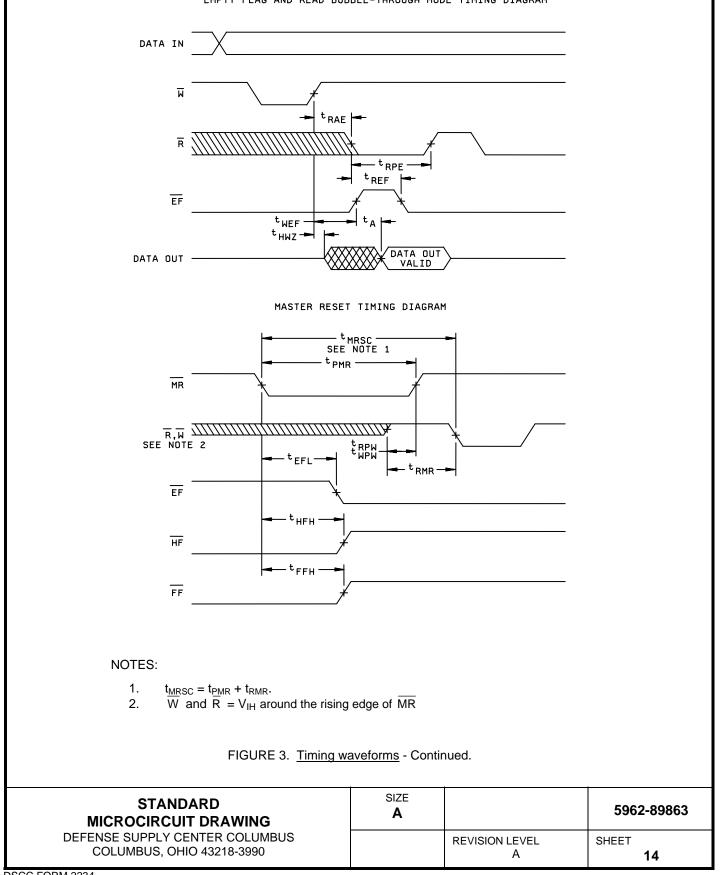
FIGURE 2. Truth table.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-89863
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EMPTY FLAG AND READ BUBBLE-THROUGH MODE TIMING DIAGRAM

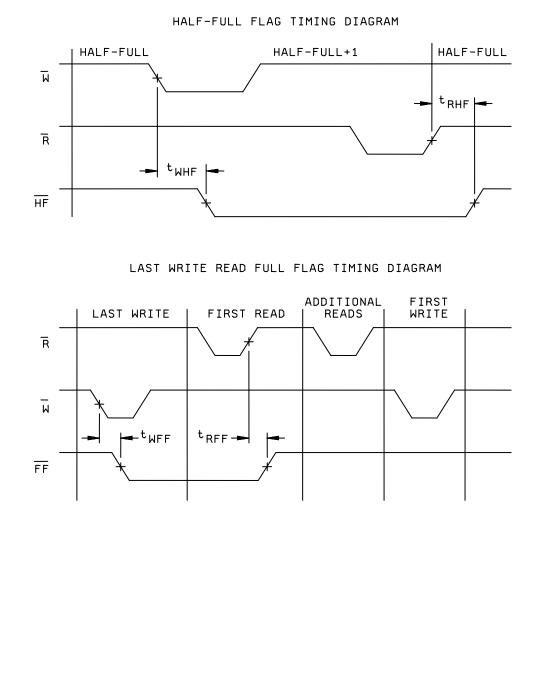
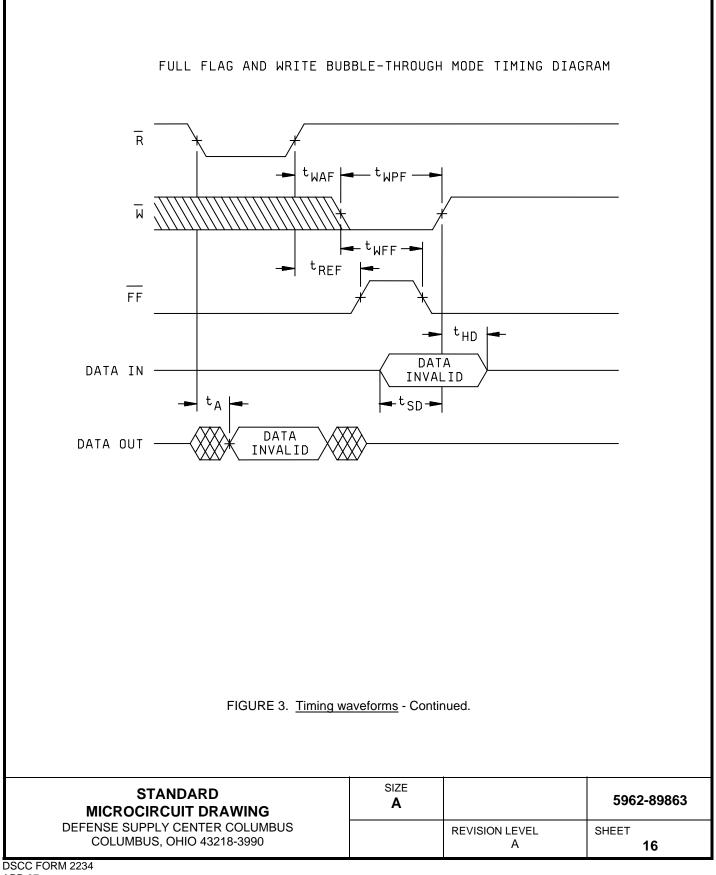
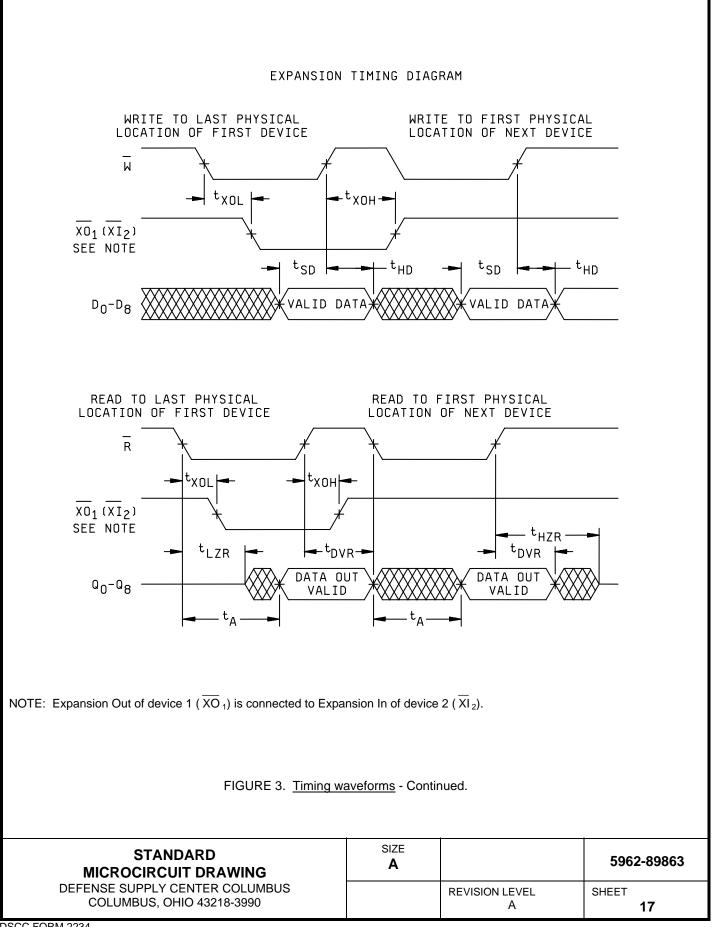


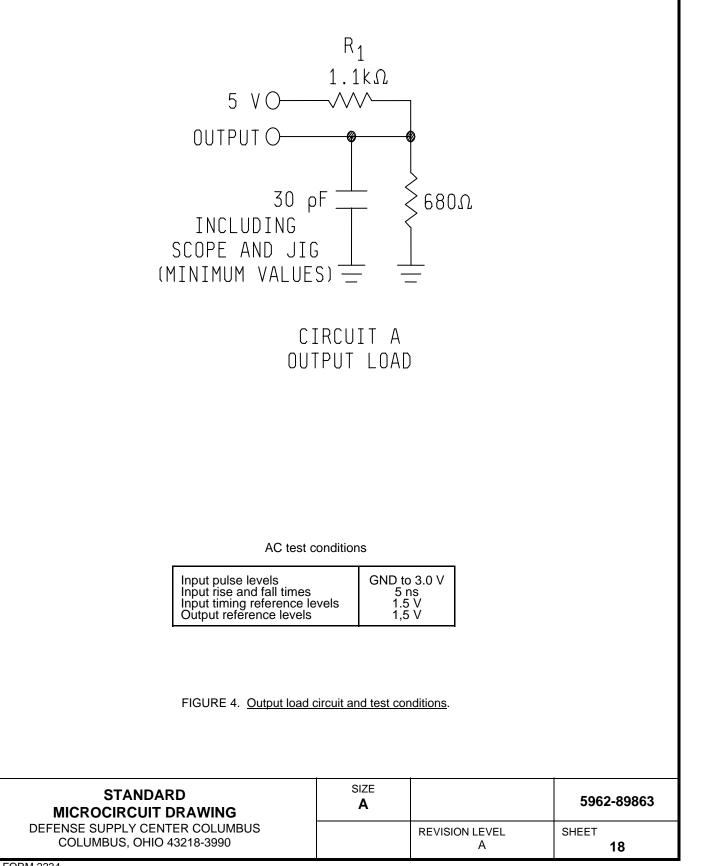
FIGURE 3. Timing waveforms - Continued.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-89863
DEFENSE SUPPLY CENTER COLUMBUS		REVISION LEVEL	SHEET
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4. VERIFICATION

4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}C$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 <u>Quality conformance inspection</u>. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

- 4.3.1 Group A inspection.
 - a. Tests shall be as specified in table II herein.
 - b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
 - c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is fifteen devices with no failures and all input and output terminals tested.
 - d. Subgroups 7 and 8 tests shall include verification of the truth table.
- 4.3.2 Groups C and D inspections.
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. Steady-state life test conditions, method 1005 of MIL-STD-883.
 - (1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $TA = +125^{\circ}C$, minimum.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10,11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ * indicates PDA applies to subgroups 1 and 7.

2/ ** see 4.3.1c.

<u>3</u>/ see 4.3.1d.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractorprepared specification or drawing.

6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 <u>Record of users</u>. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 <u>Approved sources of supply</u>. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-89863
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990		REVISION LEVEL A	SHEET 20

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-11-08

Approved sources of supply for SMD 5962-89863 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-8986301UA	0C7V7 <u>3</u> /	CY7C421-80KMB IDT7201SA80XEB
5962-8986301XA	0C7V7 <u>3</u> /	CY7C420-80DMB IDT7201SA80DB
5962-8986301YA	0C7V7 <u>3/</u> <u>3</u> /	CY7C421-80DMB IDT7201SA80TDB MM1P-67201-55MB
5962-8986301ZA	0C7V7 <u>3/</u> <u>3</u> /	CY7C421-80LMB IDT7201SA80LB MM4J-67201-55MB
5962-8986302UA	0C7V7 <u>3</u> /	CY7C421-65KMB IDT7201SA65XEB
5962-8986302XA	0C7V7 <u>3</u> /	CY7C420-65DMB IDT7201SA65DB
5962-8986302YA	0C7V7 <u>3</u> / <u>3</u> /	CY7C421-65DMB IDT7201SA65TDB MM1P-67201-55MB
5962-8986302ZA	0C7V7 <u>3</u> / <u>3</u> /	CY7C421-65LMB IDT7201SA65LB MM4J-67201-55MB
5962-8986303UA	0C7V7 <u>3</u> /	CY7C421-50KMB IDT7201SA50XEB
5962-8986303XA	0C7V7 <u>3</u> /	CY7C420-50DMB IDT7201SA50DB
5962-8986303YA	0C7V7 61772 <u>3</u> /	CY7C421-50DMB IDT7201SA50TDB MM1P-67201-45MB
5962-8986303ZA	0C7V7 <u>3/</u> <u>3</u> /	CY7C421-50LMB IDT7201SA50LB MM4J-67201-45MB
5962-8986304UA	0C7V7 <u>3</u> /	CY7C421-40KMB IDT7201SA40XEB
5962-8986304XA	0C7V7 <u>3</u> /	CY7C421-40DMB IDT7201SA40DB

See footnotes at end of table.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>1</u> /
5962-8986304YA	0C7V7 <u>3</u> / <u>3</u> /	CY7C421-40DMB IDT7201SA40TDB MM1P-67201-35MB
5962-8986304ZA	0C7V7 <u>3/</u> <u>3</u> /	CY7C421-40LMB IDT7201SA40LB MM4J-67201-35MB
5962-8986305UA	0C7V7 <u>3</u> /	CY7C421-30KMB IDT7201SA30XEB
5962-8986305XA	0C7V7 <u>3</u> /	CY7C420-30DMB IDT7201SA30DB
5962-8986305YA	0C7V7 61772	CY7C421-30DMB IDT7201SA30TDB
5962-8986305ZA	0C7V7 <u>3</u> /	CY7C421-30LMB IDT7201SA30LB
5962-8986306UA	0C7V7	CY7C421-25KMB
5962-8986306XA	0C7V7	CY7C420-25DMB
5962-8986306YA	0C7V7	CY7C421-25DMB
5962-8986306ZA	0C7V7	CY7C421-25LMB

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.
- 2/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- $\underline{3}$ / Not available from an approved source.

Vendor CAGE number	Vendor name <u>and address</u>
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051
61772	Integrated Device Technology, Inc. 2975 Stender Way Santa Clara, CA 95054

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 72V201L10PFG
 CY7C464A-10JI
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