REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update to current requirements. Editorial changes throughout. - gap	06-07-10	Raymond Monnin

REV																				
SHEET																				
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SHEET																				

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

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DRAWING APPROVAL DATE
92-12-15

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED SCHOTTKY TTL, UP/DOWN BINARY COUNTER WITH PRESET AND RIPPLE CLOCK, MONOLITHIC SILICON

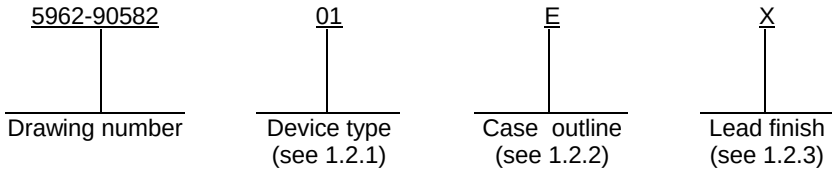
SIZE	CAGE CODE	
A	**67268**	**5962-90582**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54F191	Up/down binary counter with preset and ripple clock

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16	16	dual-in-line package
F	GDFP2-F16	16	flat package
2	CQCC1-N20	20	square chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
DC input voltage range	-0.5 V dc to +7.0 V dc
Input current range	-30 mA to +5.0 mA
Voltage applied to output in high state (with V_{CC} = 0 V)	-0.5 V dc to V_{CC}
Storage temperature range	-65°C to +150°C
Ambient temperature range under bias	-55°C to +125°C
Maximum power dissipation (P_D) 1/	500 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum low-level input voltage (V_{IL})	0.8 V dc
Minimum setup time, high or low, Pn to $\overline{PL}$ ($t_{S(H)}$, $t_{S(L)}$)	6.0 ns
Minimum hold time, high or low, Pn to $\overline{PL}$ ($t_{h(H)}$, $t_{h(L)}$)	2.0 ns
Minimum setup time, low, $\overline{CE}$ to CP ($t_{S(L)}$)	10.5 ns
Minimum hold time, low, $\overline{CE}$ to CP ($t_{h(L)}$)	0 ns
Minimum setup time, high or low, $\overline{U}$/D to CP ($t_{S(H)}$, $t_{S(L)}$)	12.0 ns
Minimum hold time, high or low, $\overline{U}$/D to CP ($t_{h(H)}$, $t_{h(L)}$)	0 ns
Minimum $\overline{PL}$ pulse width, low ($t_{W(L)}$)	8.5 ns
Minimum CP pulse width, low ($t_{W(L)}$)	7.0 ns
Minimum recovery time $\overline{PL}$ to CP (t_{rec})	7.5 ns
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil;quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth and mode select tables. The truth and mode select tables shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -1 mA V_{IH} = 2.0 V		1, 2, 3	2.5		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 20 mA V_{IL} = 0.8 V		1, 2, 3		0.5	V
Input clamp diode voltage	V_{CD}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1, 2, 3		-1.2	V
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V				20	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 7.0 V		1, 2, 3		100	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V	V_{IN} = 0.5 V (except $\overline{CE}$)	1, 2, 3		-0.6	mA
			V_{IN} = 0.5 V ($\overline{CE}$)	1, 2, 3		-1.8	mA
Short-circuit output current	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0 V 1/		1, 2, 3	-60	-150	mA
High level output leakage current	I_{CEX}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V		1, 2, 3		250	µA
Supply current	I_{CC}	V_{CC} = 5.5 V		1,2,3		55	mA
Functional tests		V_{CC} = 4.5 V, 5.5 V See 4.3.1c 2/		7, 8			
Maximum count frequency	f_{MAX}	R_L = 500 Ω		9	100		MHz
		C_L = 50 pF		10, 11	75		
Propagation delay time, CP to Qn	t_{PLH1}	See figure 4	V_{CC} = 5.0 V	9	3.0	7.5	ns
			V_{CC} = 4.5 V, 5.5 V	10, 11	3.0	9.5	
	t_{PHL1}		V_{CC} = 5.0 V	9	5.0	11.0	
			V_{CC} = 4.5 V, 5.5 V	10, 11	5.0	13.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Propagation delay time, CP to TC	t_{PLH2}	R_L = 500 Ω	V_{CC} = 5.0 V	9	6.0	13.0	ns
		C_L = 50 pF	V_{CC} = 4.5 V, 5.5 V	10, 11	6.0	16.5	
	t_{PHL2}	See figure 4	V_{CC} = 5.0 V	9	5.0	11.0	
			V_{CC} = 4.5 V, 5.5 V	10, 11	5.0	13.5	
Propagation delay time, CP to $\overline{RC}$	t_{PLH3}		V_{CC} = 5.0 V	9	3.0	7.5	ns
			V_{CC} = 4.5 V, 5.5 V	10, 11	3.0	9.5	
	t_{PHL3}		V_{CC} = 5.0 V	9	3.0	7.0	
			V_{CC} = 4.5 V, 5.5 V	10, 11	3.0	9.0	
Propagation delay time, $\overline{CE}$ to $\overline{RC}$	t_{PLH4}		V_{CC} = 5.0 V	9	3.0	7.0	ns
			V_{CC} = 4.5 V, 5.5 V	10, 11	3.0	9.0	
	t_{PHL4}		V_{CC} = 5.0 V	9	3.0	7.0	
			V_{CC} = 4.5 V, 5.5 V	10, 11	3.0	9.0	
Propagation delay time, $\overline{U}$/D to $\overline{RC}$	t_{PLH5}		V_{CC} = 5.0 V	9	7.0	18.0	ns
			V_{CC} = 4.5 V, 5.5 V	10, 11	7.0	22.0	
	t_{PHL5}		V_{CC} = 5.0 V	9	5.5	12.0	
			V_{CC} = 4.5 V, 5.5 V	10, 11	5.5	14.0	
Propagation delay time, $\overline{U}$/D to TC	t_{PLH6}		V_{CC} = 5.0 V	9	4.0	10.0	ns
			V_{CC} = 4.5 V, 5.5 V	10, 11	4.0	13.5	
	t_{PHL6}		V_{CC} = 5.0 V	9	4.0	10.0	
			V_{CC} = 4.5 V, 5.5 V	10, 11	4.0	12.5	
Propagation delay time, Pn to Qn	t_{PLH7}		V_{CC} = 5.0 V	9	3.0	7.0	ns
			V_{CC} = 4.5 V, 5.5 V	10, 11	3.0	9.0	
	t_{PHL7}		V_{CC} = 5.0 V	9	6.0	13.0	
			V_{CC} = 4.5 V, 5.5 V	10, 11	6.0	16.0	
Propagation delay time, $\overline{PL}$ to Qn	t_{PLH8}		V_{CC} = 5.0 V	9	5.0	11.0	ns
			V_{CC} = 4.5 V, 5.5 V	10, 11	5.0	13.0	
	t_{PHL8}		V_{CC} = 5.0 V	9	5.5	12.0	
			V_{CC} = 4.5 V, 5.5 V	10, 11	5.5	14.5	

1/ Not more than one output should be shorted at a time, and the duration of the short-circuit condition should not exceed one second.

2/ Functional tests shall be conducted at input test conditions of $GND \le V_{IL} \le V_{OL}$ and $V_{OH} \le V_{IH} \le V_{CC}$.

Case outlines	E and F	2
Terminal number	Terminal symbols	
1	P_1	NC
2	Q_1	P_1
3	Q_0	Q_1
4	$\overline{CE}$	Q_0
5	$\overline{U}/D$	$\overline{CE}$
6	Q_2	NC
7	Q_3	$\overline{U}/D$
8	GND	Q_2
9	P_3	Q_3
10	P_2	GND
11	$\overline{PL}$	NC
12	TC	P_3
13	$\overline{RC}$	P_2
14	CP	$\overline{PL}$
15	P_0	TC
16	V_{CC}	NC
17	- - -	$\overline{RC}$
18	- - -	CP
19	- - -	P_0
20	- - -	V_{CC}

FIGURE 2. Terminal connections.

Mode select table.

Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}$ / D	CP	
H	L	L	_/‾	Count up Count down Preset (Asynchronous) No change (Hold)
H	L	H	_/‾	
L	X	X	X	
H	H	X	X	

$\overline{RC}$ Truth table

Inputs			Outputs
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⊓	⊓
H	X	X	H
X	L	X	H

H = High voltage level.
L = Low voltage level.
* TC is generated internally.
X = Irrelevant.
_/‾ = Transition from low-to-high level.
⊓ = One low level pulse.

FIGURE 2. Truth and mode select tables

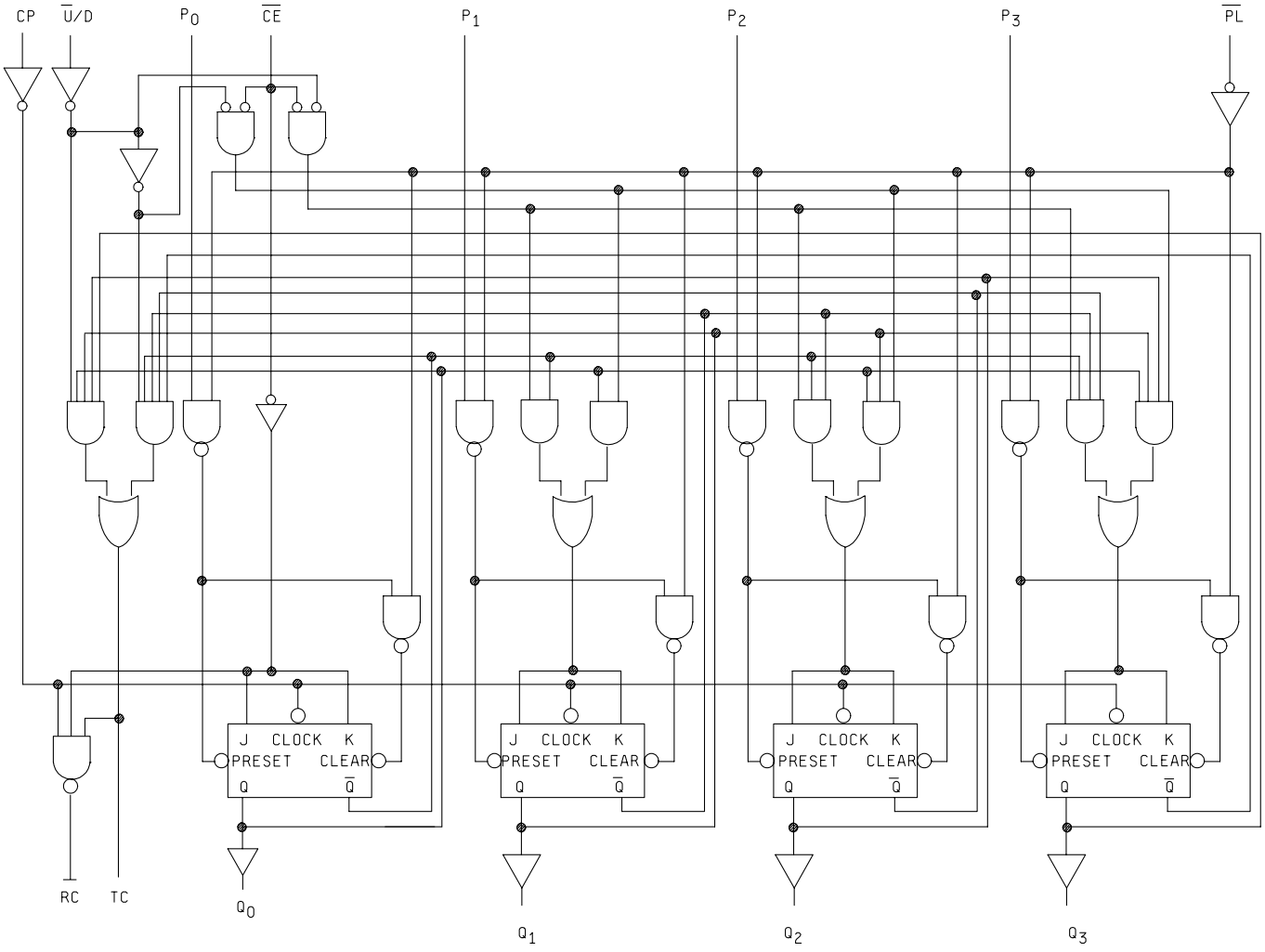
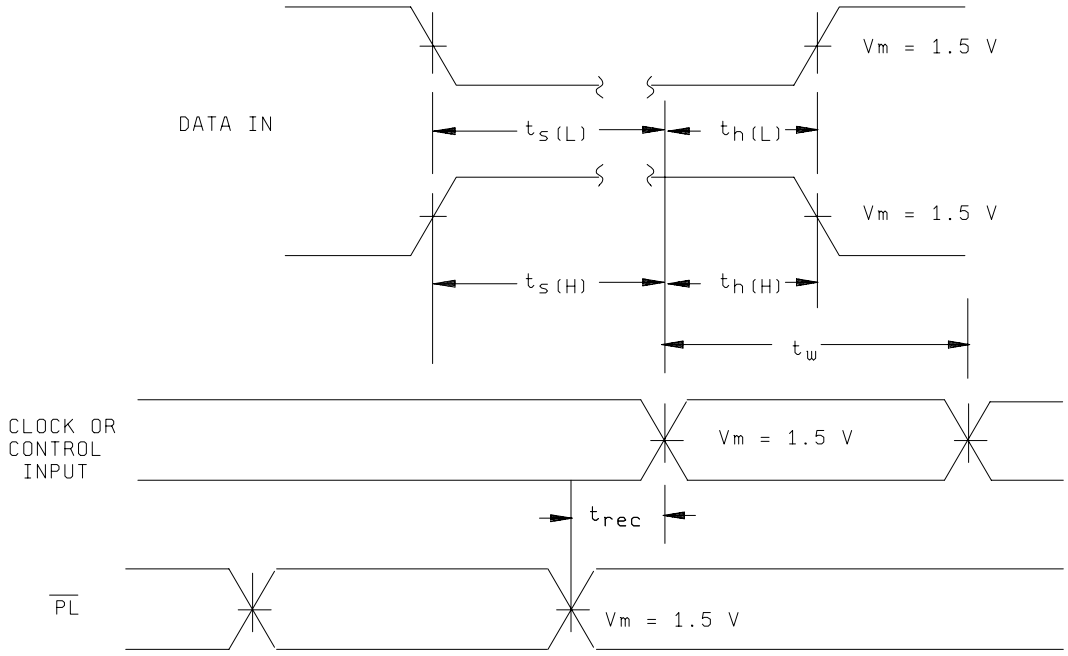


FIGURE 3. Logic diagram.

Setup time, hold time, and recovery time waveforms



Test load

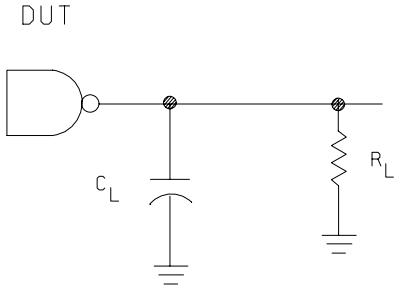
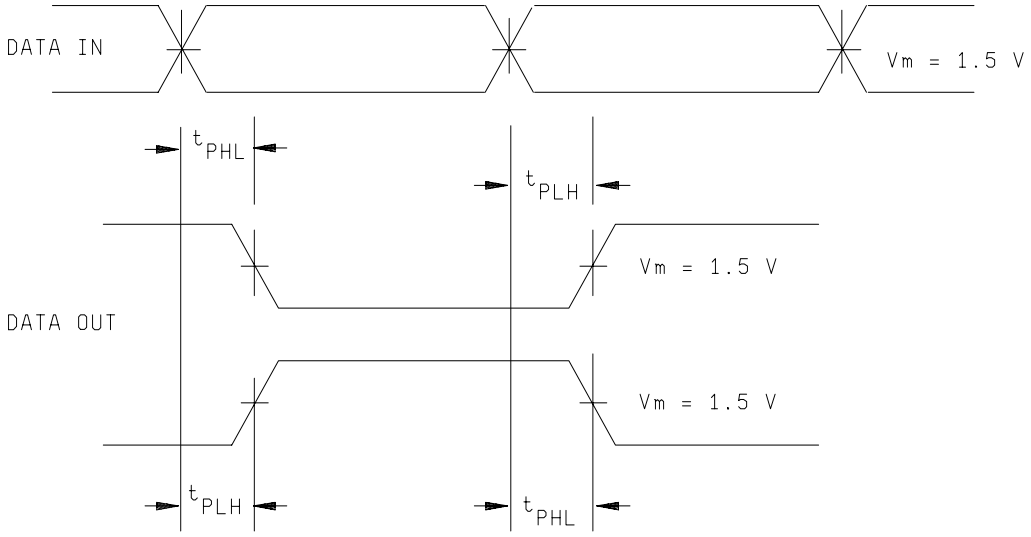


FIGURE 4. Test circuit and switching waveforms.

Propagation delay waveforms



NOTES:
1. C_L includes probe and jig capacitance.
2. All input pulses have the following characteristics: PRR = 1 MHz, $t_r = t_f = 2.5$ ns, duty cycle = 50 percent.

FIGURE 4. Test circuit and switching waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1 and 7.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-07-10

Approved sources of supply for SMD 5962-90582 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9058201EA	27014	54F191DMQB
5962-9058201FA	27014	54F191FMQB
5962-90582012A	27014	54F191LMQB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor Corporation 2900 Semiconductor Drive P. O. Box 58090 Santa Clara, CA 95052-8090

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5962-8956101EA MC10E446FNG 74HC195N 74HC4516N 74HCT182N HEF4021BD HEF4534BP MC144111P NLV74HC165ADTR2G 5962-9172201M2A MC74HC597ADG MC100EP142MNG MC100EP016AMNG 5962-9172201MFA MC74HC164BDR2G TC74HC165AP(F) 74AHC164T14-13 MC74LV594ADR2G NLV14094BDTR2G NLV74HC595ADTG MC74HC165AMNTWG TPIC6C595PWG4 74VHC164MTCX CD74HC195M96 CD4073BM96 CD4053BM96 MM74HC595MTCX 74HCT164T14-13 74HCT164S14-13 74HC4094D-Q100J NLV14014BFELG NLV74HC165ADR2G NLV74HC589ADTR2G NPIC6C595D-Q100,11 NPIC6C595PW,118 NPIC6C596ADJ NPIC6C596APW-Q100J NPIC6C596D-Q100,11 BU4094BCF-E2 BU4094BCFV-E2 74HC164D14 74HC164T14-13 TPIC6C596PWRG4 STPIC6D595MTR STP08CP05MTR CD74HC123E 74HC164D.653 74HC165D.653 74HCT165D.652 74HCT164D.652