REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Boilerplate update and part of five year review. tcr	07-04-04	Robert M. Heber

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30				

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Jeff Bowling

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Jeff Bowling

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
93-03-11

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 2K X 8-DUAL PORT STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON

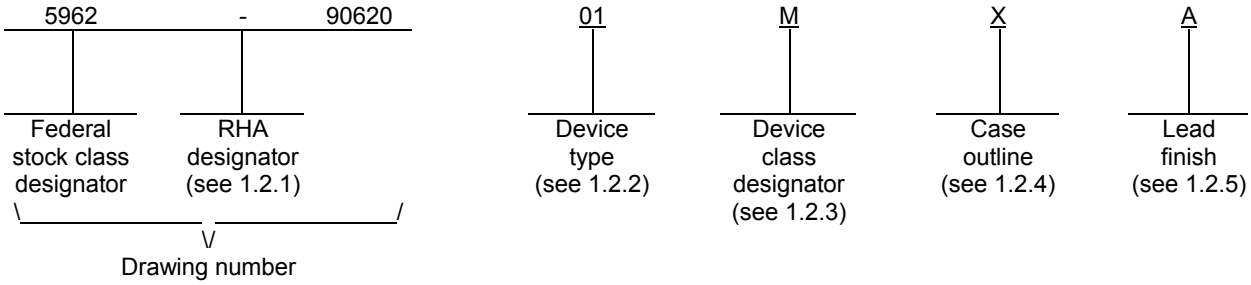
REVISION LEVEL	SIZE	CAGE CODE	
A	A	67268	**5962-90620**

SHEET 1 OF 30

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	7C132	2K X 8 Dual port SRAM, MASTER	55 ns
02	7C132	2K X 8 Dual port SRAM, MASTER	45 ns
03	7C132	2K X 8 Dual port SRAM, MASTER	35 ns
04	7C142	2K X 8 Dual port SRAM, SLAVE	55 ns
05	7C142	2K X 8 Dual port SRAM, SLAVE	45 ns
06	7C142	2K X 8 Dual port SRAM, SLAVE	35 ns
07	7C136	2K X 8 Dual port SRAM, MASTER	55 ns
08	7C136	2K X 8 Dual port SRAM, MASTER	45 ns
09	7C136	2K X 8 Dual port SRAM, MASTER	35 ns
10	7C146	2K X 8 Dual port SRAM, SLAVE	55 ns
11	7C146	2K X 8 Dual port SRAM, SLAVE	45 ns
12	7C146	2K X 8 Dual port SRAM, SLAVE	35 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CQCC1-N52	52	Square leadless chip carrier
Y	GDIP1-T48 or CDIP2-T48	48	Dual-in-line
Z	See figure 1	48	Square leadless chip carrier
U	See figure 1	48	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC voltage range applied to outputs in high Z state	-0.5 V dc to +7.0 V dc
DC Input voltage range	-3.0 V dc to +7.0 V dc
DC output current	20 mA
Maximum power dissipation 1/	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases X and Y	See MIL-STD-1835
Cases Z and U	10°C/W 2/
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias range	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage range (V_{IH})	2.2 V dc to V_{CC} + 0.5 V dc
Input low voltage range (V_{IL}) 3/	-0.5 V dc to 0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
3/ Negative undershoots to a minimum of -3.0 V are allowed with a maximum of 20 ns pulse width.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-00 - Standard Guide for the Measurement of Single Event Phenomena (SEP) induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

ELECTRONICS INDUSTRIES ALLIANCE (EIA)

JEDEC Standard EIA/JESD 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.2.5 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL- PRF -38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

3.11 Serialization for device classes V. Class V shall be serialized in accordance with MIL- PRF -38535.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V $V_{IN} = V_{IH}, V_{IL}$ I_{OH} = -4.0 mA	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, $V_{IN} = V_{IH}, V_{IL}$					
		I_{OL} = 4.0 mA	1,2,3	All		0.4	V
		I_{OL} = 16.0 mA 1/	1,2,3	All		0.5	
Input high voltage 2/	V_{IH}		1,2,3	All	2.2		V
Input low voltage 2/	V_{IL}		1,2,3	All		0.8	V
Input leakage current	I_{IX}	V_{IN} = 5.5 V to GND	1,2,3	All	-5	5	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V to GND	1,2,3	All	-5	5	µA
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA $\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$, $f = f_{MAX}$ 3/	1,2,3	01,02,04, 05,07,08, 10,11		120	mA
				03,06, 09,12		170	
Standby supply current, both ports, TTL inputs	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA $\overline{CE}_L$ and $\overline{CE}_R = V_{IH}$, $f = f_{MAX}$ 3/	1,2,3	01,02,04, 05,07,08, 10,11		45	mA
				03,06, 09,12		65	
Standby supply current, one port, TTL inputs	I_{CC3}	V_{CC} = 5.5 V, I_{OUT} = 0 mA $\overline{CE}_R$ or $\overline{CE}_L = V_{IH}$, $f = f_{MAX}$ 3/	1,2,3	01,02,04, 05,07,08, 10,11		90	mA
				03,06, 09,12		115	
Standby supply current, both ports, CMOS inputs	I_{CC4}	V_{CC} = 5.5 V, I_{OUT} = 0 mA $\overline{CE}_L$ and $\overline{CE}_R \ge (V_{CC}$ -0.2V), all other inputs $\ge (V_{CC} - 0.2\ V)$, or ≤ 0.2 V, f = 0 3/	1,2,3	All		15	mA
Standby supply current, one port, CMOS inputs	I_{CC5}	V_{CC} = 5.5 V, I_{OUT} = 0 mA $\overline{CE}_L$ or $\overline{CE}_R \ge (V_{CC}$ -0.2V), all other inputs $\ge (V_{CC} - 0.2\ V)$, or ≤ 0.2 V, $f = f_{MAX}$ 3/	1,2,3	01,02,04, 05,07,08, 10,11		85	mA
				03,06, 09,12		105	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance 4/	C_{IN}	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (See 4.4.1e)	4	All		15	ns
Output capacitance 4/	C_{OUT}	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (See 4.4.1e)	4	All		10	ns
Functional tests		See 4.4.1c	7,8A,8B	All			
Read cycle time	t_{AVAV}	See figures 4 and 5, read cycle timing 5/	9, 10, 11	01,04, 07,10	55		ns
				02,05, 08,11	45		
				03,06, 09,12	35		
Address access time	t_{AVQV}		9, 10, 11	01,04, 07,10		55	ns
				02,05, 08,11		45	
				03,06, 09,12		35	
Output hold from address change 4/	t_{AVQX}		9, 10, 11	All	0		ns
Chip enable access time	t_{ELQV}		9, 10, 11	01,04, 07,10		55	ns
				02,05, 08,11		45	
				03,06, 09,12		35	
Output enable access time	t_{OLQV}		9, 10, 11	01,02,04, 05,07,08, 10,11		25	ns
				03,06, 09,12		20	
Output enable to output active	t_{OLQX}	See figures 4 and 5, read cycle timing 4/ 6/	9, 10, 11	All	3		ns
Output enable to output inactive	t_{OHQZ}		9, 10, 11	01,04, 07,10		25	ns
				02,03,05, 06,08,09, 11,12		20	
Chip enable to output active	t_{ELQX}		9, 10, 11	All	5		ns
Chip select to output inactive	t_{EHQZ}		9, 10, 11	01,04, 07,10		25	ns
				02,03,05, 06,08,09, 11,12		20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip enable to power up 4/	t_{ELPU}	See figures 4 and 5, read cycle timing 5/	9, 10, 11	All	0		ns
Chip enable to power down 4/	t_{EHPD}		9, 10, 11	All		35	ns
Write cycle time	t_{AVAV}	See figures 4 and 5, write cycle timing 5/	9, 10, 11	01,04, 07,10	55		ns
				02,05, 08,11	45		
				03,06, 09,12	35		
Chip enable to write end	t_{ELWH}		9, 10, 11	01,04, 07,10	40		ns
				02,05, 08,11	35		
				03,06, 09,12	30		
Address setup to end of write	t_{AVWH}		9, 10, 11	01,04, 07,10	40		ns
				02,05, 08,11	35		
				03,06, 09,12	30		
Address hold from write end	t_{WHAX}		9, 10, 11	All	2		ns
Address setup to write start	t_{AVWL}		9, 10, 11	All	0		ns
Write enable pulse width	t_{WLWH}		9, 10, 11	01,02,04, 05,07,08, 10,11	30		ns
				03,06, 09,12	25		
Data setup to write end	t_{DVWH}		9, 10, 11	01,02,04, 05,07,08, 10,11	20		ns
				03,06, 09,12	15		
Data hold from write end	t_{WHDX}		9, 10, 11	All	0		ns
Write enable low to output inactive	t_{WLQZ}	See figures 4 and 5, write cycle timing 4/ 6/	9, 10, 11	01,04, 07,10		25	ns
				02,03,05, 06,08,09, 11,12		20	
Write enable high to output active	t_{WHQX}		9, 10, 11	All	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Busy low from address match	t_{BLA}	See figures 4 and 5, busy cycle timing 5/	9, 10, 11	01,07		30	ns
				02,08		25	
				03,09		20	
Busy high from address mismatch 7/	t_{BHA}		9, 10, 11	01,07		30	ns
				02,08		25	
				03,09		20	
Busy low from chip enable low	t_{BLC}		9, 10, 11	01,07		30	ns
				02,08		25	
				03,09		20	
Busy high from chip enable high 7/	t_{BHC}		9, 10, 11	01,07		30	ns
				02,08		25	
				03,09		20	
Port setup for priority	t_{PS}		9, 10, 11	01-03, 07-09	5		ns
Write enable low after busy low	t_{WB}		9, 10, 11	04-06 10-12	0		ns
Write enable high after busy high	t_{WH}		9, 10, 11	04,05 10,11	35		ns
				06,12	30		
Busy high to valid data	t_{BDD}		9, 10, 11	01,02, 07,08		45	ns
				03,09		35	
Write data valid to read data valid 4/	t_{DDD}		9, 10, 11	01-03, 07-09		8/	ns
Write pulse to data delay 4/	t_{WDD}		9, 10, 11	01-03, 07-09		8/	ns
Write enable to interrupt set time	t_{WINS}	See figures 4 and 5, interrupt cycle timing 5/	9, 10, 11	07,10		45	ns
				08,11		35	
				09,12		25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Chip enable to interrupt set time	t_{EINS}	See figures 4 and 5, interrupt cycle timing 5/	9, 10, 11	07,10		45	ns
				08,11		35	
				09,12		25	
Address to interrupt interrupt set time	t_{INS}		9, 10, 11	07,10		45	ns
				08,11		35	
				09,12		25	
Output enable to interrupt reset time 7/	t_{OINR}		9, 10, 11	07,10		45	ns
				08,11		35	
				09,12		25	
Chip enable to interrupt reset time 7/	t_{EINR}		9, 10, 11	07,10		45	ns
				08,11		35	
				09,12		25	
Address to interrupt reset time 7/	t_{INR}		9, 10, 11	07,10		45	ns
				08,11		35	
				09,12		25	

1/ $\overline{BUSY}$ and $\overline{INT}$ outputs only.

2/ These are absolute values with respect to device ground and all overshoots and undershoots due to system or tester noise are included.

3/ At $f = f_{MAX}$, address and data inputs are cycling at the maximum frequency of $1/t_{AVAV}$.

4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

5/ AC tests are performed with transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load in figure 4 (circuit A). For $\overline{BUSY}$ and $\overline{INT}$ loads for devices 01-03 and 07-09 , see figure 4 (circuit C).

6/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input, C_L = 5 pF (including scope and jig). See figure 4 (circuit B). For $\overline{BUSY}$ and $\overline{INT}$ loads for devices 01-03 and 07-09 , see figure 4 (circuit C).

7/ These parameters are measured from the input signal changing, until the output pin goes to the high-impedance state.

8/ A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:

A. $\overline{BUSY}$ on Port B goes HIGH.

B. Port B's address toggled.

C. $\overline{CE}$ for Port B is toggled.

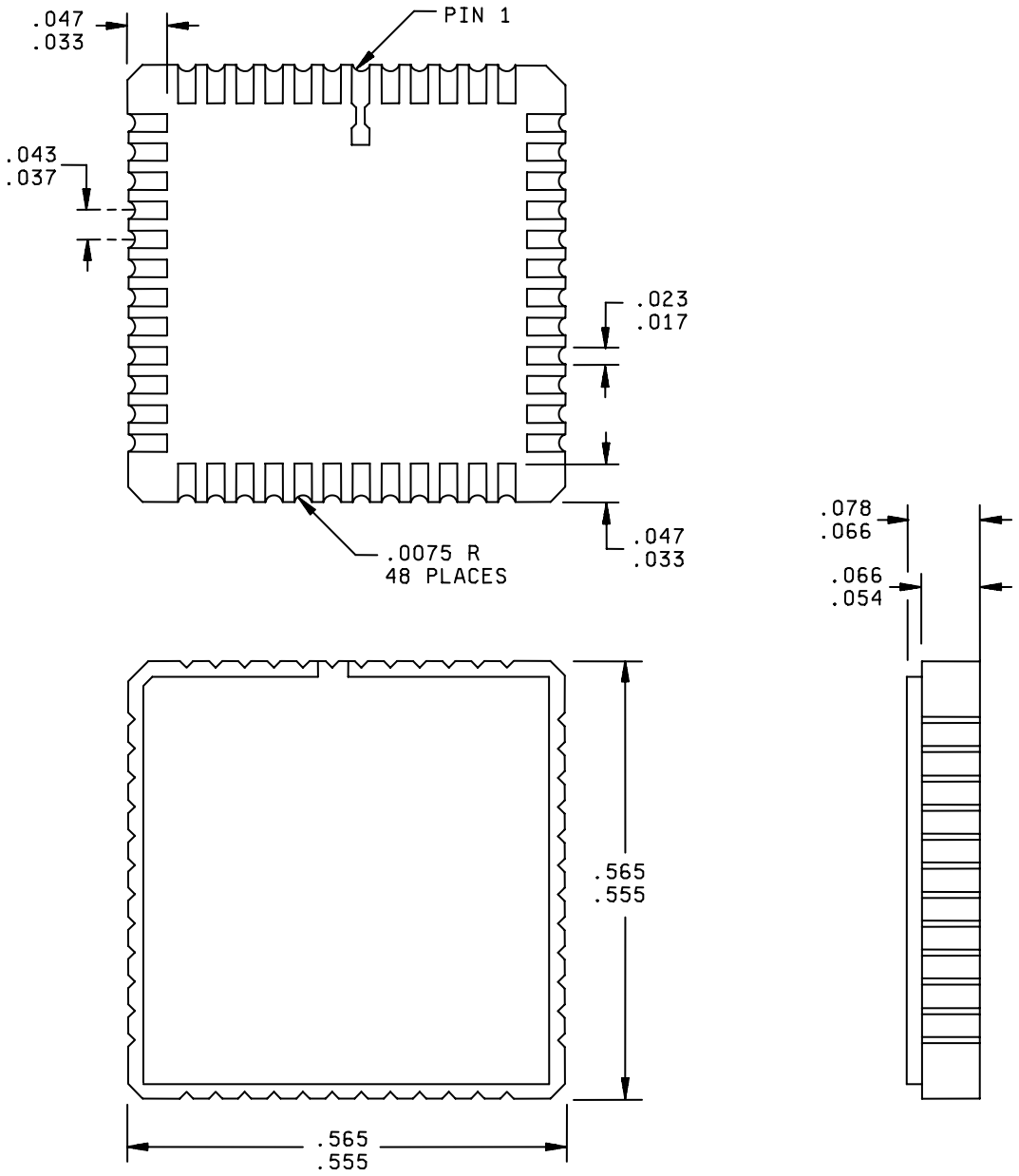
D. R/$\overline{W}$ for Port B is toggled, during valid read.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line No.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, method 5005, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9,10,11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicates tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters.
7/ See 4.4.1d.

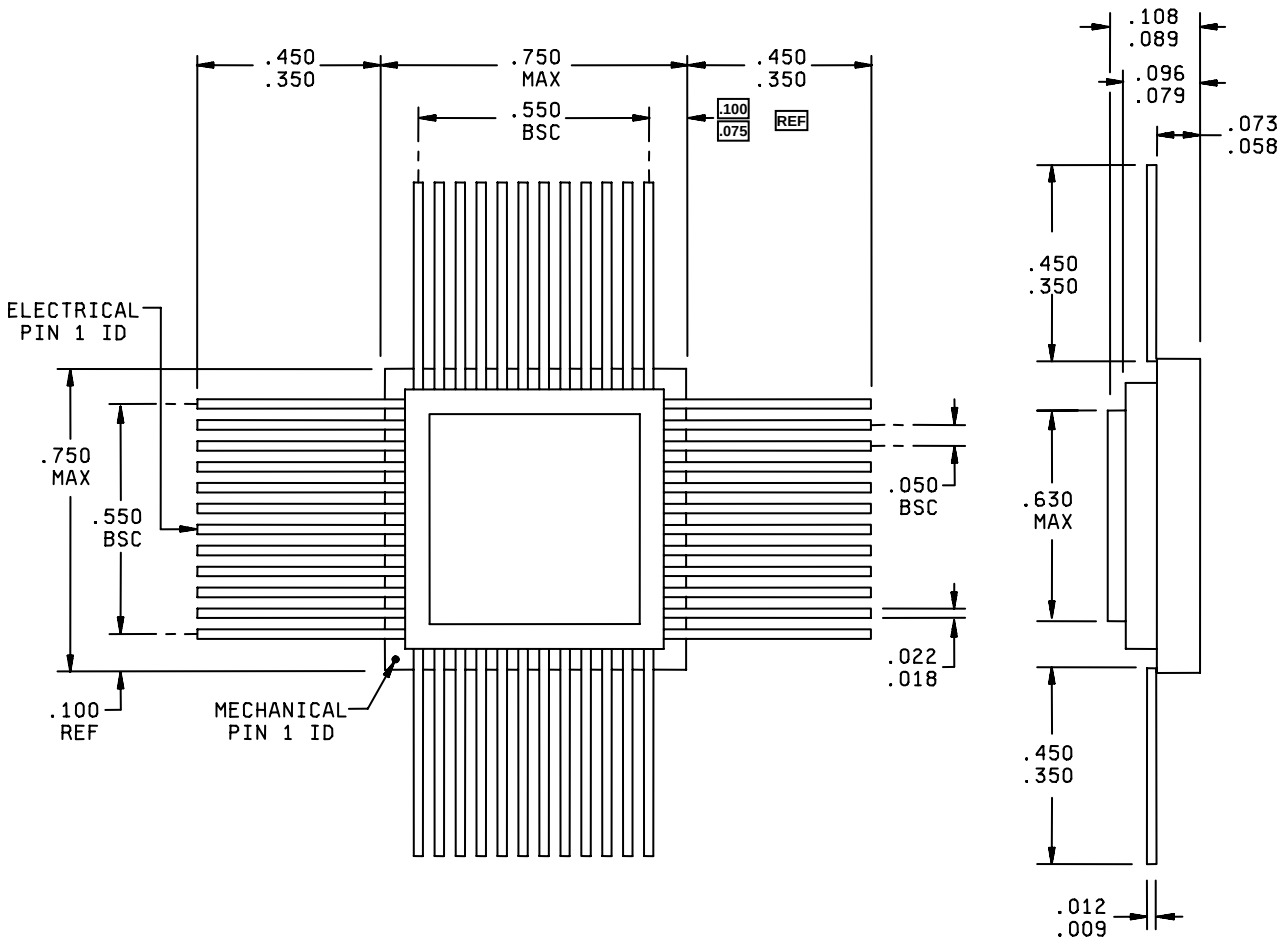
Case Z



Inches	mm	Inches	mm
.0075	0.191	.047	1.19
.017	0.43	.054	1.37
.023	0.58	.066	1.68
.033	0.84	.078	1.98
.037	0.94	.555	14.10
.043	1.09	.565	14.35

FIGURE 1. Case outlines .

Case U



Inches	mm	Inches	mm
.009	0.23	.096	2.44
.012	0.30	.100	2.54
.018	0.46	.108	2.74
.022	0.56	.350	8.89
.050	1.27	.450	11.43
.058	1.47	.550	13.97
.073	1.85	.630	16.00
.079	2.01	.750	19.05
.089	2.26		

NOTES:

1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 1. Case outlines - Continued.

Device types	01-06	07-12	Device types	01-06	07-12
Case outlines	Y, Z and U	X	Case outlines	Y, Z and U	X
Terminal number	Terminal symbol		Terminal number	Terminal symbol	
1	$\overline{CE}_L$	$\overline{CE}_L$	27	I/O_{2R}	I/O_{0R}
2	$R/\overline{W}_L$	$R/\overline{W}_L$	28	I/O_{3R}	I/O_{1R}
3	$\overline{BUSY}_L$	$\overline{BUSY}_L$	29	I/O_{4R}	I/O_{2R}
4	A_{10L}	$\overline{INT}_L$	30	I/O_{5R}	I/O_{3R}
5	$\overline{OE}_L$	A_{10L}	31	I/O_{6R}	I/O_{4R}
6	A_{0L}	$\overline{OE}_L$	32	I/O_{7R}	I/O_{5R}
7	A_{1L}	A_{0L}	33	A_{9R}	I/O_{6R}
8	A_{2L}	A_{1L}	34	A_{8R}	I/O_{7R}
9	A_{3L}	A_{2L}	35	A_{7R}	NC
10	A_{4L}	A_{3L}	36	A_{6R}	A_{9R}
11	A_{5L}	A_{4L}	37	A_{5R}	A_{8R}
12	A_{6L}	A_{5L}	38	A_{4R}	A_{7R}
13	A_{7L}	A_{6L}	39	A_{3R}	A_{6R}
14	A_{8L}	A_{7L}	40	A_{2R}	A_{5R}
15	A_{9L}	A_{8L}	41	A_{1R}	A_{4R}
16	I/O_{0L}	A_{9L}	42	A_{0R}	A_{3R}
17	I/O_{1L}	I/O_{0L}	43	$\overline{OE}_R$	A_{2R}
18	I/O_{2L}	I/O_{1L}	44	A_{10R}	A_{1R}
19	I/O_{3L}	I/O_{2L}	45	$\overline{BUSY}_R$	A_{0R}
20	I/O_{4L}	I/O_{3L}	46	$R/\overline{W}_R$	$\overline{OE}_R$
21	I/O_{5L}	I/O_{4L}	47	$\overline{CE}_R$	A_{10R}
22	I/O_{6L}	I/O_{5L}	48	V_{CC}	$\overline{INT}_R$
23	I/O_{7L}	I/O_{6L}	49	----	$\overline{BUSY}_R$
24	GND	I/O_{7L}	50	----	$R/\overline{W}_R$
25	I/O_{0R}	NC	51	----	$\overline{CE}_R$
26	I/O_{1R}	GND	52	----	V_{CC}

FIGURE 2. Terminal connections.

Noncontention read/write control

Left or right port (see note 1)				Function
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	
X	H	X	Z	Port disabled and in power-down mode I_{CC3} or I_{CC5}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, power-down mode I_{CC2} or I_{CC4}
L	L	X	Data in	Data on port written into memory (see note 2)
H	L	L	Data out	Data in memory output on port (see note 3)
H	L	H	z	High impedance outputs

NOTES:

1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid. See t_{WDD} and t_{DDD} timing.

H = High, L = Low, X = Don't care, Z = High impedance

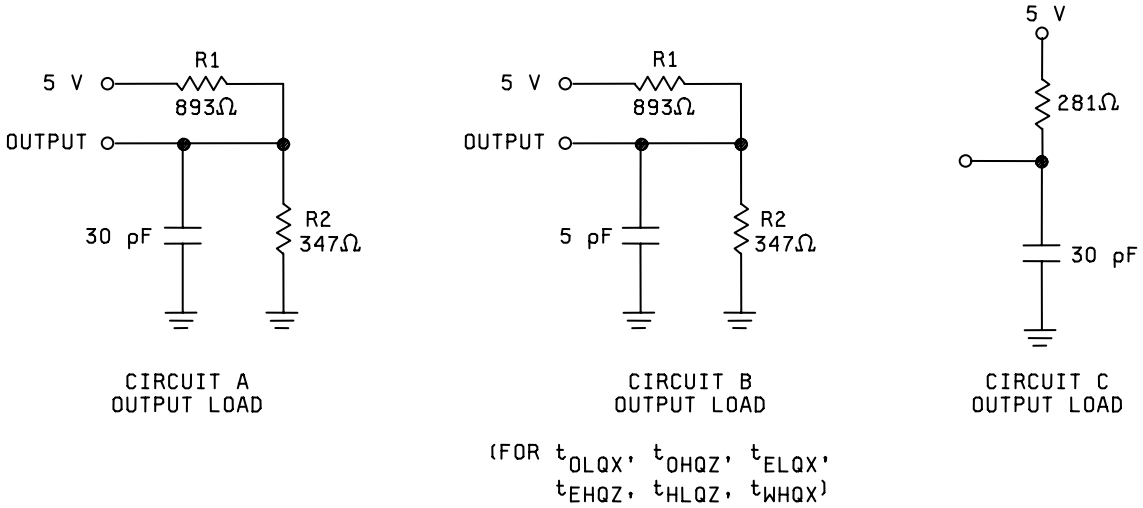
FIGURE 3. Truth tables.

Bus arbitration

Left port		Right port		Flags (see notes)		Function
$\overline{CE}_L$	$A_{0L} – A_{10L}$	$\overline{CE}_R$	$A_{0R} – A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No contention
L	Any	H	X	H	H	No contention
H	X	L	Any	H	H	No contention
L	$\neq A_{0R} – A_{10R}$	L	$\neq A_{0L} – A_{10L}$	H	H	No contention
Address arbitration with $\overline{CE}$ low before address match						
L	LV5R	L	LV5R	H	L	Left-port wins
L	RV5L	L	RV5L	L	H	Right-port wins
L	Same	L	Same	H	L	Arbitration resolved
L	Same	L	Same	L	H	Arbitration resolved
$\overline{CE}$ arbitration with address match before $\overline{CE}$						
LL5R	$= A_{0R} – A_{10R}$	LL5R	$= A_{0L} – A_{10L}$	H	L	Left-port wins
RL5L	$= A_{0R} – A_{10R}$	RL5L	$= A_{0L} – A_{10L}$	L	H	Right-port wins
LW5R	$= A_{0R} – A_{10R}$	LW5R	$= A_{0L} – A_{10L}$	H	L	Arbitration resolved
LW5R	$= A_{0R} – A_{10R}$	LW5R	$= A_{0L} – A_{10L}$	L	H	Arbitration resolved

NOTES:
1. X = Don't care, L = Low, H = High.
2. LV5R = Left address valid $\geq$ 5 ns before right address.
3. RV5L = Right address valid $\geq$ 5 ns before left address.
4. Same = Left and right addresses match within 5 ns of each other.
5. LL5R = Left $\overline{CE}$ = Low $\geq$ 5 ns before left $\overline{CE}$.
6. RL5L = Right $\overline{CE}$ = Low $\geq$ 5 ns before left $\overline{CE}$.
7. LW5R = Left and right $\overline{CE}$ = Low within 5 ns of each other.

FIGURE 3. Truth tables – continued.



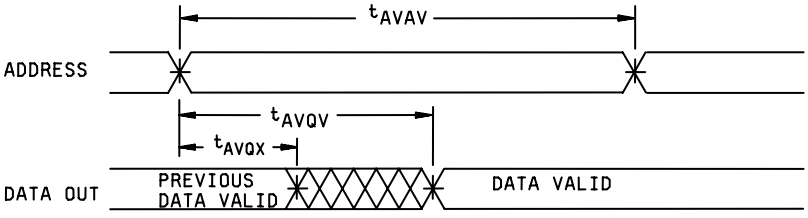
NOTES:
1. Capacitance includes scope and jig (minimum values).
2. Circuit C is used only for $\overline{\text{BUSY}}$ and $\overline{\text{INT}}$ loads for devices 01-03 and 07-09.

AC test conditions

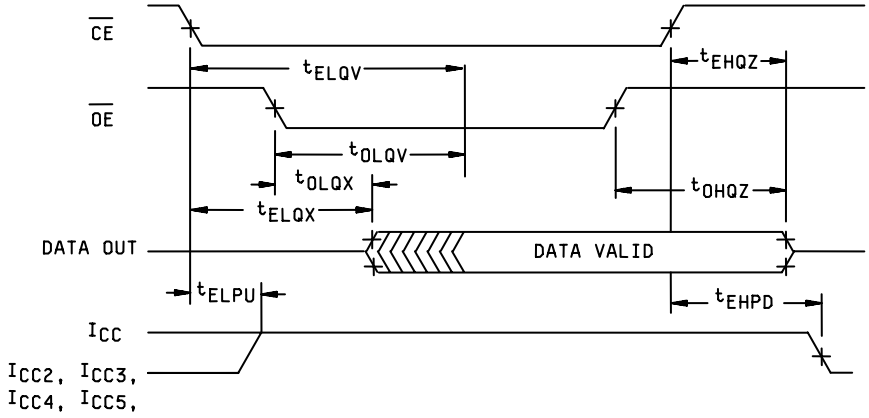
Input pulse levels	GND to 3.0 V
Input rise and fall times (t_r, t_f)	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 4. Output load circuit and test conditions.

Read cycle number 1 either port (see notes 1 and 2)



Read cycle number 2 either port (see notes 1 and 3)



Read cycle number 3 read with $\overline{BUSY}$ (see note 2) - master devices only

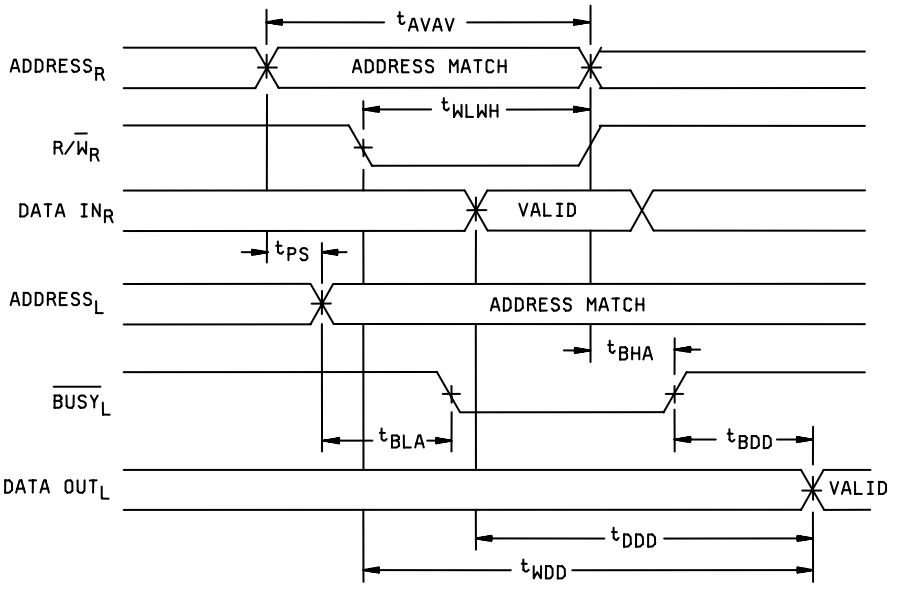
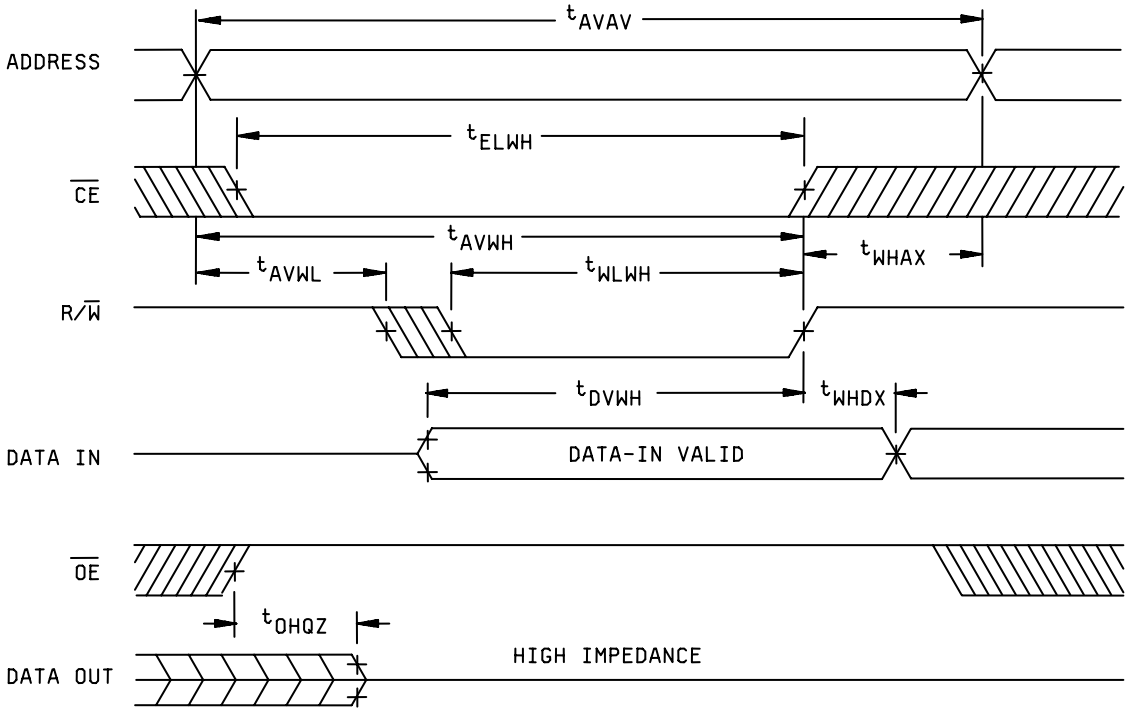


FIGURE 5. Timing waveforms.

Write cycle number 1 either port (see notes 4, 5, 6, and 7)



Write cycle number 2 either port (see notes 4, 5, 6, and 7)

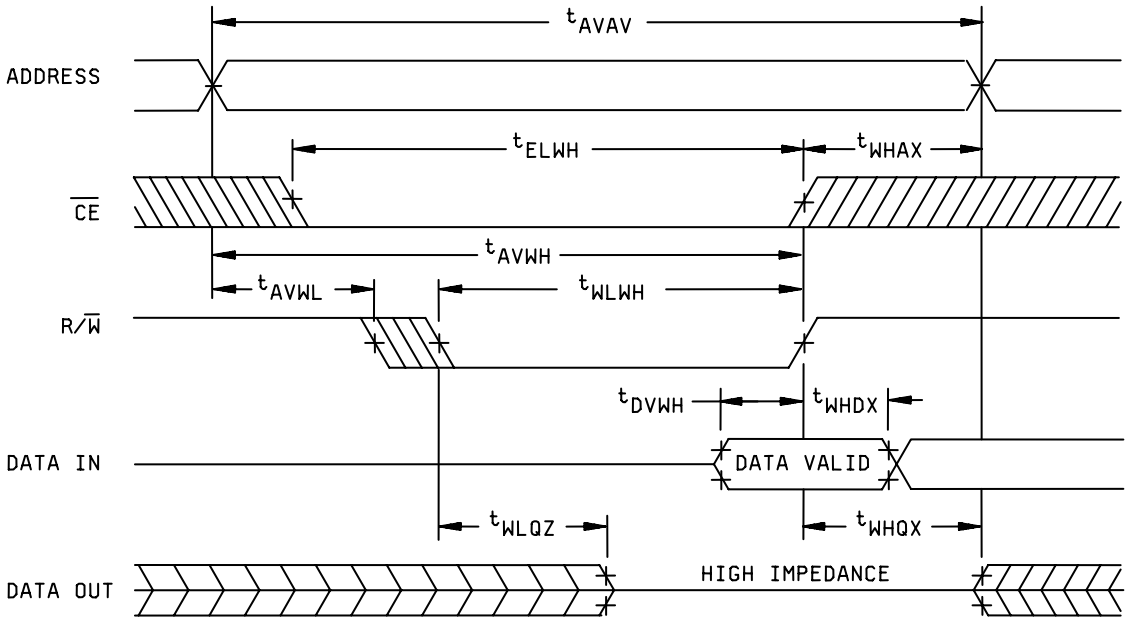
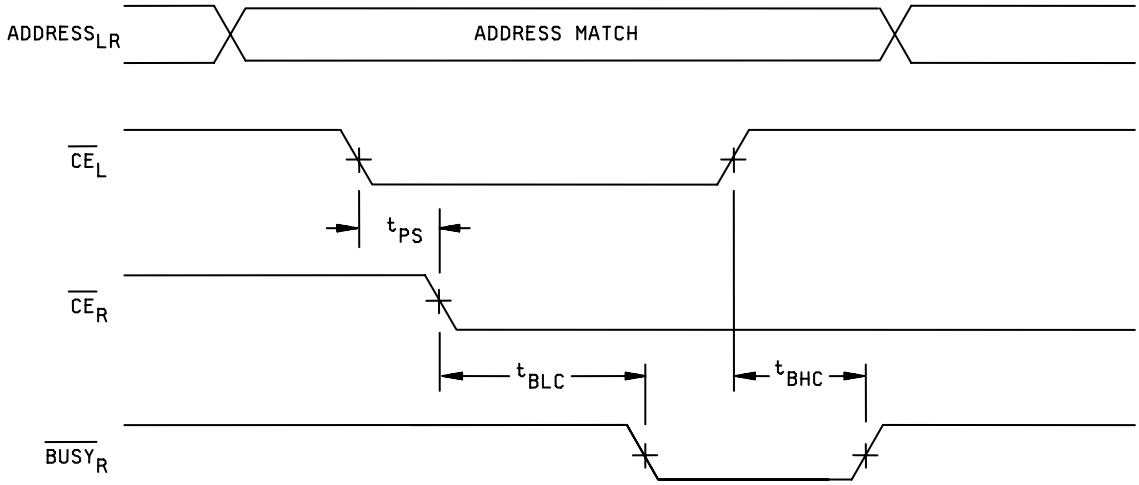


FIGURE 5. Timing waveforms - Continued.

Busy timing number 1 ($\overline{CE}$ arbitration) - master devices only

$\overline{CE}_L$ valid first:



$\overline{CE}_R$ valid first:

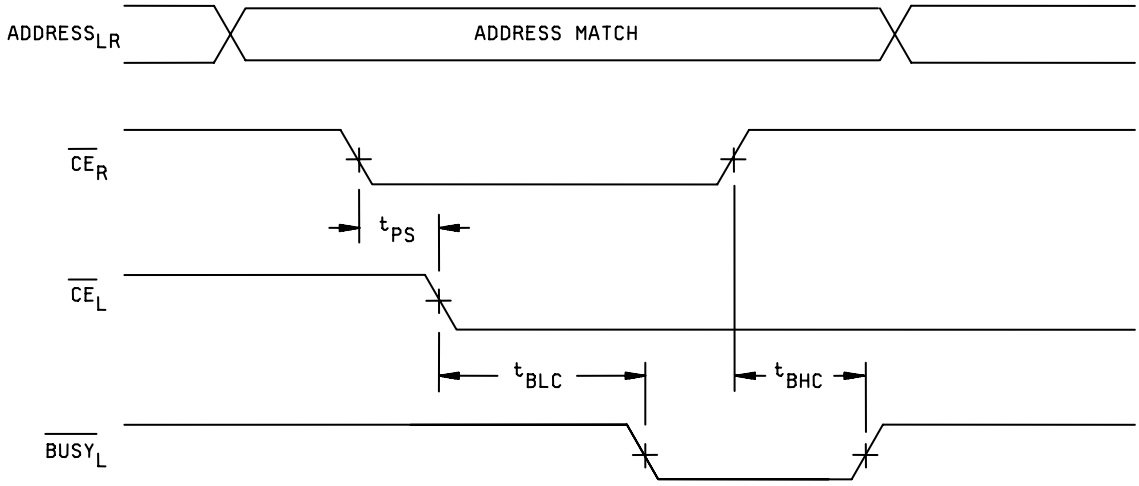
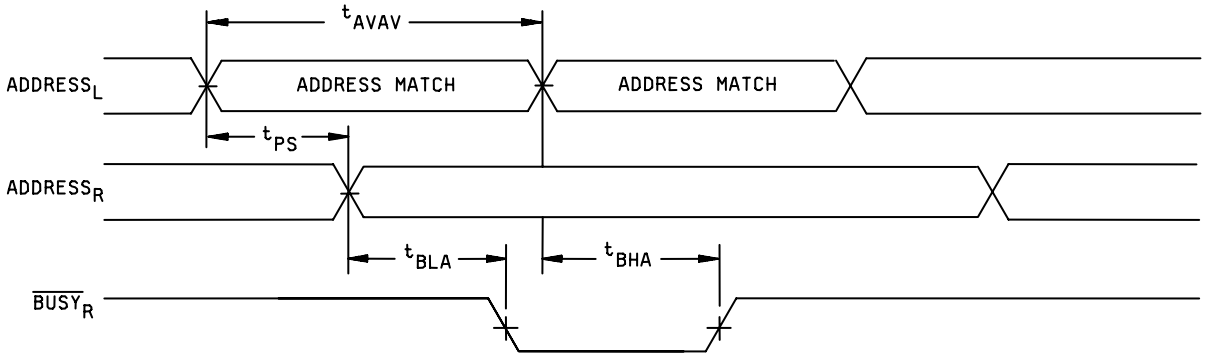


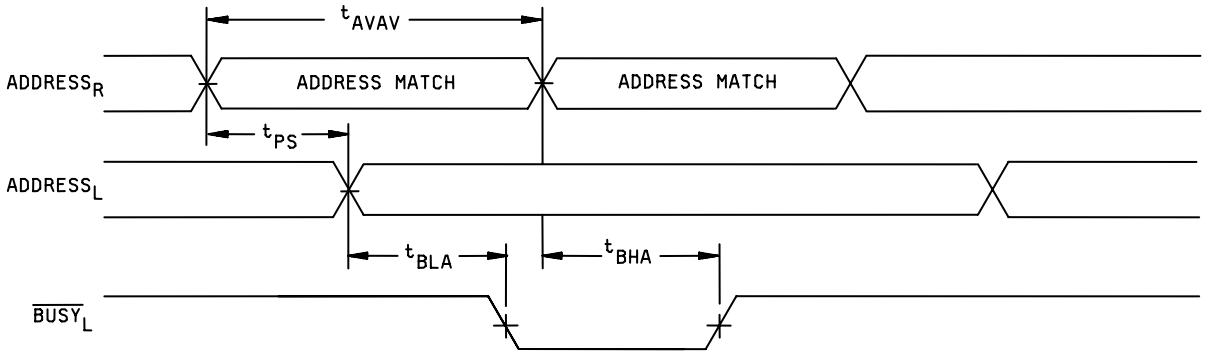
FIGURE 5. Timing waveforms - Continued.

Busy timing number 2 (address arbitration) - master devices only

Left address valid first



Right address valid first



Busy timing number 3 (Write with $\overline{BUSY}$) - slave devices only

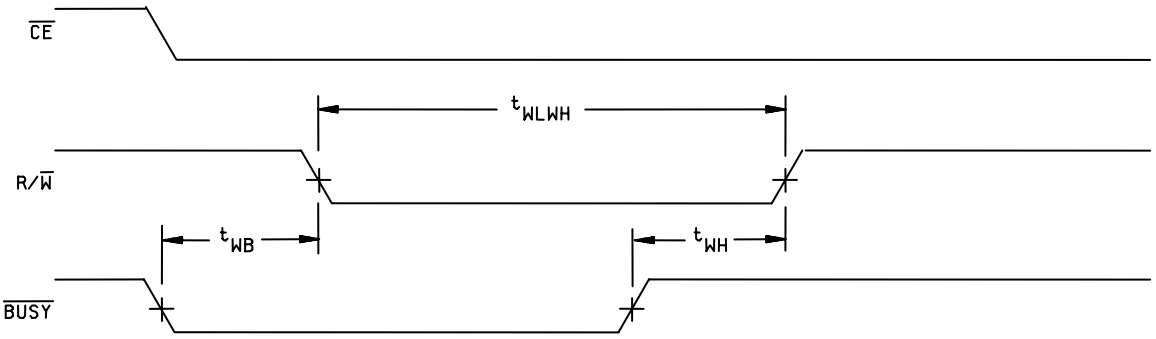
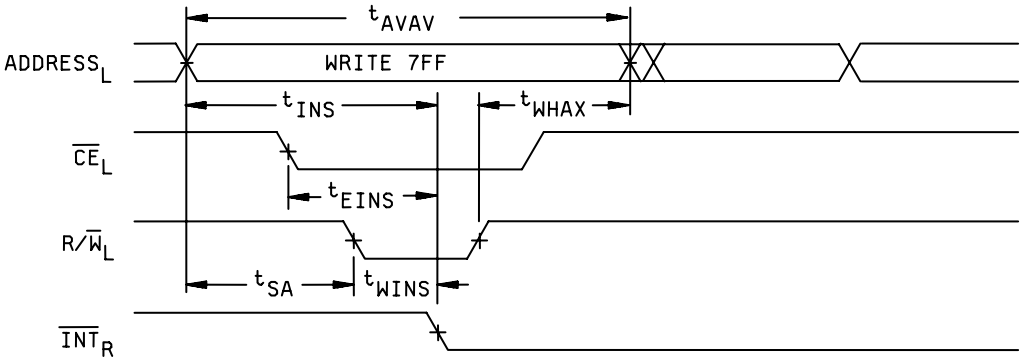


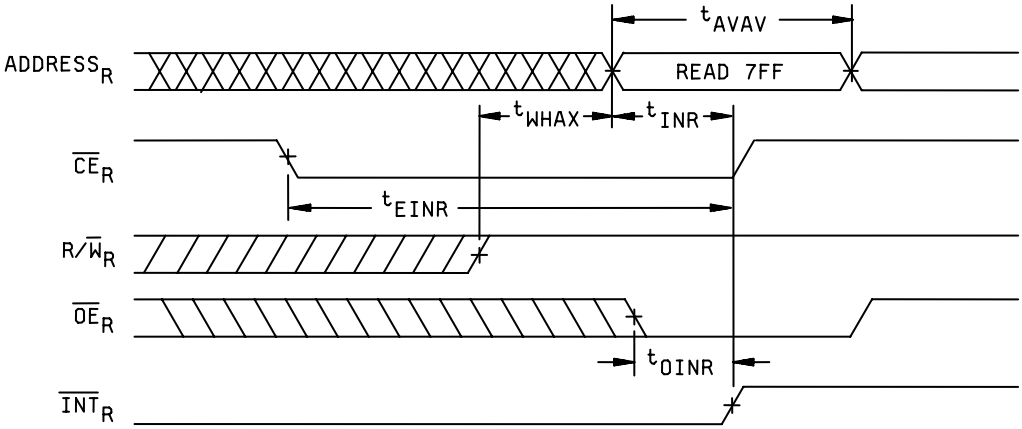
FIGURE 5. Timing waveforms - Continued.

Interrupt timing (device types 07 - 12)

Left side sets $\overline{INT}_R$:



Right side clears $\overline{INT}_R$:



Right side sets $\overline{INT}_L$:

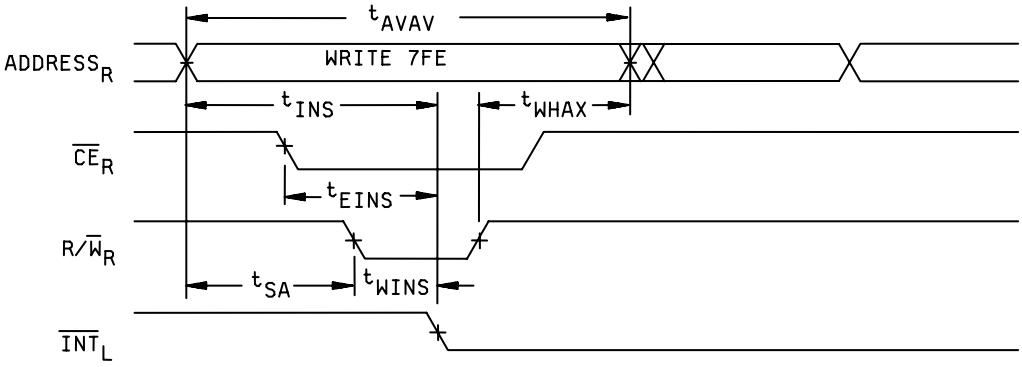
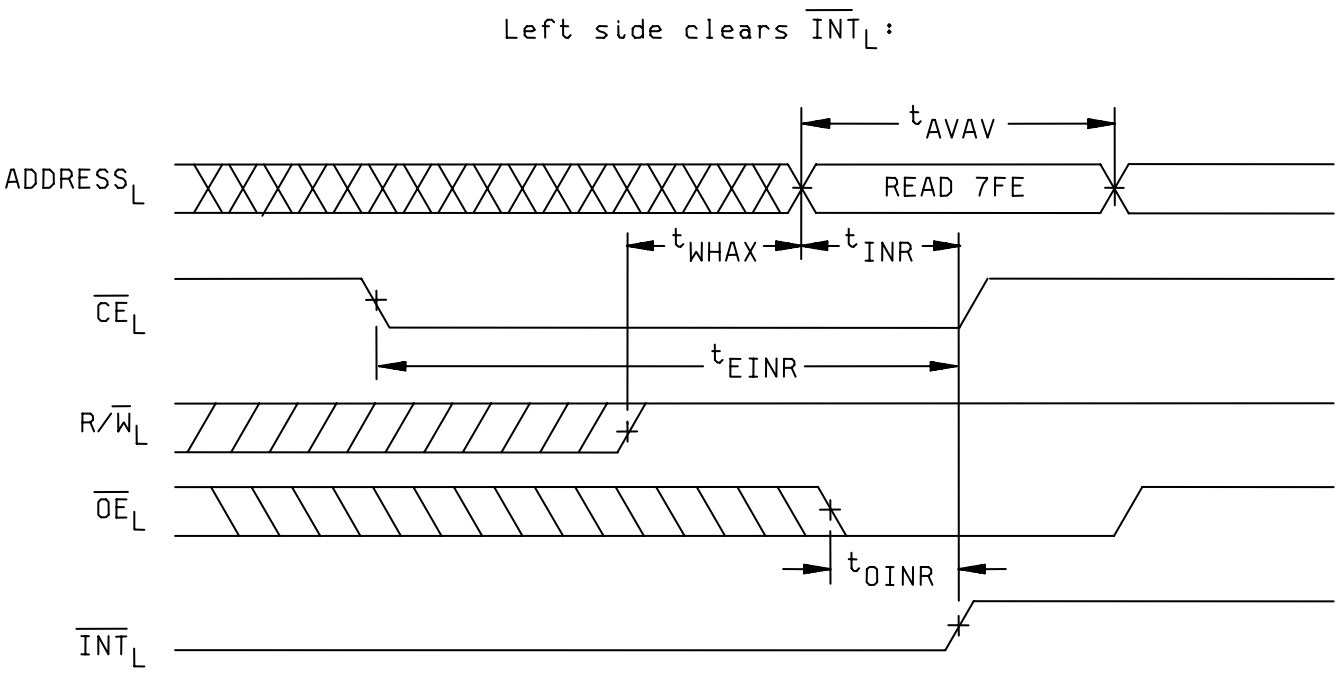


FIGURE 5. Timing waveforms - Continued.



NOTES:

1. R/$\overline{W}$ is high for read cycle.
2. For read cycles no. 1 and no. 3, device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
3. For read cycle no. 2, addresses are valid prior to or coincident with $\overline{CE}$ transition low.
4. A write occurs during the overlap of $\overline{CE}$ low and R/$\overline{W}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WLWH} or t_{WLQZ} + t_{DVWH} to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{DVWH}.
6. If $\overline{CE}$ switches low coincident with or after R/$\overline{W}$ switches low, the outputs will stay in a high impedance state.

FIGURE 5. Timing waveforms - Continued.

TABLE IIB. Delta limits at +25°C.

Test 1/	Device types
	All
I_{CC4} standby	±10% of specified value in table I
I_{IX}, I_{OZ}	±10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7, 8A, and 8B tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

(a) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(b) T_A = +125°C, minimum.

(c) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and herein:

C_{IN} and C_{OUT} ..... Input and bidirectional output, terminal-to-GND capacitance.
GND ..... Ground zero voltage potential.
I_{CC} ..... Supply current.
T_C ..... Case temperature.
T_A ..... Ambient temperature.
V_{CC} ..... Positive supply voltage.
O/V ..... Latch-up over-voltage
O/I ..... Latch-up over-current

6.5.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transitions. Thus the format is:

t X X X X

Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

a. Signal definitions:

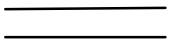
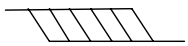
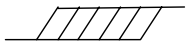
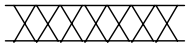
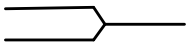
A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable
O = Output enable

b. Transition definitions:

H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)

6.5.2 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.3 Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

APPENDIX A
FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

A.3.2 Algorithm B (pattern 2).

A.3.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for, each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14 Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially, for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-04-04

Approved sources of supply for SMD 5962-90620 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9062001MUA	0C7V7	CY7C132-55FMB
5962-9062001MZA	0C7V7	CY7C132-55LMB
5962-9062001MYA	0C7V7	CY7C132-55DMB
5962-9062002MUA	0C7V7	CY7C132-45FMB
5962-9062002MZA	0C7V7	CY7C132-45LMB
5962-9062002MYA	0C7V7	CY7C132-45DMB
5962-9062003MUA	0C7V7	CY7C132-35FMB
5962-9062003MZA	0C7V7	CY7C132-35LMB
5962-9062003MYA	0C7V7	CY7C132-35DMB
5962-9062004MUA	3/	CY7C142-55FMB
5962-9062004MZA	3/	CY7C142-55LMB
5962-9062004MYA	3/	CY7C142-55DMB
5962-9062005MUA	3/	CY7C142-45FMB
5962-9062005MZA	3/	CY7C142-45LMB
5962-9062005MYA	3/	CY7C142-45DMB
5962-9062006MUA	3/	CY7C142-35FMB
5962-9062006MZA	3/	CY7C142-35LMB
5962-9062006MYA	3/	CY7C142-35DMB
5962-9062007MXA	0C7V7	CY7C136-55LMB
5962-9062008MXA	0C7V7	CY7C136-45LMB
5962-9062009MXA	0C7V7	CY7C136-35LMB
5962-90620010MXA	3/	CY7C146-55LMB
5962-90620011MXA	3/	CY7C146-45LMB
5962-90620012MXA	3/	CY7C146-35LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Ct. Santa Clara, CA 95051-0812

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