REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing converted to new format. Change to table I. Add RHA data. Editorial changes throughout.	93-02-08	Monica L. Poelking
B	Add section 1.5, radiation features. Update the boilerplate in accordance with MIL-PRF-38535 requirements. Editorial changes throughout. – TVN	04-11-08	Thomas M. Hess
C	Add device type 03. Add device Class V criteria. Add radiation hardened assurance features in section 1.5 and SEP limits in table IB. Update boilerplate paragraphs to the current requirements as specified in MIL-PRF-38535. - jak	10-02-17	Thomas M. Hess

REV																				
SHEET																				
REV	C	C	C	C	C	C	C													
SHEET	15	16	17	18	19	20	21													

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Larry T. Gauder

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Thomas J. Ricciuti

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
92-02-13

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, 8-BIT MAGNITUDE COMPARATOR WITH ENABLE, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
C	**A**	**67268**	**5962-90985**

SHEET 1 OF 20

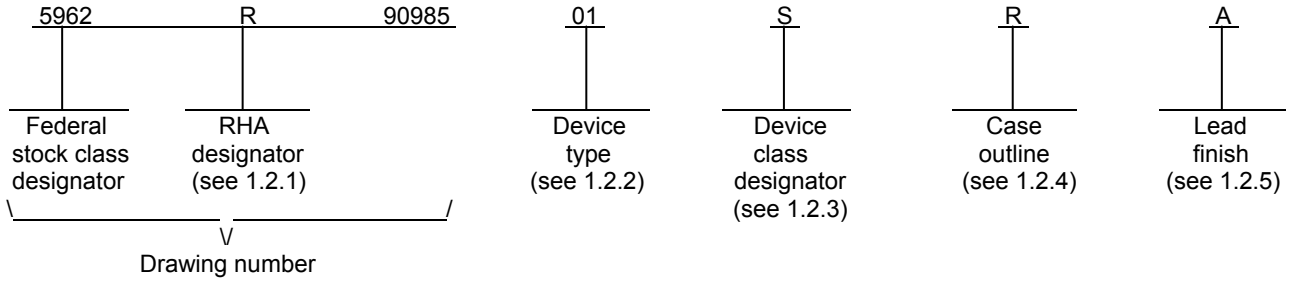
DSCC FORM 2233
APR 97

5962-E141-10

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes B, Q, and M) and space application (device classes S and V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes B, S, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54AC521	8-bit magnitude comparator with enable
02	54AC11521	8-bit magnitude comparator with enable
03	54AC521	Radiation hardened 8-bit magnitude comparator with enable

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
B, S, Q, or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
X	See figure 1	20	Flat pack
2	CQCC1-N20	20	Leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes B, S, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK})	±20 mA
DC output current (I_{OUT})	±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND})	±100 mA
Maximum power dissipation (P_D)	500 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	175°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+3.0 V dc to +5.5 V dc
Input voltage range (V_{IN})	0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	0.0 V dc to V_{CC}
Minimum high level input voltage (V_{IH}):	
V_{CC} = 3.0 V	2.10 V
V_{CC} = 4.5 V	3.15 V
V_{CC} = 5.5 V	3.85 V
Maximum low level input voltage (V_{IL}):	
V_{CC} = 3.0 V	0.90 V
V_{CC} = 4.5 V	1.35 V
V_{CC} = 5.5 V	1.65 V
Maximum high level output current (I_{OH}):	
V_{CC} = 3.0 V	-4 mA
V_{CC} = 4.5 V	-24 mA
Maximum low level output current (I_{OL}):	
V_{CC} = 3.0 V	+12 mA
V_{CC} = 4.5 V	+24 mA
Maximum input rise or fall time rate ($\Delta t/\Delta v$):	
V_{CC} = 3.6 V, V_{CC} = 5.5 V	8 ns/V
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Radiation features.

Device type 01:

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	≥ 100 krads (Si)
Single event phenomenon (SEP) effective:	
linear energy threshold (LET) no upsets (see 4.4.5.4)	≤ 100 MeV-cm^2/mg

Device type 03:

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	≥ 300 krads (Si)
Single event phenomenon (SEP) effective:	
linear energy threshold (LET) no upsets (see 4.4.5.4)	≤ 110 MeV–cm^2/mg

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
2/ Unless otherwise specified, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

EIA/JEDEC Standard No. 78 - IC Latch-up Test

JEDEC Standard No. 20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Copies of these documents are available online at http://www.jedec.org or from Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834.)

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes B, S, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes B, S, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes B, S, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes B, S, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes B, S, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 39 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
High level output voltage 3006	V_{OH1} 5/	For all inputs affecting output under test, V_{IN} = 2.10 V or 0.90 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OH} = -50 µA	All All	3.0 V	1, 2, 3	2.9		V
	V_{OH2} 5/	For all inputs affecting output under test, V_{IN} = 3.15 V or 1.35 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OH} = -50 µA	All All	4.5 V	1, 2, 3	4.4		V
	V_{OH3} 6/ 7/	For all inputs affecting output under test, V_{IN} = 3.85 V or 1.65 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OH} = -50 µA	All All	5.5 V	1, 2, 3	5.4		V
	V_{OH4} 5/	For all inputs affecting output under test, V_{IN} = 2.10 V or 0.90 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OH} = -4 mA	01, 02 All	3.0 V	1, 2, 3	2.4		V
			03 All	3.0 V	1	2.56		V
			03 All	3.0 V	2, 3	2.4		V
	V_{OH5} 6/ 7/	For all inputs affecting output under test, V_{IN} = 3.15 V or 1.35 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OH} = -24 mA	01, 02 All	4.5 V	1, 2, 3	3.7		V
			03 All	4.5 V	1	3.86		V
			03 All	4.5 V	2, 3	3.7		V
	V_{OH6} 5/	For all inputs affecting output under test, V_{IN} = 3.85 V or 1.65 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OH} = -24 mA	01, 02 All	5.5 V	1, 2, 3	4.7		V
			03 All	5.5 V	1	4.86		V
			03 All	5.5 V	2, 3	4.7		V
	V_{OH7} 6/ 7/ 8/	For all inputs affecting output under test, V_{IN} = 3.85 V or 1.65 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OH} = -50 mA	All All	5.5 V	1, 2, 3	3.85		V

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
Low level output voltage 3007	V_{OL1} 5/	For all inputs affecting output under test, V_{IN} = 2.10 V or 0.90 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OL} = 50 µA	All All	3.0 V	1, 2, 3		0.1	V
	V_{OL2} 5/	For all inputs affecting output under test, V_{IN} = 3.15 V or 1.35 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OL} = 50 µA	All All	4.5 V	1, 2, 3		0.1	V
	V_{OL3} 6/ 7/	For all inputs affecting output under test, V_{IN} = 3.85 V or 1.65 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OL} = 50 µA	All All	5.5 V	1, 2, 3		0.1	V
	V_{OL4} 5/	For all inputs affecting output under test, V_{IN} = 2.10 V or 0.90 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OL} = 12 mA	01 B, S, Q, V	3.0 V	1, 3		0.4	V
					2		0.5	
			All M		1		0.4	
					2, 3		0.5	
			03 Q, V	3.0 V	1		0.36	V
					2, 3		0.50	
	V_{OL5} 6/ 7/	For all inputs affecting output under test, V_{IN} = 3.15 V or 1.35 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OL} = 24 mA	01 B, S, Q, V	4.5 V	1, 3		0.4	V
					2		0.5	
			All M		1		0.4	
					2, 3		0.5	
			03 Q, V	3.0 V	1		0.36	V
					2, 3		0.50	
	V_{OL6} 5/	For all inputs affecting output under test, V_{IN} = 3.85 V or 1.65 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OL} = 24 mA	01 B, S, Q, V	5.5 V	1, 3		0.4	V
					2		0.5	
			All M		1		0.4	
					2, 3		0.5	
			03 Q, V	3.0 V	1		0.36	V
					2, 3		0.50	
	V_{OL7} 6/ 7/ 8/	For all inputs affecting output under test, V_{IN} = 3.85 V or 1.65 V For all other inputs, $V_{IN} = V_{CC}$ or GND I_{OL} = 50 mA	All All	5.5 V	1, 2, 3		1.65	V

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
							Min	Max	
Positive input clamp voltage 3022	V_{IC+} 6/ 7/	For input under test, I_{IN} = 1.0 mA		01 B, S, Q, V	0.0 V	1	0.4	1.5	V
Negative input clamp voltage 3022	V_{IC-} 6/ 7/	For input under test, I_{IN} = -1.0 mA		01 B, S, Q, V	Open	1	-0.4	-1.5	V
Input current high 3010	I_{IH} 6/ 7/	For input under test, $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND		All B, S, Q, V	5.5 V	1		0.1	µA
						2		1.0	
				All M		1		0.1	
						2, 3		1.0	
Input current low 3009	I_{IL} 6/ 7/	For input under test, V_{IN} = GND For all other inputs, $V_{IN} = V_{CC}$ or GND		All B, S, Q, V	5.5 V	1		-0.1	µA
						2		-1.0	
				All M		1		-0.1	
						2, 3		-1.0	
Quiescent supply current, output high 3005	I_{CCH} 6/ 7/	For all inputs, $V_{IN} = V_{CC}$ or GND		All B, S, Q, V	5.5 V	1		2.0	µA
						2		40.0	
				All M		1		8.0	
						2, 3		160.0	
			M	01 B, S, Q, V		1		15.0	
			D					75.0	
			P, L, R					700.0	
Quiescent supply current, output low 3005	I_{CCL} 6/ 7/	For all inputs, $V_{IN} = V_{CC}$ or GND		All B, S, Q, V	5.5 V	1		2.0	µA
						2		40.0	
				All M		1		8.0	
						2, 3		160.0	
			M	01 B, S, Q, V		1		15.0	
			D					75.0	
			P, L, R					700.0	
Input capacitance 3012	C_{IN}	See 4.4.1c T_C = +25°C		All All	GND	4		10	pF
Power dissipation capacitance	C_{PD} 9/	See 4.4.1c T_C = +25°C		All All	5.0 V	4		75	pF

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
Latch-up input/output over-voltage	I_{CC} (O/V1) 10/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$ $V_{over} = 10.5\ V$	All B, S, Q, V	5.5 V	2		200	mA
Latch-up input/ output positive over-current	I_{CC} (O/I1+) 10/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$ $I_{trigger} = 120\ mA$	All B, S, Q, V	5.5 V	2		200	mA
Latch-up input/ output negative over-current	I_{CC} (O/I1-) 10/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$ $I_{trigger} = -120\ mA$	All B, S, Q, V	5.5 V	2		200	mA
Latch-up supply over-voltage	I_{CC} (O/V2) 10/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$ $V_{over} = 9.0\ V$	All B, S, Q, V	5.5 V	2		100	mA
Truth table test 3014	6/ 7/ 11/	$V_{IL} = 0.45\ V$, $V_{IH} = 2.5\ V$ Verify output V_O	All All	3.0 V	7, 8	L	H	
		$V_{IL} = 0.6\ V$, $V_{IH} = 3.7\ V$ Verify output V_O	All All	4.5 V	7, 8	L	H	
Propagation delay time, An or Bn to output 3003	t_{PLH1}, t_{PHL1} 6/ 7/ 12/ 13/	$C_L = 50\ pF$ minimum $R_L = 500\Omega$ See figure 4	All B, S, Q, V	3.0 V	9, 11	1.0	12.5	ns
					10	1.0	15.0	
			01 M		9	1.0	12.5	
					10, 11	1.0	15.0	
			02 M		9	1.0	16.6	
					10, 11	1.0	20.4	
			03 Q, V		9	1.0	14.0	
					10, 11	1.0	17.5	
		$C_L = 50\ pF$ minimum $R_L = 500\Omega$ See figure 4	All B, S, Q, V	4.5 V	9, 11	1.0	9.0	
					10	1.0	11.0	
			01 M		9	1.0	9.0	
					10, 11	1.0	11.0	
			02 M		9	1.0	11.3	
					10, 11	1.0	14.0	
			03 Q, V		9	1.0	10.5	
					10, 11	1.0	12.5	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and device class	V_{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
Propagation delay time, $I_{A=B}$ to output 3003	t_{PLH2}, t_{PHL2} 6/ 7/ 12/ 13/	C_L = 50 pF minimum R_L = 500Ω See figure 4	All B, S, Q, V	3.0 V	9, 11	1.0	9.0	ns
					10	1.0	10.5	
			01 M		9	1.0	9.0	
					10, 11	1.0	10.5	
			02 M		9	1.0	9.8	
					10, 11	1.0	11.4	
			03 Q, V		9	1.0	14.5	
					10, 11	1.0	17.0	
		C_L = 50 pF minimum R_L = 500Ω See figure 4	All B, S, Q, V	4.5 V	9, 11	1.0	6.5	
					10	1.0	8.0	
			01 M		9	1.0	6.5	
					10, 11	1.0	8.0	
			02 M		9	1.0	7.1	
					10, 11	1.0	8.6	
			03 Q, V		9	1.0	11.0	
					10, 11	1.0	12.5	

1/ For tests not listed in the referenced MIL-STD-883, [e.g. I_{CC} (O/V1)], utilize the general test procedure under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ RHA parts for device type 01 of this drawing have been characterized through all levels M, D, P, L, and R. RHA parts for device type 03 of this drawing have been characterized through all levels M, D, P, L, R, and F of irradiation. However, these devices are only tested at the 'F' level. Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

5/ For device classes B, S, Q, and V, this test is guaranteed, if not tested, to the limits specified in table I.

6/ RHA samples do not have to be tested at -55°C and +125°C prior to irradiation.

7/ When performing post irradiation electrical measurements for any RHA level, T_A = 25°C. Limits shown are guaranteed at T_A = +25°C ±5°C.

TABLE IA. Electrical performance characteristics - Continued.

8/ Transmission driving tests are performed at V_{CC} = 5.5 V dc with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for V_{IN} = 3.85 V or 1.65 V. For device class M, subgroup 1 testing shall be guaranteed if not tested to the limits specified in table I. For radiation hardness assured (RHA) devices, subgroup 1 testing shall be performed.

9/ Power dissipation capacitance (C_{PD}) determines both the no load dynamic power consumption (P_D) and dynamic current consumption (I_S). Where:

$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC}$

For both P_D and I_S, f is the frequency of the input signal and C_L is the external output load capacitance.

10/ See EIA/JEDEC Standard No. 78 for electrically induced latch-up test methods and procedures. The values listed for $I_{trigger}$ and V_{over} are to be accurate within ±5 percent.

11/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. For V_{CC} = 4.5 V, H ≥ 2.5 V, L < 2.5 V; V_{IH} = 3.7 V, V_{IL} = 0.6 V. For device class M at V_{CC} = 4.5 V, the following input values may be used: V_{IH} = 3.78 V, V_{IL} = 0.68 V. For V_{CC} = 3.0 V, H ≥ 1.5 V, L < 1.5 V; V_{IH} = 2.5 V, V_{IL} = 0.45 V. Allowable tolerances in accordance with MIL-STD-883 for the input voltage levels are already incorporated. Tests at V_{CC} = 3.0 V are for RHA specified devices only (T_A = 25°C ±5°C). Functional tests at V_{CC} = 3.0 V are worst case for RHA specified devices. For device classes B, S, Q, and V, non-RHA specified devices, functional tests at V_{CC} = 3.0 V are guaranteed, if not tested.

12/ Device classes B, S, Q, and V are tested at V_{CC} = 4.5 V and T_C = +125°C for sample testing and at V_{CC} = 4.5 V and T_C = +25°C for screening. Other voltages of V_{CC} and temperatures are guaranteed, if not tested (see 4.4.1d).

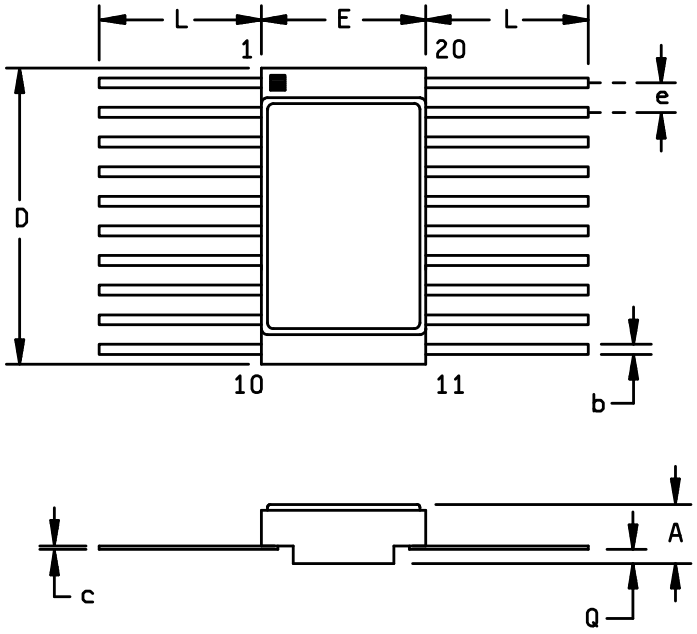
13/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. AC limits at V_{CC} = 3.6 V are equal to the limits at V_{CC} = 3.0 V and guaranteed by testing at V_{CC} = 3.0 V. Minimum AC limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

TABLE IB. SEP test limits. 1/ 2/

Device type	SEP	T_A = temperature ±10°C	V_{CC}	Effective LET
01	SEL	+125°C	3.6 V and 5.5 V	≥ 100 MeV-cm^2/mg
03	SEL	+125°C	3.6 V and 5.5 V	≥ 110 MeV-cm^2/mg

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

Case X



Dimensions				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.045	.085	1.14	2.16
b	.015	.019	0.38	0.48
c	.003	.006	0.076	0.152
D	.505	.515	12.83	13.08
E	.275	.285	6.99	7.24
e	.045	.055	1.14	1.40
L	.250	.370	6.35	9.39
Q	.010	---	0.25	---
N	20		20	

FIGURE 1. Case outlines

Device types	01 and 03	02	
Case outlines	R, S, X, 2	R	2
Terminal number	Terminal symbol	Terminal symbol	Terminal symbol
1	$\overline{I}_{A=B}$	B1	B3
2	A0	A1	A3
3	B0	B0	B2
4	A1	A0	A2
5	B1	GND	$\overline{I}_{A=B}$
6	A2	$\overline{O}_{A=B}$	B1
7	B2	B7	A1
8	A3	A7	B0
9	B3	B6	A0
10	GND	A6	GND
11	A4	B5	$\overline{O}_{A=B}$
12	B4	A5	B7
13	A5	B4	A7
14	B5	A4	B6
15	A6	V_{CC}	A6
16	B6	B3	B5
17	A7	A3	A5
18	B7	B2	B4
19	$\overline{O}_{A=B}$	A2	A4
20	V_{CC}	$\overline{I}_{A=B}$	V_{CC}

FIGURE 1. Terminal connections.

Inputs		Output
$\overline{I}_{A=B}$	An, Bn	$\overline{O}_{A=B}$
L	A = B *	L
L	A ≠ B **	H
H	A = B *	H
H	A ≠ B **	H

H = High voltage level
L = Low voltage level
* All A0 = B0, A1 = B1, …, A7 = B7
** Any A0 ≠ B0, A1 ≠ B1, … A7 ≠ B7

FIGURE 2. Truth table.

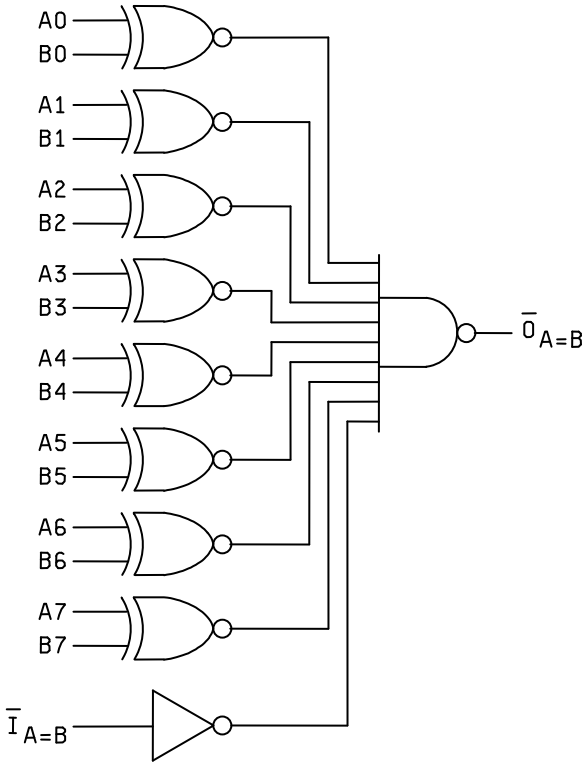
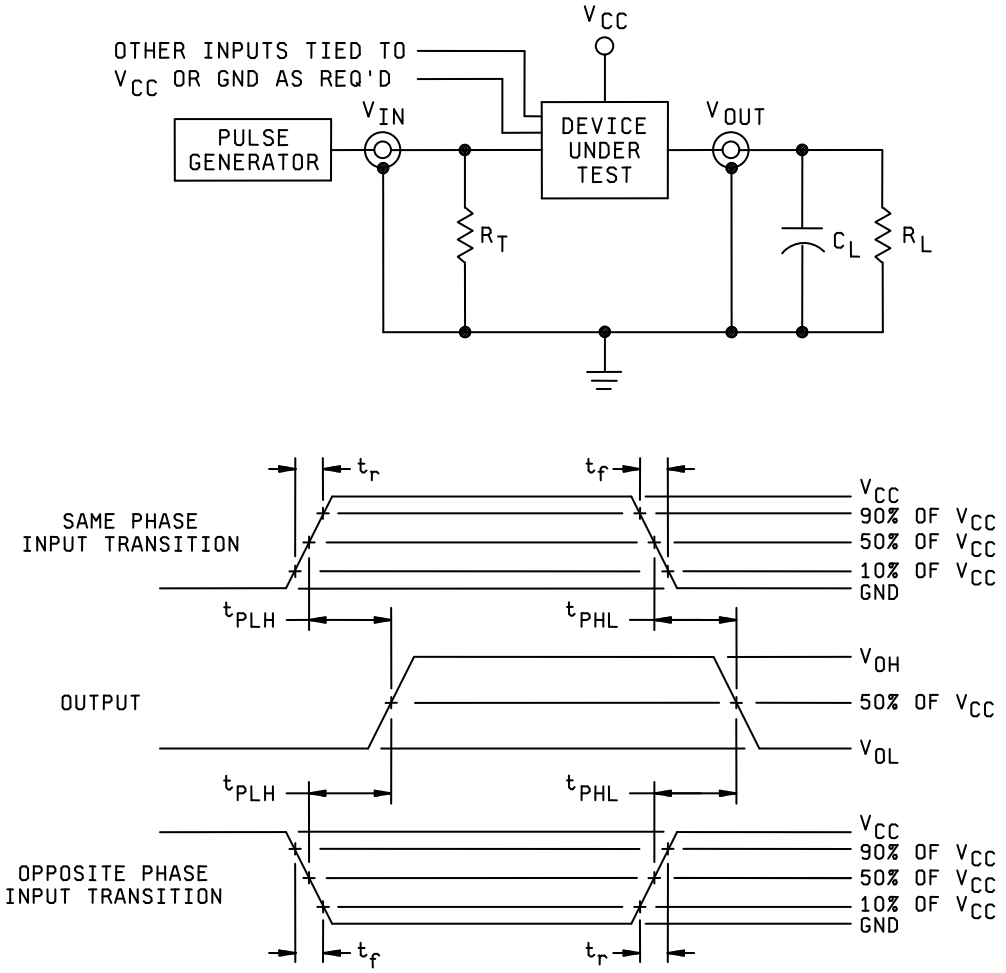


FIGURE 3. Logic diagram.



NOTES:

1. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
2. R_T = 50Ω or equivalent, R_L = 500Ω or equivalent.
3. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 10 MHz; t_r ≤ 3.0 ns; t_f ≤ 3.0 ns; t_r and t_f shall be measured from 10% of V_{CC} to 90% of V_{CC} and from 90% of V_{CC} to 10% of V_{CC}, respectively; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1MHz.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes B, S, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes B, S, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Delete the sequence specified in 3.1.10 through 3.1.14 of method 5004 and substitute the first 7 test requirements of table IIA herein.

(4) For device class M, unless otherwise noted, the requirements for device class B in method 1015 of MIL-STD-883 shall be followed.

(5) Unless otherwise specified in the QM plan for static burn-in, device classes B and S, test condition A, method 1015 of MIL-STD-883, the test duration for each static test shall be 24 hours minimum for class S devices and in accordance with table IA of method 1015 for class B devices.

(a) For static burn-in I, all inputs shall be connected to GND. The output may be open or connected to $V_{CC}/2$ ±0.5 V. Resistors R1 are optional on inputs. A resistor R1 is optional on the output if it is open and required when it is connected to $V_{CC}/2$ ±0.5 V. R1 = 220Ω to 47 kΩ.

(b) For static burn-in II, all inputs shall be connected through the R1 resistors to V_{CC}. The output may be open or connected to $V_{CC}/2$ ±0.5 V. A resistor R1 is optional on the output if it is open and required on the output when it is connected to $V_{CC}/2$ ±0.5 V. R1 = 220Ω to 47 kΩ.

(c) V_{CC} = 5.5 V +0.5 V, -0.00 V.

(6) Unless otherwise specified in the QM plan for dynamic burn-in, device classes B and S, test condition D, method 1015 of MIL-STD-883, the following shall apply:

(a) Input resistors = 220Ω to 2 kΩ ±20 percent.

(b) Output resistors = 220Ω ±20 percent.

(c) V_{CC} = 5.5 V +0.5 V, -0.00 V.

(d) The $\overline{I}_{A=B}$ input pin shall be connected through a resistor in series with GND. The $\overline{O}_{A=B}$ output pin shall be connected through a resistor in series with V_{CC} nominal. The An input pins shall be connected to the resistors in parallel to clock pulse 1 (CP1). The Bn input pins shall be connected to the resistors in parallel to clock pulse 2 (CP2).

(e) CP1 = 25 kHz to 1 MHz square wave; frequency of CP2 = 1/2 frequency of CP1; duty cycle = 50 percent ±15 percent; V_{IH} = 4.5 V to V_{CC}; V_{IL} = 0.0 V ±0.5 V; t_r, t_f ≤ 100 ns.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.2 Additional criteria for device classes B, S, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V or S beyond the requirements of device class Q or B shall be as specified in MIL-PRF-38535, appendix B.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S or V devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. Static burn-in I and II failures shall be cumulative for determining the PDA.

c. The PDA for class B or Q devices shall be in accordance with MIL-PRF-38535 for static burn-in. Dynamic burn-in is not required.

d. The PDA for class M devices shall be in accordance with MIL-PRF-38535, appendix A for static burn-in and dynamic burn-in.

e. Those devices whose measured characteristics, after burn-in, exceed the specified delta limits or electrical parameter limits specified in table I, subgroup I, are defective and shall be removed from the lot. The verified number of failed devices times 100, divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot, and the lot shall be accepted or rejected based on the specified PDA.

4.3 Qualification inspection for device classes B, S, Q, and V. Qualification inspection for device classes B, S, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Technology conformance inspection for classes B, S, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups 1/ (in accordance with MIL-STD-883, method 5005, table I)	Subgroups 1/ (in accordance with MIL-PRF-38535, table III)			
	Device class M	Device class B 2/	Device class S 2/	Device class Q	Device class V
Interim electrical parameters, method 5004		1	1	1	1
Static burn-in I, method 1015 (4.2.1a)	3/	Not required	Required 4/	Not required	Required 4/
Interim electrical parameters, method 5004 (4.2.1b)			1 5/		1 5/
Static burn-in II, method 1015 (4.2.1a)	3/	Required 6/	Required 4/	Required 6/	Required 4/
Interim electrical parameters, method 5004 (4.2.1b)		1 2/ 5/	1 2/ 5/	1 2/ 5/	1 2/ 5/
Dynamic burn-in I, method 1015 (4.2.1a)	3/	Not required	Required 4/	Not required	Required 4/
Interim electrical parameters, method 5004 (4.2.1b)			1 5/		1 5/
Final electrical parameters, method 5004	1, 2, 3, 7, 8, 9 2/	1, 2, 7, 9 2/ 6/	1, 2, 7, 9 2/	1, 2, 3, 7, 8, 9, 10, 11 2/ 6/	1, 2, 3, 7,8, 9, 10, 11 2/
Group A test requirements, method 5005 (4.4.1)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group B end-point electrical parameters, method 5005 (4.4.2)			1, 2, 3, 7, 8, 9, 10, 11 5/		
Group C end-point electrical parameters, method 5005 (4.4.3)	1, 2, 3	1, 2 5/		1, 2, 3 5/	1, 2, 3, 7, 8, 9, 10, 11 5/
Group D end-point electrical parameters, method 5005 (4.4.4)	1, 2, 3	1, 2	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters, method 5005 (4.4.5)	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ PDA applies to subgroup 1 (see 4.2.3). For device classes S and V, PDA applies to subgroups 1 and 7 (see 4.2.3).
3/ The burn-in shall meet the requirements of 4.2.1a herein.
4/ On all class S lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1), in accordance with test method 5004 of MIL-STD-883. For pre-burn-in and interim electrical parameters, the read-and-record requirements are for delta measurements only.
5/ Delta limits shall be required only on table IA, subgroup 1. The delta values shall be computed with reference to the previous interim electrical parameters. The delta limits are specified in table IIB.
6/ The device manufacturer may, at his option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias) or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias). When the manufacturer elects to perform the subgroup 1 electrical parameter measurements without delta measurements, there is no requirement to perform the pre-burn-in electrical tests (first interim electrical parameters test in table IIA).

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameter 1/	Symbol	Device type	Delta limits
Quiescent supply current	I_{CCH}, I_{CCL}	01	±100 nA
Supply current	I_{CCH}, I_{CCL}, I_{CCZ}	03	±300 nA
Input current low level	I_{IL}	03	±20 nA
Input current high level	I_{IH}	03	±20 nA
Output voltage low level (V_{CC} = 5.5 V, I_{OL} = 24 mA)	V_{OL}	03	±0.04 V
Output voltage high level (V_{CC} = 5.5 V, I_{OH} = -24 mA)	V_{OH}	03	±0.20 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determined delta limits.
2/ These parameters shall be recorded before and after the required burn-in and life tests to determine the delta limits.

4.4.1 Group A inspection

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall test all possible input to output combinations. For device classes B, S, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

d. For device classes B, S, Q, and V, subgroups 9 and 11 tests shall be measured only for initial qualifications and after process or design changes which may affect dynamic performance.

e. Latch-up tests are required for device classes B, S, Q, and V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up tests, test all applicable pins on five devices with zero failures.

4.4.2 Group B inspection. When applicable, the group B inspection end-point electrical parameters shall be as specified in table IIA herein. For device class S steady steady-state life tests, the test circuit shall be maintained by the manufacturer and shall be made available to the acquiring or preparing activity upon request.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes B, S, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes B, S, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. RHA tests for device classes M, B, S, Q, and V for levels M, D, P, L, and R shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

d. Prior to irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

4.4.5.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

a. Inputs tested high, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω ±20%, V_{IN} = 5.0 V dc +5%, R_{IN} = 1 kΩ ±20%, and the output is open.

b. Inputs tested low, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω ±20%, V_{IN} = 0.0 V, R_{IN} = 1 kΩ ±20%, and the output is open.

4.4.5.1.1 Accelerated annealing test. Accelerated annealing shall be performed on classes M, B, S, Q, and V devices requiring an RHA level greater than 5K rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.5.2 Dose rate induced latch-up testing. When required by the customer, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.5.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing for class M devices shall be performed at initial qualification and after any design or process changes which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.5.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C. The latchup test temperature shall be at the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes B, S, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes B, S, Q, and V. Sources of supply for device classes B, S, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN
DATE: 10-02-17

Approved sources of supply for SMD 5962-90985 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9098501B2A	0C7V7	JM54AC521B2A
5962-9098501BRA	0C7V7	JM54AC521BRA
5962-9098501BSA	0C7V7	JM54AC521BSA
5962-9098501M2A	0C7V7	54AC521LMQB
5962-9098501MRA	0C7V7	54AC521DMQB
5962-9098501MSA	0C7V7	54AC521FMQB
5962-9098501SRA	3/	54AC521
5962-9098501SSA	3/	54AC521
5962-9098501S2A	3/	54AC521
5962R9098501BRA	3/	JM54AC521BRA-RH
5962R9098501BSA	3/	JM54AC521BSA-RH
5962R9098501B2A	3/	JM54AC521B2A-RH
5962R9098501SRA	3/	JM54AC521SRA-RH
5962R9098501SSA	3/	JM54AC521SSA-RH
5962R9098501S2A	3/	JM54AC521S2A-RH
5962-9098502MRA	3/	54AC11521
5962-9098502M2A	3/	54AC11521
5962F9098503VXA	F8859	RHFAC521K02V
5962F9098503VXC	F8859	RHFAC521K01V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
F8859	ST Microelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2 - FRANCE
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Logic Comparators ***category:***

Click to view products by E2v ***manufacturer:***

Other Similar products are found below :

742450X 74FCT521ATQG LMC7221BIM5X/NOPB SC2903NG M38510/10301BHA 74HC85D.652 74HCT4046AD.112 HEF4046BT.652 HEF4541BT.512 SN74ALS520NSR SN74LS682NSR ADCMP393ARUZ-RL7 74HC280D.652 74HC85DB.118 74HCT9046AD.112 74HC688DB.118 74HCT85D.652 74HC4046AD.652 74HC4046ADB.112 74HC4046APW.112 74HC688PW.112 74HCT85DB.112 CD54HC688F3A AS339GTR-E1 MC33298 74FCT521ATSOG 74FCT521ATSOG8 74FCT521CTQG 74FCT521CTSOG8 74HCT688N 004592X 74HCT85D 74HC688D,652 74HC688DB,118 74HC688PW,112 74HC688PW,118 74HC85D,652 74HC85DB,112 74HC85DB,118 74HC85PW,118 74HC688D 74HCT85D,652 74HCT85D,653 MC14585BDG MC14585BDR2G MC14585BD HA17903APS-E MC3363DW LM239DG4 CD74HCT688MG4