REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R232-94.	94-09-30	Michael A. Frye
B	Update drawing to reflect current requirements. Editorial changes throughout. - gap	01-02-26	Raymond Monnin
C	Boilerplate update and part of five year review. tcr	06-09-26	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C											
SHEET	15	16	17	18	19	20	21	22	23											
REV STATUS	REV						C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET						1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Jeff Bowling

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
93-10-08

MICROCIRCUIT, MEMORY, CMOS, 1K X 9 PARALLEL FIFO, MONOLITHIC SILICON

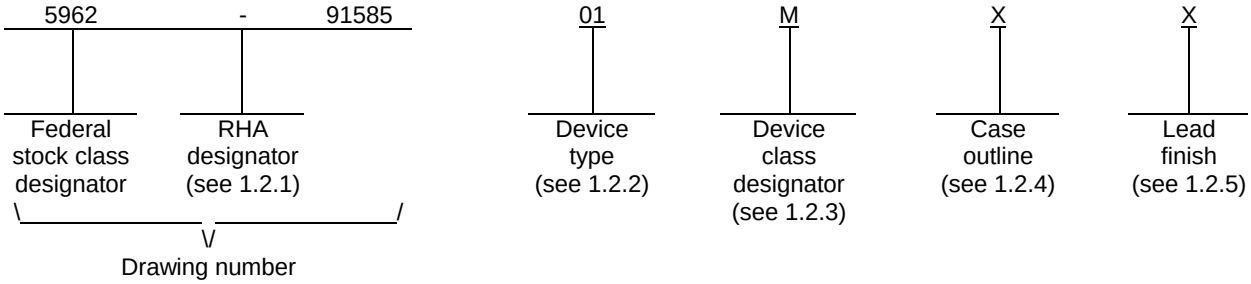
REVISION LEVEL	SIZE	CAGE CODE	
C	A	**67268**	**5962-91585**

SHEET 1 OF 23

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	7202SA	1K X 9 FIFO	120 ns
02	7202SA	1K X 9 FIFO	80 ns
03	7C424, 7C425	1K X 9 FIFO	65 ns
04	7C424, 7C425	1K X 9 FIFO	50 ns
05	7C424, 7C425	1K X 9 FIFO	40 ns
06	7C424, 7C425	1K X 9 FIFO	30 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP3-T28 or GDIP4-T28	28	Dual-in-line package
Y	CDIP2-T28 or GDIP1-T28	28	Dual-in-line package
Z	GDFP2-F28	28	Flat pack
U	CQCC1-N32	32	Rectangular chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC voltage range applied to outputs in High Z state	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to +7.0 V dc
DC output current	20 mA
Maximum power dissipation	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Storage temperature range (T_{STG})	-65°C to +150°C
Temperature under bias	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JEDEC Standard EIA/JESD 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.0 mA $V_{IN} = V_{IH}(Min), V_{IL}(Max)$	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA $V_{IN} = V_{IH}(Min), V_{IL}(Max)$	1, 2, 3	All		0.4	V
Input high voltage	V_{IH} 2/		1, 2, 3	All	2.2		V
Input low voltage	V_{IL} 2/		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{IN} = 5.5 V to GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, $\overline{R} = V_{IH}$, V_{OUT} = 5.5 V and GND	1, 2, 3	All	-10	10	µA
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA $f = 1/t_{RC}$ $\overline{W}$, $\overline{R}$, $D_O - D_8$ pins are toggling between 0 V and 3 V $\overline{FF}$, $\overline{XO}/\overline{HF}$ = 0 mA $Q_0 - Q_8$ = 0 mA $\overline{MR}$, $\overline{FL}/\overline{FT}$ = 3.0 V	1, 2, 3	01-04		115	mA
				05		130	
				06		140	
Standby current	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA All inputs = V_{IH} $\overline{FF}$, $\overline{XO}/\overline{HF}$ = 0 mA $Q_0 - Q_8$ = 0 mA	1, 2, 3	All		30	mA
Power down current	I_{CC3}	V_{CC} = 5.5 V, I_{OUT} = 0 mA All inputs = V_{CC} –0.2 V $\overline{FF}$, $\overline{XO}/\overline{HF}$ = 0 mA $Q_0 - Q_8$ = 0 mA	1, 2, 3	All		25	mA
Input capacitance	C_{IN} 3/	V_{CC} = 5.0 V, V_{IN} = 0 V T_A = +25°C, f = 1 MHz See 4.4.1e	4	All		8	pF
Output capacitance	C_{OUT} 3/	V_{CC} = 5.0 V, V_{OUT} = 0 V T_A = +25°C, f = 1 MHz See 4.4.1e	4	All		12	pF
Functional tests		See 4.4.1c	7, 8A, 8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle time	t_{RC}	See figure 4	9, 10, 11	01	140		ns
				02	100		
				03	80		
				04	65		
				05	50		
				06	40		
Access time	t_A		9, 10, 11	01		120	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		30	
Read recovery time	t_{RR}		9, 10, 11	01, 02	20		ns
				03, 04	15		
				05, 06	10		
Read pulse width 4/	t_{PR}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		
Read low to low Z 3/, 5/	t_{LZR}		9, 10, 11	All	3		ns
Read high to data valid 6/	t_{DVR}		9, 10, 11	All	3		ns
Read high to high Z 3/, 5/, 6/	t_{HZR}		9, 10, 11	01		35	ns
				02-04		30	
				05		25	
				06		20	
Write cycle time	t_{WC}		9, 10, 11	01	140		ns
				02	100		
				03	80		
				04	65		
				05	50		
				06	40		
Write pulse width 4/	t_{PW}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write high to low Z 3/, 5/, 7/	t_{HWZ}	See figure 4	9, 10, 11	All	10		ns
Write recovery time	t_{WR}		9, 10, 11	01, 02	20		ns
				03, 04	15		
				05, 06	10		
Data setup time	t_{SD}		9, 10, 11	01, 02	40		ns
				03, 04	30		
				05	20		
				06	18		
Data hold time	t_{HD}		9, 10, 11	01-03	10		ns
				04	5		
				05, 06	0		
Master reset cycle time	t_{MRSC}		9, 10, 11	01	140		ns
				02	100		
				03	80		
				04	65		
				05	50		
				06	40		
Master reset pulse width 4/	t_{PMR}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		
Master reset recovery time	t_{RMR}		9, 10, 11	01, 02	20		ns
				03, 04	15		
				05, 06	10		
Read high to master reset high 8/	t_{RPW}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		
Write high to master reset high 8/	t_{WPW}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		
Retransmit cycle time	t_{RTC}		9, 10, 11	01	140		ns
				02	100		
				03	80		
				04	65		
				05	50		
				06	40		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Retransmit pulse width 4/	t_{PRT}	See figure 4	9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		
Retransmit recovery time	t_{RTR}		9, 10, 11	01, 02	20		ns
				03, 04	15		
				05, 06	10		
Master reset to empty flag low	t_{EFL}		9, 10, 11	01		140	ns
				02		100	
				03		80	
				04		65	
				05		50	
				06		40	
Master reset to half-full flag high	t_{HFH}		9, 10, 11	01		140	ns
				02		100	
				03		80	
				04		65	
				05		50	
				06		40	
Master reset to full flag high	t_{FFH}		9, 10, 11	01		140	ns
				02		100	
				03		80	
				04		65	
				05		50	
				06		40	
Read low to empty flag low	t_{REF}		9, 10, 11	01-03		60	ns
				04		45	
				05		35	
				06		30	
Read high to full flag high	t_{RFF}		9, 10, 11	01-03		60	ns
				04		45	
				05		35	
				06		30	
Write high to empty flag high	t_{WEF}		9, 10, 11	01-03		60	ns
				04		45	
				05		35	
				06		30	
Write low to full flag low	t_{WFF}		9, 10, 11	01-03		60	ns
				04		45	
				05		35	
				06		30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write low to half-full flag low	t_{WHF}	See figure 4	9, 10, 11	01		140	ns
				02		100	
				03		80	
				04		65	
				05		50	
				06		40	
Read high to half-full flag high	t_{RHF}		9, 10, 11	01		140	ns
				02		100	
				03		80	
				04		65	
				05		50	
				06		40	
Effective read pulse width after empty flag high	t_{RPE}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		
Effective write pulse width after full flag high	t_{WPF}		9, 10, 11	01	120		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	30		
Expansion out low delay from clock	t_{XOL}		9, 10, 11	01		120	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		30	
Expansion out high delay from clock	t_{XOH}		9, 10, 11	01		120	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		30	

1/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load in figure 3, circuit A, unless otherwise specified.
2/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
4/ Pulse widths less than minimum are not allowed.
5/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input.
6/ Use output load figure 3 (circuit B).
7/ Only applies to read data flow-through mode.
8/ If not tested, these parameter limits shall be guaranteed by design.

Device types	All	
Case outlines	X, Y, Z	U
Terminal number	Terminal symbol	
1	$\overline{W}$	NC
2	D_8	$\overline{W}$
3	D_3	D_8
4	D_2	D_3
5	D_1	D_2
6	D_0	D_1
7	$\overline{XI}$	D_0
8	$\overline{FF}$	$\overline{XI}$
9	Q_0	$\overline{FF}$
10	Q_1	Q_0
11	Q_2	Q_1
12	Q_3	NC
13	Q_8	Q_2
14	GND	Q_3
15	$\overline{R}$	Q_8
16	Q_4	GND
17	Q_5	NC
18	Q_6	$\overline{R}$
19	Q_7	Q_4
20	$\overline{XO}$ / $\overline{HF}$	Q_5
21	$\overline{EF}$	Q_6
22	$\overline{MR}$	Q_7
23	$\overline{FL}$ / $\overline{RT}$	$\overline{XO}$ / $\overline{HF}$
24	D_7	$\overline{EF}$
25	D_6	$\overline{MR}$
26	D_5	$\overline{FL}$ / $\overline{RT}$
27	D_4	NC
28	V_{CC}	D_7
29	---	D_6
30	---	D_5
31	---	D_4
32	---	V_{CC}

NC = no connection

FIGURE 1. Terminal connections.

Reset and retransmit
Single device configuration/width expansion mode

Mode	Inputs			Internal status		Outputs		
	$\overline{MR}$	$\overline{RT}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X	X	X
Read/write	1	1	0	Increment 1/	Increment 1/	X	X	X

1/ Pointer will increment if flag is high.

Reset and first load truth table
Depth expansion/compound expansion mode

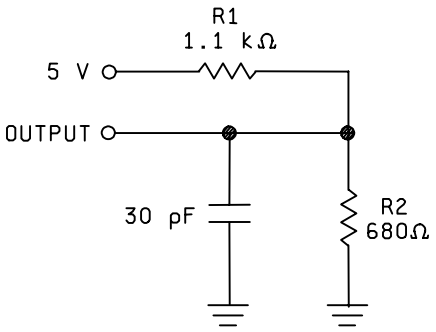
Mode	Inputs			Internal status		Outputs	
	$\overline{MR}$	$\overline{FL}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$
Reset first device	0	0	1/	Location zero	Location zero	0	1
Reset all other devices	0	1	1/	Location zero	Location zero	0	1
Read/write	1	X	1/	X	X	X	X

1/ $\overline{XI}$ is connected to $\overline{XO}$ of previous device.

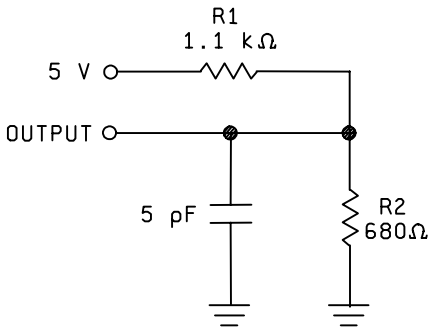
NOTE:

$\overline{MR}$ = Reset input, $\overline{FL}$ / $\overline{RT}$ = First load/retransmit $\overline{EF}$ = Empty flag output,
$\overline{FF}$ = Full flag output, $\overline{XI}$ = Expansion input, and $\overline{HF}$ = Half-full flag output
0 = Low level voltage
1 = High level voltage
X = Don't care

FIGURE 2. Truth table.



Circuit A
Output load



Circuit B
Output load

NOTE: Including scope and jig. (minimum values)

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit and test conditions.

Asynchronous read and write timing diagram

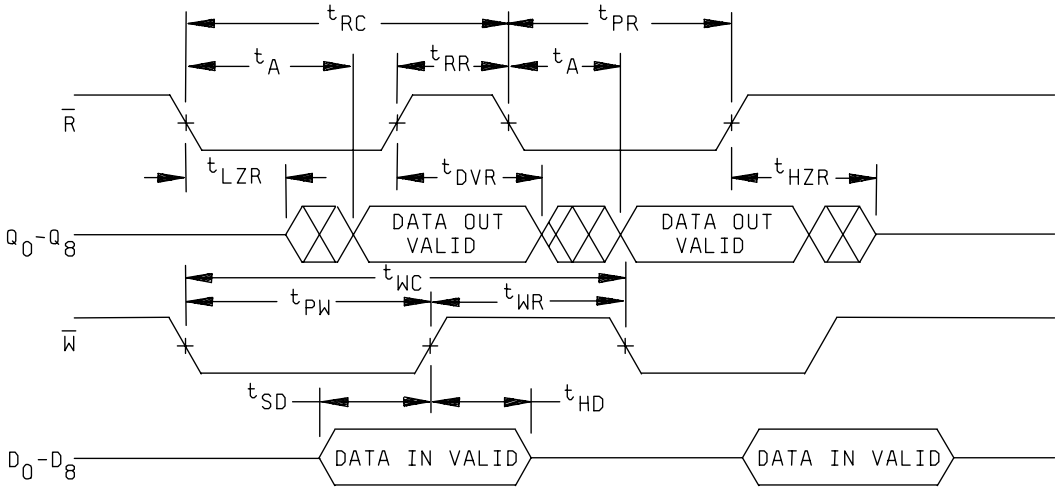
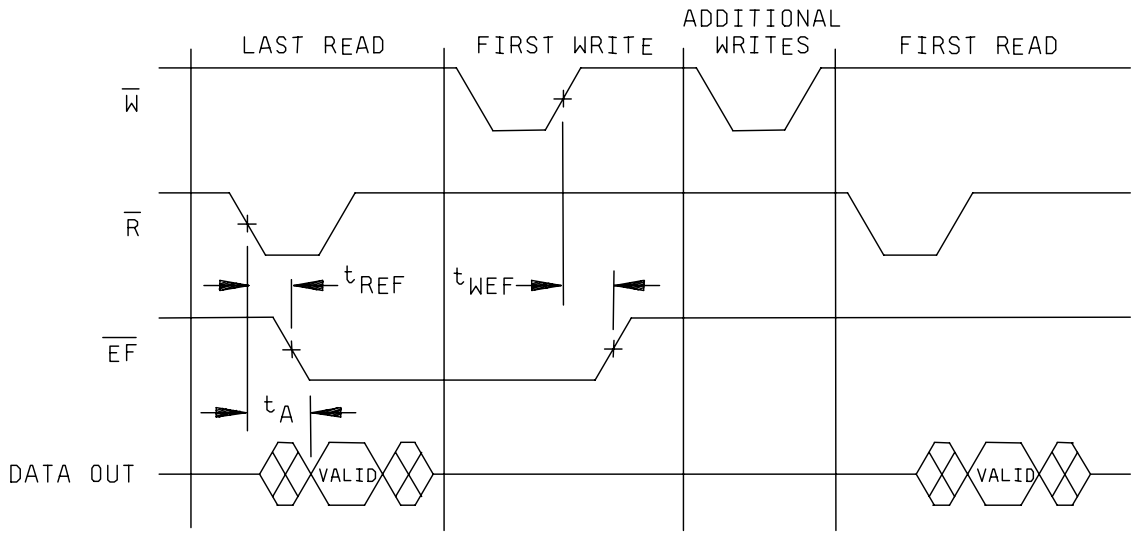
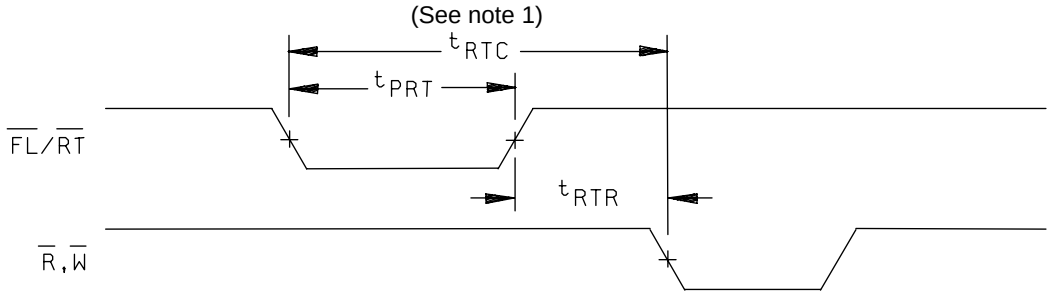


FIGURE 4. Timing waveforms.

Last read to first write empty flag timing diagram



Retransmit timing diagram (See note 2)

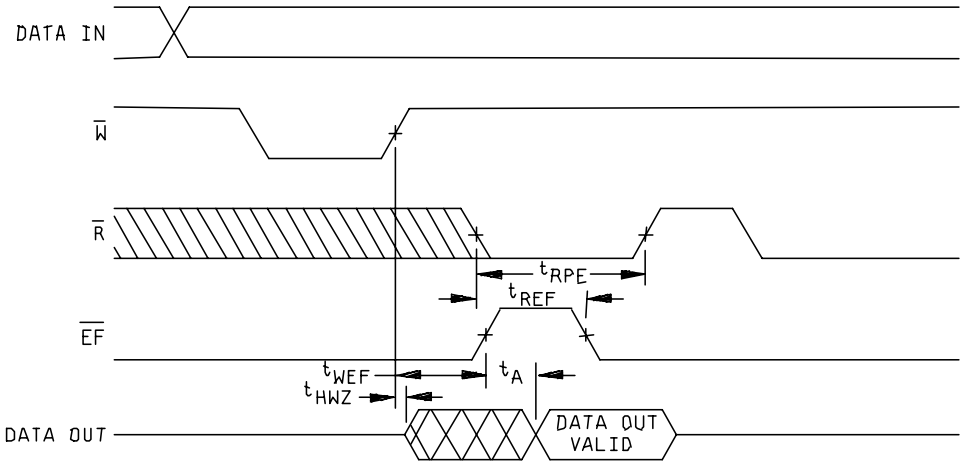


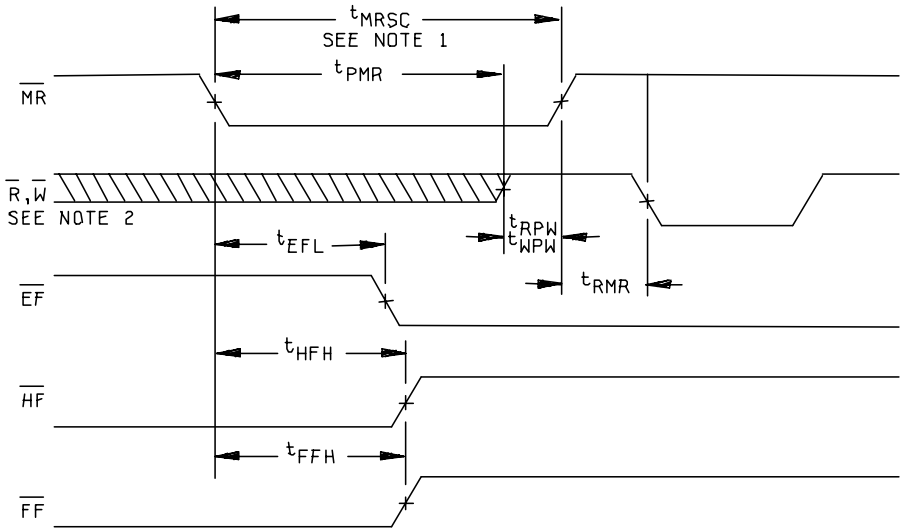
NOTES:

1. $t_{RTC} = t_{PRT} + t_{RTR}$
2. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

FIGURE 4. Timing waveforms – Continued.

Empty flag and read bubble-through mode timing diagram



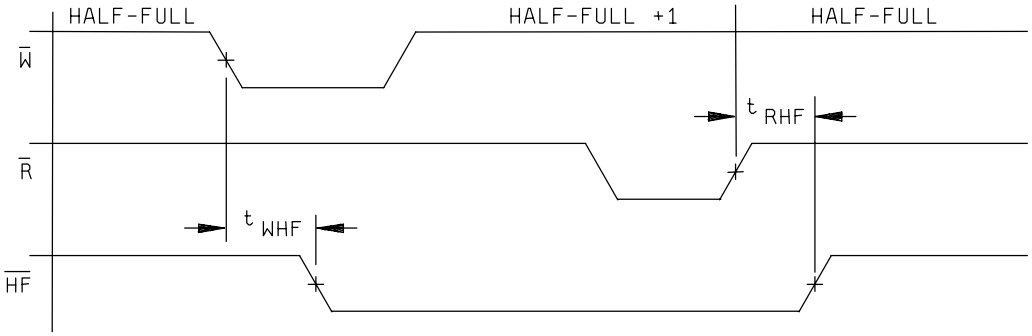


Master reset timing diagram

NOTES:
1. $t_{MRSC} = t_{PMR} + t_{RMR}$
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{MR}$.

FIGURE 4. Timing waveforms – Continued.

Half-full flag timing diagram



Last write to first read full flag timing diagram

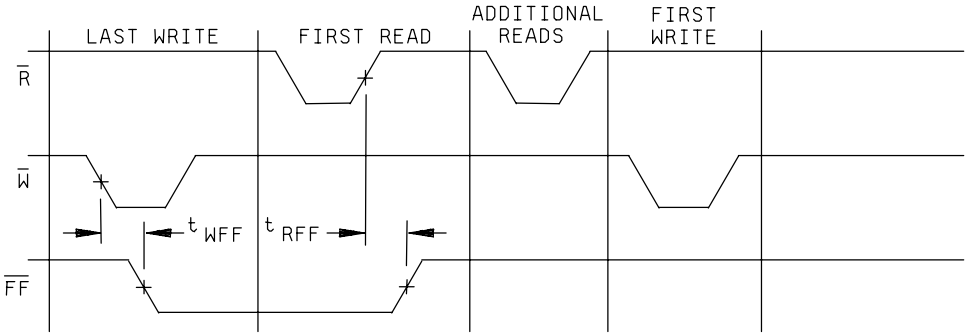


FIGURE 4. Timing waveforms – Continued.

Full flag and write bubble-through mode timing diagram

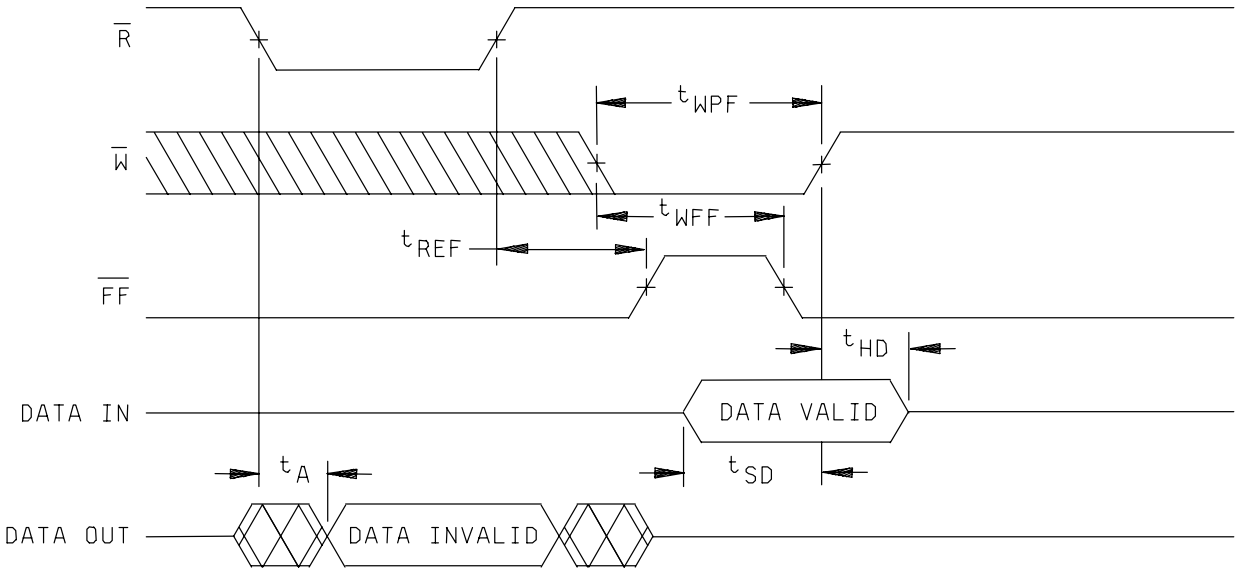
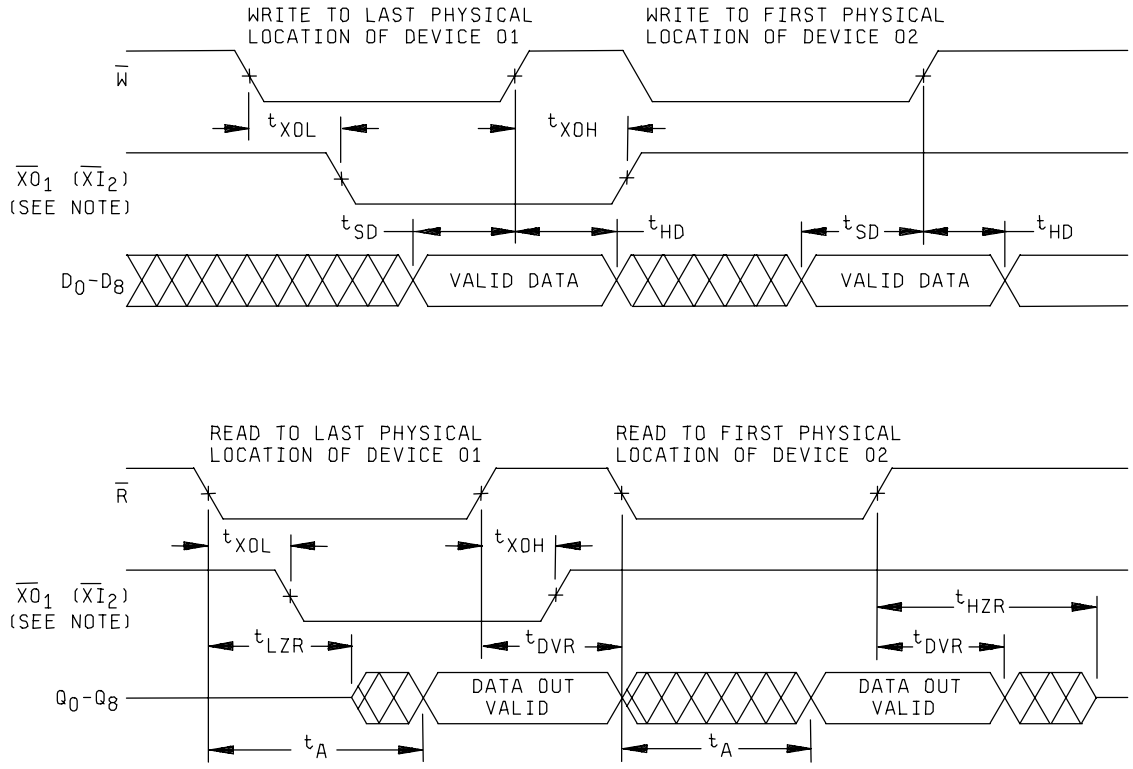


FIGURE 4. Timing waveforms – Continued.

Expansion timing diagrams



NOTE: Expansion out of device 1 ($\overline{XO}_1$) is connected to expansion in of device 2 ($\overline{XI}_2$)

FIGURE 4. Timing waveforms – Continued.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

TABLE IIA. Electrical test requirements. 1/, 2/, 3/, 4/, 5/

Line No.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (per MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
2	Static burn-in I and II method 1015	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B
10	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ * indicates PDA applies to subgroup 1 and 7.
4/ ** see 4.4.1e.
5/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (line 1).

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{IX}	±10 percent of specified value in table I
I_{OZ}	±10 percent of specified value in table I
I_{CC2} standby	±10 percent of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device class Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

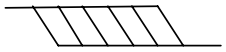
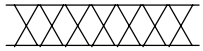
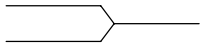
6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

C_{IN} ..... Input terminal capacitance.
C_{OUT} ..... Output and bidirectional output terminal capacitance.
GND ..... Ground zero voltage potential.
I_{CC} ..... Supply current.
I_{IX} ..... Input current.
I_{OZ} ..... Output current.
T_C ..... Case temperature.
V_{CC} ..... Positive supply voltage.

6.5.1 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-09-26

Approved sources of supply for SMD 5962-91585 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9158501MXA	3/	IDT7202SA120TCB
	0C7V7	CY7C425-120DMB
5962-9158501MYA	3/	IDT7202SA120DB
	0C7V7	CY7C424-120DMB
5962-9158501MZA	3/	IDT7202SA120XEB
	0C7V7	CY7C425-120KMB
5962-9158501MUA	3/	IDT7202SA120LB
	0C7V7	CY7C425-120LMB
5962-9158502MXA	3/	IDT7202SA80TCB
	0C7V7	CY7C425-80DMB
5962-9158502MYA	3/	IDT7202SA80DB
	0C7V7	CY7C424-80DMB
5962-9158502MZA	3/	IDT7202SA80XEB
	0C7V7	CY7C425-80KMB
5962-9158502MUA	3/	IDT7202SA80LB
	0C7V7	CY7C425-80LMB
5962-9158503MXA	0C7V7	CY7C425-65DMB
	3/	IDT7202SA65TCB
5962-9158503MYA	3/	IDT7202SA65DB
	0C7V7	CY7C424-65DMB
5962-9158503MZA	3/	IDT7202SA65XEB
	0C7V7	CY7C425-65KMB
5962-9158503MUA	3/	IDT7202SA65LB
	0C7V7	CY7C425-65LMB
5962-9158504MXA	3/	IDT7202SA50TCB
	0C7V7	CY7C425-50DMB
5962-9158504MYA	3/	IDT7202SA50DB
	0C7V7	CY7C424-50DMB
5962-9158504MZA	3/	IDT7202SA50XEB
	0C7V7	CY7C425-50KMB
5962-9158504MUA	3/	IDT7202SA50LB
	0C7V7	CY7C425-50LMB

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9158505MXA	3/	IDT7202SA40TCB
	0C7V7	CY7C425-40DMB
5962-9158505MYA	3/	IDT7202SA40DB
	0C7V7	CY7C424-40DMB
5962-9158505MZA	3/	IDT7202SA40XEB
	0C7V7	CY7C425-40KMB
5962-9158505MUA	3/	IDT7202SA40LB
	0C7V7	CY7C425-40LMB
5962-9158506MXA	0C7V7	CY7C425-30DMB
	3/	IDT7202SA30TCB
5962-9158506MYA	3/	IDT7202SA30DB
	0C7V7	CY7C424-30DMB
5962-9158506MZA	3/	IDT7202SA30XEB
	0C7V7	CY7C425-30KMB
5962-9158506MUA	0C7V7	CY7C425-30LMB
	3/	IDT7202SA30LB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

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