| | | REVISIONS | | |
|---|---|---|---|---|
| LTR | DESCRIPTION | | DATE (YR-MO-DA) | APPROVED |
| A | Changes IAW NOR 5962-R075-94 – jak. | | 93-12-22 | Monica L. Poelking |
| B | Changes IAW NOR 5962-R129-94 -tvn. | | 94-03-21 | Monica L. Poelking |
| C | Changes IAW NOR 5962-R224-96 -bjm. | | 96-09-30 | Thomas M. Hess |
| D | Incorporate NORs, notice of revisions, into the drawing.  Update the boilerplate to the current requirements of MIL-PRF-38535.  -  jak | | 08-01-28 | Thomas M. Hess |
| E | Add footnote $\underline{8}$/ to $I_{CC}$ in table I. - jak | | 10-03-22 | Muhammad A. Akbar |

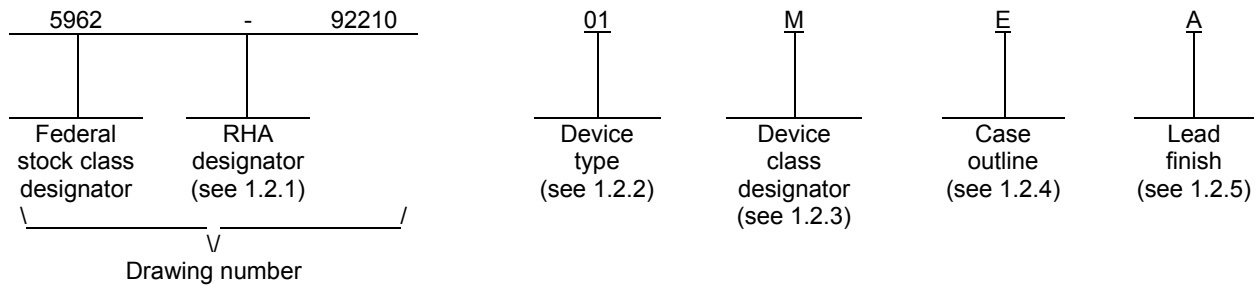| REV | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SHEET | | | | | | | | | | | | | | | | | | | |
| REV | E | E | E | E | E | | | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | 18 | 19 | | | | | | | | | | | | | | |

| REV STATUS | | REV | E | E | E | E | E | E | E | E | E | E | E | E | E | E |
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| OF SHEETS | | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 |

| PMIC N/A | PREPARED BY<br><br>Jeffery Tunstall | **DEFENSE SUPPLY CENTER COLUMBUS**<br>**COLUMBUS, OHIO  43218-3990**<br>**http://www.dscc.dla.mil** | | |
|---|---|---|---|---|
| **STANDARD MICROCIRCUIT DRAWING** | CHECKED BY<br><br>Thomas J. Ricciuti | | | |
| THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS<br><br>AND AGENCIES OF THE DEPARTMENT OF DEFENSE | APPROVED BY<br><br>Monica L. Poelking | MICROCIRCUIT, DIGITAL, FAST CMOS, 4-BIT PRESETTABLE BINARY COUNTER WITH SYNCHRONOUS RESET, TTL COMPATIBLE INPUTS AND LIMITED OUTPUT VOLTAGE SWING, MONOLITHIC SILICON | | |
| | DRAWING APPROVAL DATE<br>93-09-27 | | | |
| AMSC N/A | REVISION LEVEL<br><br>E | SIZE<br>**A** | CAGE CODE<br>**67268** | **5962-92210** |
| | | SHEET<br><br>1   OF   19 | | |

1. SCOPE

1.1 <u>Scope</u>.  This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V).  A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN).  When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 <u>PIN</u>.  The PIN is as shown in the following example:

```
   5962        -      92210         01            M              E            A
```

| Federal stock class designator | RHA designator (see 1.2.1) | Device type (see 1.2.2) | Device class designator (see 1.2.3) | Case outline (see 1.2.4) | Lead finish (see 1.2.5) |

```
      _____/
                   V
           Drawing number
```

1.2.1 <u>RHA designator</u>.  Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator.  Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator.  A dash (-) indicates a non-RHA device.

1.2.2 <u>Device type(s)</u>.  The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01, 02 | 54FCT163T | 4-bit presettable binary counters with synchronous reset, TTL compatible inputs and limited output voltage swing |
| 03, 04 | 54FCT163AT | 4-bit presettable binary counters with synchronous reset, TTL compatible inputs and limited output voltage swing |
| 05, 06 | 54FCT163CT | 4-bit presettable binary counters with synchronous reset, TTL compatible inputs and limited output voltage swing |

1.2.3 <u>Device class designator</u>.  The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 <u>Case outline(s)</u>.  The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| E | GDIP1-T16 or CDIP2-T16 | 16 | Dual-in-line |
| F | GDFP2-F16 or CDFP3-F16 | 16 | Flat pack |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |

1.2.5 <u>Lead finish</u>.  The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

| STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 | SIZE **A** | | **5962-92210** |
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1.3  Absolute maximum ratings.  1/ 2/ 3/

    Supply voltage range ($V_{CC}$)................................................................................... -0.5 V dc to +7.0 V dc
    DC input voltage range ($V_{IN}$) ............................................................................ -0.5 V dc to $V_{CC}$ + 0.5 V dc  4/
    DC output voltage range ($V_{OUT}$) ...................................................................... -0.5 V dc to $V_{CC}$ + 0.5 V dc  4/
    Input clamp current ($I_{IK}$) ($V_{IN}$ = -0.5V)............................................................. -20 mA
    Output clamp current ($I_{OK}$) ($V_{OUT}$ = -0.5V and +7.0 V) ........................................ $\pm$20 mA
    DC output source current ($I_{OH}$) per output.......................................................... -30 mA
    DC output sink current ($I_{OL}$) per output.............................................................. +70 mA
    DC $V_{CC}$ current ($I_{CC}$)....................................................................................... $\pm$260 mA
    DC ground current ($I_{GND}$)................................................................................. $\pm$550 mA
    Storage temperature range ($T_{STG}$) ................................................................... -65°C to +150°C
    Case temperature under bias ($T_{BIAS}$) ................................................................ -65°C to +135°C
    Maximum power dissipation ($P_D$) ....................................................................... 500 mW
    Lead temperature (soldering, 10 seconds) ...................................................... +300°C
    Thermal resistance, junction-to-case ($\theta_{JC}$) .......................................................... See MIL-STD-1835
    Junction temperature ($T_J$) ................................................................................. +175°C

1.4  Recommended operating conditions.  2/ 3/

    Supply voltage range ($V_{CC}$)................................................................................... +4.5 V dc to +5.5 V dc
    Input voltage range ($V_{IN}$) ................................................................................... +0.0 V dc to $V_{CC}$
    Output voltage range ($V_{OUT}$) .............................................................................. +0.0 V dc to $V_{CC}$
    Maximum low level input voltage($V_{IL}$)................................................................ 0.8 V
    Maximum high level input voltage ($V_{IH}$)............................................................. 2.7 V
    Case operating temperature range ($T_C$)............................................................. -55°C to +125°C
    Maximum input rise or fall rate ($\Delta t/\Delta V$):
     (from $V_{IN}$ = 0.3 V to 2.7 V, 2.7 V to 0.3 V) .......................................................... 5 ns/V
    Maximum high level output current ($I_{OH}$):
     Device types 01, 03, and 05  .......................................................................... -12 mA
     Device types 02, 04, and 06  .......................................................................... -6 mA
    Maximum low level output current ($I_{OL}$) ............................................................. 32 mA

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1/  Stresses above the absolute maximum rating may cause permanent damage to the device.  Extended operation at the
    maximum levels may degrade performance and affect reliability.
2/  Unless otherwise noted, all voltages are referenced to GND.
3/  The limits for the parameters specified herein shall apply over the full specified $V_{CC}$ range and case temperature range of
    -55°C to +125°C.
4/  For $V_{CC} \geq$ 6.5 V, the upper limit on the range is limited to 7.0 V.

| STANDARD<br>MICROCIRCUIT DRAWING<br>DEFENSE SUPPLY CENTER COLUMBUS<br>COLUMBUS, OHIO 43218-3990 | SIZE<br>**A** | | **5962-92210** |
| --- | --- | --- | --- |
| | | REVISION LEVEL<br>E | SHEET<br>3 |

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535   -  Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883    -    Test Method Standard Microcircuits.
MIL-STD-1835   -    Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103  -    List of Standard Microcircuit Drawings.
MIL-HDBK-780  -    Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the Qualifying Activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device   class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

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|---|---|---|---|
| **STANDARD** **MICROCIRCUIT DRAWING** | **A** | | **5962-92210** |
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3.3  <u>Electrical performance characteristics and postirradiation parameter limits</u>.  Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4  <u>Electrical test requirements</u>.  The electrical test requirements shall be the subgroups specified in table II.  The electrical tests for each subgroup are defined in table I.

3.5  <u>Marking</u>.  The part shall be marked with the PIN listed in 1.2 herein.  In addition, the manufacturer's PIN may also be marked.  For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.  For RHA product using this option, the RHA designator shall still be marked.  Marking for device classes Q and V shall be in accordance with  MIL-PRF-38535.  Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1  <u>Certification/compliance mark</u>.  The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.  The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.  For class Q product built in accordance with A.3.2.2 of MIL-PRF-38535 or other alternative approved by the Qualifying Activity, the "QD" certification mark shall be used in place of the "QML" or "Q" certification mark.

3.6  <u>Certificate of compliance</u>.  For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein).  For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein).  The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7  <u>Certificate of conformance</u>.  A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8  <u>Notification of change for device class M</u>.  For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affect this drawing.

3.9  <u>Verification and review for device class M</u>.  For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation.  Offshore documentation shall be made available onshore at the option of the reviewer.

3.10  <u>Microcircuit group assignment for device class M</u>.  Device class M devices covered by this drawing shall be in microcircuit group number 38 (see MIL-PRF-38535, appendix A).

| STANDARD<br>**MICROCIRCUIT DRAWING**<br>**DEFENSE SUPPLY CENTER COLUMBUS**<br>**COLUMBUS, OHIO 43218-3990** | SIZE<br>**A** | | **5962-92210** |
|---|---|---|---|
| | | REVISION LEVEL<br>E | SHEET<br>5 |

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ $-55°C \leq T_C \leq +125°C$ $+4.5\ V \leq V_{CC} \leq +5.5\ V$ unless otherwise specified | | Device type | $V_{CC}$ | Group A subgroups | Limits 3/ Min | Limits 3/ Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| High level output voltage 3006 | $V_{OH1}$ 4/ | For all inputs affecting output under test $V_{IH} = 2.7\ V$, $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -300\ \mu A\ *--$ | | All | 4.5 V | 1, 2, 3 | 2.7 | $V_{CC}$-0.5 | V |
| | $V_{OH2}$ | For all inputs affecting output under test $V_{IH} = 2.7\ V$, $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND | $I_{OH} = -12\ mA$ | 01, 03, 05 | 4.5 V | 1, 2, 3 | 2.4 | $V_{CC}$-0.5 | |
| | | | $I_{OH} = -6\ mA$ | 02, 04, 06 | 4.5 V | 1, 2, 3 | 2.4 | $V_{CC}$-0.5 | |
| | | | $I_{OH} = -12\ mA$ | | | | 2.0 | $V_{CC}$-0.5 | |
| Low level output voltage 3007 | $V_{OL1}$ 4/ | For all inputs affecting output under test $V_{IH} = 2.7\ V$, $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 300\ \mu A$ | | All | 4.5 V | 1, 2, 3 | | 0.20 | V |
| | $V_{OL2}$ | For all inputs affecting output under test $V_{IH} = 2.7\ V$, $V_{IL} = 0.8\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 32\ mA$ | | | 4.5 V | 1, 2, 3 | | 0.55 | |
| Negative input clamp voltage 3022 | $V_{IC-}$ | For input under test, $I_{IN} = -15\ mA$ | | 01, 03, 05 | 4.5 V | 1, 2, 3 | | -1.3 | V |
| | | For input under test, $I_{IN} = -18\ mA$ | | 02, 04, 06 | | | | -1.2 | |
| Input current high 3010 | $I_{IH}$ | For input under test, $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND | | 01, 03, 05 | 5.5 V | 1, 2 | | +0.1 | μA |
| | | | | | | 3 | | +1.0 | |
| | | | | 02, 04, 06 | | 1, 2 | | +1.0 | |
| | | | | | | 3 | | +5.0 | |
| Input current low 3010 | $I_{IL}$ | For input under test, $V_{IN} = GND$ For all other inputs, $V_{IN} = V_{CC}$ or GND | | 01, 03, 05 | 5.5 V | 1, 2 | | -0.1 | μA |
| | | | | | | 3 | | -1.0 | |
| | | | | 02, 04, 06 | | 1, 2 | | -1.0 | |
| | | | | | | 3 | | -5.0 | |

TABLE I. Electrical performance characteristics.

See footnotes at end of table.

| TABLE I. Electrical performance characteristics – Continued. | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ -55°C ≤ $T_C$ ≤ +125°C +4.5 V ≤ $V_{CC}$ ≤ +5.5 V unless otherwise specified | | Device type | $V_{CC}$ | Group A subgroups | Limits 3/ | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Min | Max | |
| Input capacitance 3012 | $C_{IN}$ 5/ | See 4.4.1c $T_C$ = +25° | | All | GND | 4 | | 10 | pF |
| Output capacitance 3012 | $C_{OUT}$ 5/ | See 4.4.1c $T_C$ = +25° | | All | GND | 4 | | 12 | pF |
| Short circuit output current 3005 | $I_{OS}$ 6/ | For all inputs $V_{IN}$ = $V_{CC}$ or GND $V_{OUT}$ = GND | | All | 5.5 V | 1, 2, 3 | -60 | -225 | mA |
| Dynamic power supply current | $I_{CCD}$ 4/ 7/ | Outputs open | | All | 5.5 V | 4, 5, 6 | | 0.25 | mA/ MHz•Bit |
| Quiescent supply current delta, TTL input levels 3005 | $\Delta I_{CC}$ 9/ | For input under test $V_{IN}$ = $V_{CC}$ – 2.1 V For all other inputs $V_{IN}$ = $V_{CC}$ or GND | | All | 5.5 V | 1, 2, 3 | | 2.0 | mA |
| Quiescent supply current output high 3005 | $I_{CCH}$ | For all other inputs $V_{IN}$ = $V_{CC}$ or GND | | All | 5.5 V | 1, 2, 3 | | 1.5 | mA |
| Quiescent supply current output low 3005 | $I_{CCL}$ | For all other inputs $V_{IN}$ = $V_{CC}$ or GND | | All | 5.5 V | 1, 2, 3 | | 1.5 | mA |
| Total supply current | $I_{CCT}$ 8/ 10/ | Outputs open, Load mode $f_{CP}$ = 10 MHz, 50% duty cycle CEP = CET = $\overline{PE}$ = GND $f_{IN}$ = 5 MHz, 50% duty cycle One bit toggling For nonswitching inputs, $V_{IN}$ = $V_{CC}$ or GND | For switching inputs $V_{IN}$ = $V_{CC}$ or GND | All | 5.5 V | 4, 5, 6 | | 4.0 | mA |
| | | | For switching inputs $V_{IN}$ = 3.4 V or GND | | | 4, 5, 6 | | 6.0 | |
| | | Load mode 4/ $\overline{SR}$ = $V_{CC}$ CEP = CET = $\overline{PE}$ = GND Four bits toggling $f_{IN}$ = 5 MHz, 50% duty cycle For nonswitching inputs, $V_{IN}$ = $V_{CC}$ or GND | For switching inputs $V_{IN}$ = $V_{CC}$ or GND | | | 4, 5, 6 | | 7.8 | |
| | | | For switching inputs $V_{IN}$ = 3.4 V or GND | | | 4, 5, 6 | | 16.8 | |

See footnotes at end of table.

| STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990 | SIZE **A** | | 5962-92210 |
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| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ -55°C ≤ $T_C$ ≤ +125°C +4.5 V ≤ $V_{CC}$ ≤ +5.5 V unless otherwise specified | Device type | $V_{CC}$ | Group A subgroups | Limits 3/ Min | Limits 3/ Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Low level ground bounce noise | $V_{OLP}$ 5/ 10/ | $V_{IH}$ = 3.0 V $V_{IL}$ = 0.0 V $T_A$ = +25°C See figure 4 See 4.4.1d | 01, 03, 05 | 5.0 V | 4 | | | mV |
| | | | 02, 04, 06 | | | | 1500 | |
| Low level ground bounce noise | $V_{OLV}$ 5/ 10/ | | 01, 03, 05 | 5.0 V | 4 | | | mV |
| | | | 02, 04, 06 | | | | -1700 | |
| High level $V_{CC}$ bounce noise | $V_{OHP}$ 5/ 10/ | | 01, 03, 05 | 5.0 V | 4 | | | mV |
| | | | 02, 04, 06 | | | | 700 | |
| High level $V_{CC}$ bounce noise | $V_{OHV}$ 5/ 10/ | | 01, 03, 05 | 5.0 V | 4 | | | mV |
| | | | 02, 04, 06 | | | | -650 | |
| Functional test | 11/ | $V_{IL}$ = 0.8 V $V_{IH}$ = 2.7 V Verify output $V_O$ See 4.4.1b | All | 4.5 V | 7, 8 | L | H | |
| | | $V_{IL}$ = 0.8 V $V_{IH}$ = 2.7 V Verify output $V_O$ See 4.4.1b | All | 5.5 V | 7, 8 | L | H | |
| Propagation delay time, CP to Qn (PE input high) 3003 | $t_{PHL}$ $t_{PLH}$ 12/ | $C_L$ = 50 pF minimum $R_L$ = 500 Ω See figure 5 | 01, 02 | 4.5 V | 9, 10, 11 | 2.0 | 11.5 | ns |
| | | | 03, 04 | | 9, 10, 11 | 2.0 | 7.5 | |
| | | | 05, 06 | | 9, 10, 11 | 2.0 | 6.3 | |
| Propagation delay time, CP to Qn (PE input low) 3003 | $t_{PHL}$ $t_{PLH}$ 12/ | $C_L$ = 50 pF minimum $R_L$ = 500 Ω See figure 5 | 01, 02 | 4.5 V | 9, 10, 11 | 2.0 | 10.0 | ns |
| | | | 03, 04 | | 9, 10, 11 | 2.0 | 6.5 | |
| | | | 05, 06 | | 9, 10, 11 | 2.0 | 6.3 | |
| Propagation delay time, CP to TC 3003 | $t_{PHL}$ $t_{PLH}$ 12/ | $C_L$ = 50 pF minimum $R_L$ = 500 Ω See figure 5 | 01, 02 | 4.5 V | 9, 10, 11 | 2.0 | 16.5 | ns |
| | | | 03, 04 | | 9, 10, 11 | 2.0 | 10.8 | |
| | | | 05, 06 | | 9, 10, 11 | 2.0 | 8.3 | |
| Propagation delay time, CET to TC 3003 | $t_{PHL}$ $t_{PLH}$ 12/ | $C_L$ = 50 pF minimum $R_L$ = 500 Ω See figure 5 | 01, 02 | 4.5 V | 9, 10, 11 | 2.0 | 9.0 | ns |
| | | | 03, 04 | | 9, 10, 11 | 2.0 | 5.9 | |
| | | | 05, 06 | | 9, 10, 11 | 2.0 | 5.6 | |
| Set-up time, high or low, Pn to CP | $t_s$ 12/ | $C_L$ = 50 pF minimum $R_L$ = 500 Ω See figure 5 | 01, 02 | 4.5 V | 9, 10, 11 | 5.5 | | ns |
| | | | 03, 04 | | 9, 10, 11 | 4.5 | | |
| | | | 05, 06 | | 9, 10, 11 | 4.5 | | |

See footnote at end of table.

STANDARD
MICROCIRCUIT DRAWING
DEFENSE SUPPLY CENTER COLUMBUS
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SIZE
A

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DSCC FORM 2234
APR 97

TABLE I.  <u>Electrical performance characteristics</u> - Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ -55°C ≤ $T_C$ ≤ +125°C +4.5 V ≤ $V_{CC}$ ≤ +5.5 V unless otherwise specified | Device type | $V_{CC}$ | Group A subgroups | Limits 3/ Min | Limits 3/ Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Hold time, high or low, Pn from CP | $t_h$ 12/ | $C_L$ = 50 pF minimum $R_L$ = 500 Ω See figure 5 | 01, 02 | 4.5 V | 9, 10, 11 | 2.0 | | ns |
| | | | 03, 04 | | 9, 10, 11 | 2.0 | | |
| | | | 05, 06 | | 9, 10, 11 | 2.0 | | |
| Set-up time, high or low, PE to CP, SR to CP | $t_s$ 12/ | $C_L$ = 50 pF minimum $R_L$ = 500 Ω See figure 5 | 01, 02 | 4.5 V | 9, 10, 11 | 13.5 | | ns |
| | | | 03, 04 | | 9, 10, 11 | 11.5 | | |
| | | | 05, 06 | | 9, 10, 11 | 11.5 | | |
| Hold time, high or low, PE from CP, SR from CP | $t_h$ 12/ | $C_L$ = 50 pF minimum $R_L$ = 500 Ω See figure 5 | 01, 02 | 4.5 V | 9, 10, 11 | 1.5 | | ns |
| | | | 03, 04 | | 9, 10, 11 | 1.5 | | |
| | | | 05, 06 | | 9, 10, 11 | 1.5 | | |
| Set-up time, high or low, CEP to CP, CET to CP | $t_s$ 12/ | $C_L$ = 50 pF minimum $R_L$ = 500 Ω See figure 5 | 01, 02 | 4.5 V | 9, 10, 11 | 13.0 | | ns |
| | | | 03, 04 | | 9, 10, 11 | 11.0 | | |
| | | | 05, 06 | | 9, 10, 11 | 11.0 | | |
| Hold time, high or low, CEP from CP, CET from CP | $t_h$ 12/ | $C_L$ = 50 pF minimum $R_L$ = 500 Ω See figure 5 | 01, 02 | 4.5 V | 9, 10, 11 | 0 | | ns |
| | | | 03, 04 | | 9, 10, 11 | 0 | | |
| | | | 05, 06 | | 9, 10, 11 | 0 | | |
| Clock pulse width, (Load) high or low | $t_w$ 4/ 12/ | $C_L$ = 50 pF minimum $R_L$ = 500 Ω See figure 5 | 01, 02 | 4.5 V | 9, 10, 11 | 5.0 | | ns |
| | | | 03, 04 | | 9, 10, 11 | 4.0 | | |
| | | | 05, 06 | | 9, 10, 11 | 4.0 | | |
| Clock pulse width, (Count) high or low | $t_w$ 12/ | $C_L$ = 50 pF minimum $R_L$ = 500 Ω See figure 5 | 01, 02 | 4.5 V | 9, 10, 11 | 8.0 | | ns |
| | | | 03, 04 | | 9, 10, 11 | 7.0 | | |
| | | | 05, 06 | | 9, 10, 11 | 7.0 | | |

1/  For tests not listed in the referenced MIL-STD-883 (e.g. $\Delta I_{CC}$), utilize the general test procedure of 883 under the conditions listed here in.

2/  Each input/output, as applicable shall be tested at the specified temperature, for the specified limits, to the tests in table I herein.  Output terminals not designated shall be high level logic, low level logic, or open, except for all $I_{CC}$ and $\Delta I_{CC}$ tests, the output terminals shall be open.  When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/  For negative and positive voltage and current values:  The sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.  All devices shall meet or exceed the limits specified in table I at 4.5 V ≤ $V_{CC}$ ≤ 5.5 V.

4/  This parameter is guaranteed, if not tested, to the limits specified in table I.

5/  This test is required only for group A testing, see 4.4.1 herein.

6/  Not more than one output should be shorted at a time.  The duration of the short circuit test should not exceed one second.

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TABLE I.  <u>Electrical performance characteristics</u> - Continued.

7/    $I_{CCD}$ may be verified by the following equation:
$$I_{CCD} = \frac{I_{CCT} - I_{CC} - D_H N_T \Delta I_{CC}}{f_{CP}/2 + f_I N_i}$$

8/    For $I_{CC}$ tests, in an ATE environment, the effect of parasitic output capacitive loading from the test environment must be taken into account, as its effect is not intended to be included in the test results.  The impact must be characterized and appropriate offset factors must be applied to the test result."

   where, $I_{CCT}$, $I_{CC}$ ($I_{CC}$ or $I_{CCH}$ in table I), and $\Delta I_{CC}$ shall be measured values of these parameters, for the device under test, when tested as described in table I, herein.  The values for $D_H$, $N_T$, $f_{CP}$, $f_I$, and $N_I$ shall be as listed in the test conditions column for $I_{CCT}$ in table I, herein.

9/    This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ –2.1 V (alternate method).  Classes Q, and V shall use the preferred method.  When the test is performed using the alternate test method: the maximum limit is equal to the number of inputs at a high TTL input level times 2.0 mA; and the preferred method and limits are guaranteed.

10/   $I_{CCT}$ is calculated as follows:
      $I_{CCT} = I_{CC} + D_H N_T \Delta I_{CC} + I_{CCD}(f_{CP}/2 + f_I N_I)$
      where
            $I_{CC}$ = Quiescent supply current (any $I_{CCL}$ or $I_{CCH}$)
            $D_H$ = Duty cycle for TTL inputs at 3.4 V
            $N_T$ = Number of TTL inputs at 3.4 V
            $\Delta I_{CC}$ = Quiescent supply current delta, TTL inputs at 3.4 V
            $I_{CCD}$ = Dynamic power supply current caused by an input transition pair (HLH or LHL)
            $f_{CP}$ = Clock frequency for registered devices ($f_{CP} = 0$ for nonregistered devices)
            $f_I$ = Input frequency
            $N_I$ = Number on inputs at $f_I$

11/   This test is for qualification only.  Ground and $V_{CC}$ bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs.  The test is performed on a low noise bench test fixture.  For the device under test, all outputs shall be loaded with 500Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 4).  Only chip capacitors and resistors shall be used.  The output load components shall be located as close as possible to the device outputs.  It is suggested, that whenever possible, this distance be kept to less than 0.25 inches.  Decoupling capacitors shall be placed in parallel from $V_{CC}$ to ground.  The values of these decoupling capacitors shall be determined by the device manufacturer.  The low and high level ground and $V_{CC}$ bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

   The device inputs shall be conditioned such that all outputs are at a high nominal $V_{OH}$ level.  The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at $V_{OH}$ as all other outputs possible are switched from $V_{OH}$ to $V_{OL}$. $V_{OHV}$ and $V_{OHP}$ are then measured from the nominal $V_{OH}$ level to the largest negative and positive peaks, respectively (see figure 4).  This is then repeated with the same outputs not under test switching from $V_{OL}$ to $V_{OH.}$

   The device inputs shall be conditioned such that all outputs are at a low nominal $V_{OL}$ level.  The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at $V_{OL}$ as all other outputs possible are switched from $V_{OL}$ to $V_{OH}$. $V_{OLP}$ and $V_{OLV}$ are then measured from the nominal $V_{OL}$ level to the largest positive and negative peaks, respectively (see figure 4).  This is then repeated with the same outputs not under test switching from $V_{OH}$ to $V_{OL.}$

   For device types 01, 03, and 05, the limits for $V_{CC}$ and ground bounce tests were never supplied.  Device types 01, 03, and 05 with $I_{OH}$ = -12 mA were never made available from an approved source of supply.

12/   Tests shall be performed in sequence, attributes data only.  Functional tests shall include the truth table and other logic patterns used for fault detection.  The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output.  All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein.  Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices.   $H \geq 1.5$ V,  $L < 1.5$ V

13/   AC limits at $V_{CC}$ = 5.5 V are equal to the limits at $V_{CC}$ = 4.5 V and guaranteed by testing at $V_{CC}$ = 4.5 V.  Minimum propagation delay time limits for $V_{CC}$ = 4.5 V and 5.5 V are guaranteed, if not tested, to the limits specified in table I, herein.  For propagation delay tests, all paths must be tested.

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| Device type | 01, 02, 03, 04, 05, 06 | |
|---|---|---|
| Case outlines | E, F | 2 |
| Terminal number | Terminal symbol | Terminal symbol |
| 1 | $\overline{SR}$ | NC |
| 2 | CP | $\overline{SR}$ |
| 3 | P0 | CP |
| 4 | P1 | P0 |
| 5 | P2 | P1 |
| 6 | P3 | NC |
| 7 | CEP | P2 |
| 8 | GND | P3 |
| 9 | $\overline{PE}$ | CEP |
| 10 | CET | GND |
| 11 | Q3 | NC |
| 12 | Q2 | $\overline{PE}$ |
| 13 | Q1 | CET |
| 14 | Q0 | Q3 |
| 15 | TC | Q2 |
| 16 | $V_{CC}$ | NC |
| 17 | --- | Q1 |
| 18 | --- | Q0 |
| 19 | --- | TC |
| 20 | --- | $V_{CC}$ |

NC = No connection

| Pin description | |
|---|---|
| Terminal symbol | Description |
| CEP | Count enable parallel input |
| CET | Count enable trickle input |
| CP | Clock enable, timing input, (active rising edge) |
| $\overline{SR}$ | Synchronous reset input (active low) |
| Pn (n = 0 to 3) | Parallel data inputs |
| $\overline{PE}$ | Parallel enable, synchronous input (active low) |
| Qn (n = 0 to 3) | Flip-flop outputs |
| TC | Terminal count output |

FIGURE 1.  Terminal connections.

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| INPUTS | | | | OUTPUTS |
|---|---|---|---|---|
| $\overline{E}$ | S | I0n | I1n | Zn |
| H | X | X | X | L |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | L | X | L |
| L | L | H | X | H |

H = High voltage level
L = Low voltage level
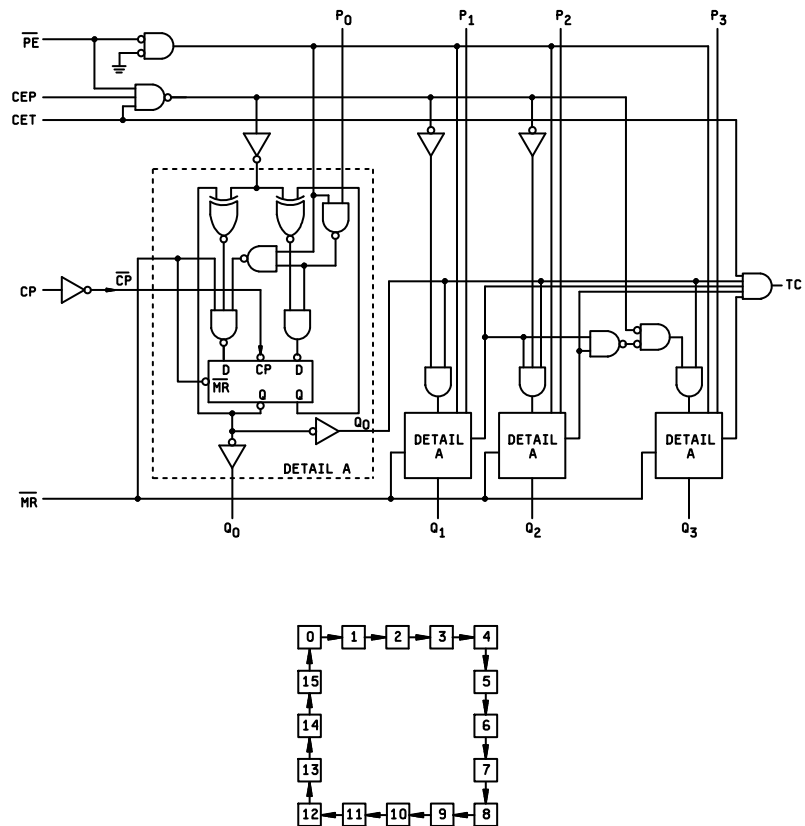X = Irrelevant

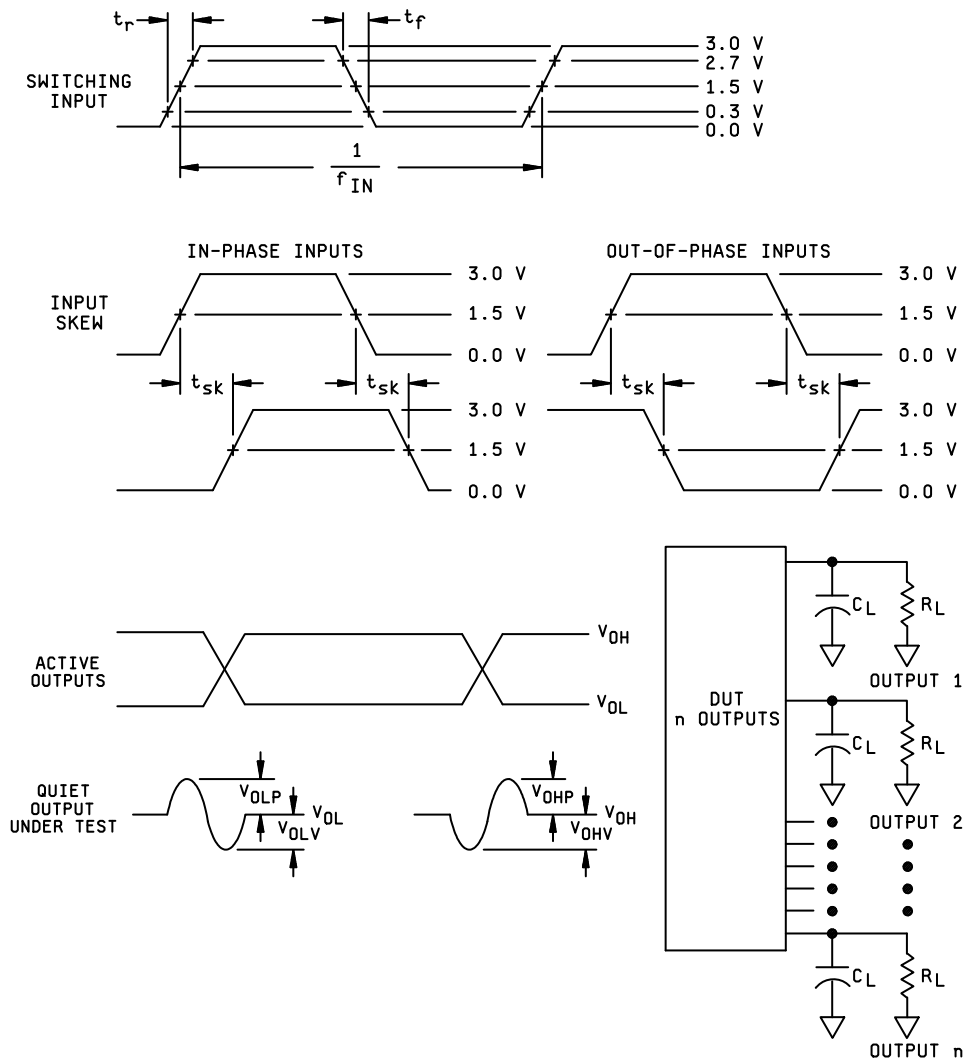FIGURE 2.  Truth table.



FIGURE 3.  Logic diagram.

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NOTES:
1. $C_L$ includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. $R_L$ = 450Ω ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. $V_{IN}$ = 0.0 V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq$ 1 MHz.
   b. $t_r$, $t_f$ = 3.0 ns ±1.0 ns. For input signal generators incapable of maintaining these values of $t_r$ and $t_f$, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns; skew between any two switching inputs signals ($t_{sk}$): ± 250 ps.

FIGURE 4.  Ground bounce test circuit and waveforms.

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DATA INPUT

$t_s$   $t_h$

3.0 V
1.5 V
0.0 V

TIMING INPUT

3.0 V
1.5 V
0.0 V

$t_{rem}$

ASYNCHRONOUS
CONTROL
INPUT

3.0 V
1.5 V
0.0 V

$t_s$   $t_h$

SYNCHRONOUS
CONTROL
INPUT

3.0 V
1.5 V
0.0 V

$t_W$

INPUT PULSE WIDTH
HIGH AND LOW

3.0 V
1.5 V
0.0 V

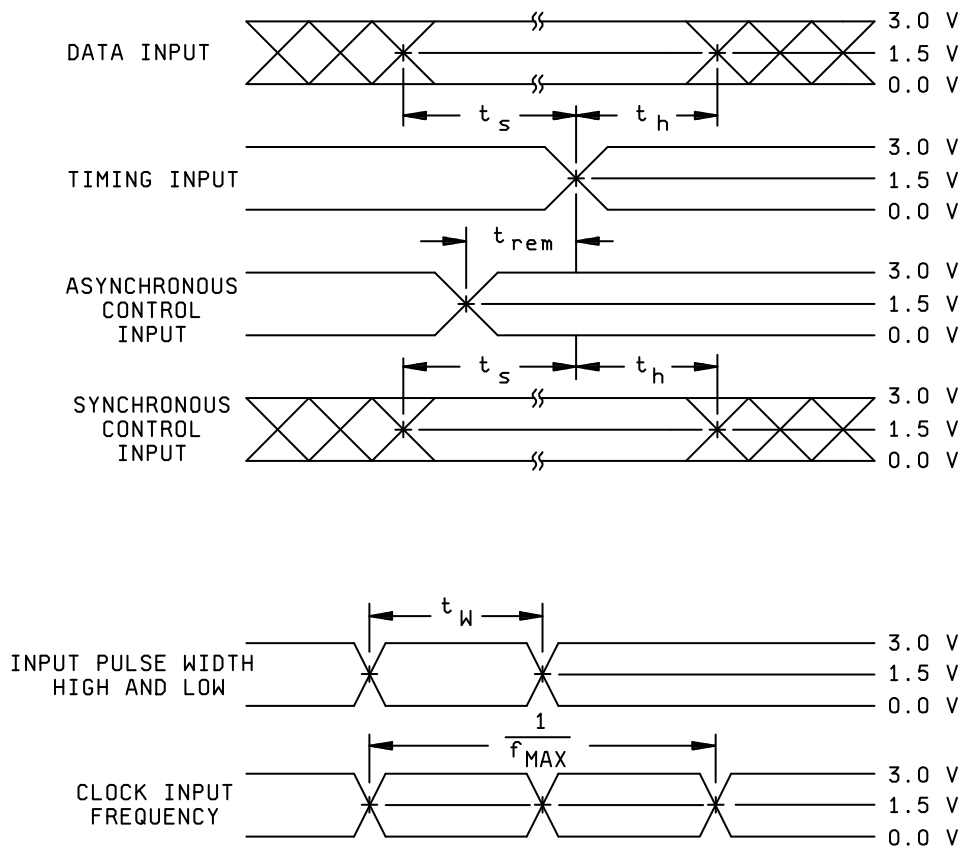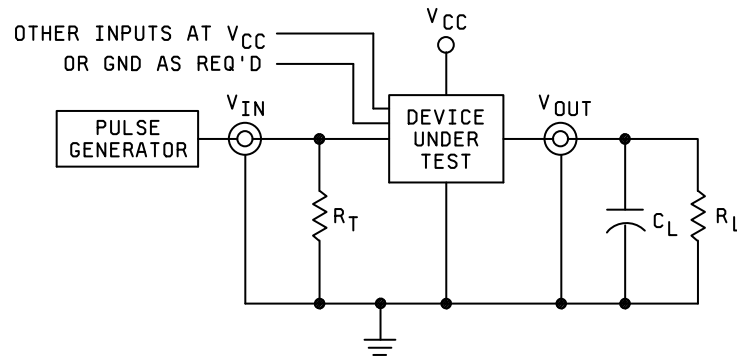$\dfrac{1}{f_{MAX}}$

CLOCK INPUT
FREQUENCY
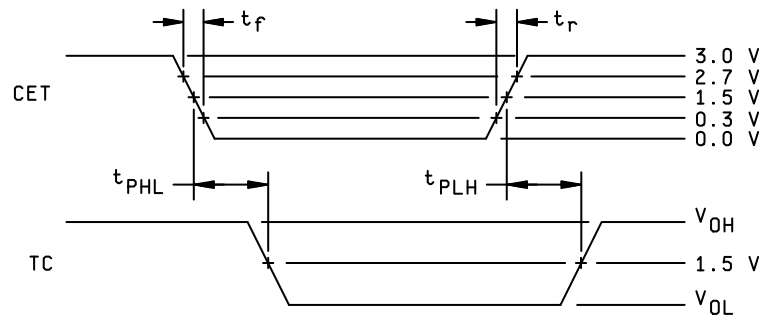
3.0 V
1.5 V
0.0 V

FIGURE 5.  Switching waveforms and test circuit.

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NOTES:

1. $C_L$ = 50 pF (includes test jig and probe capacitance).
2. RL = 500$\Omega$ or equivalent, $R_T$ = 50$\Omega$ or equivalent
3. Input signal from pulse generator: $V_{IN}$ = 0.0 V to 3.0 V; PRR $\leq$ 10 MHz; duty cycle = 50 percent; $t_r \leq$ 2.5 ns; $t_f \leq$ 2.5 ns; $t_r$ and $t_f$ shall be measured from 0.3 V to 2.7V and from 2.7 V to 0.3 V, respectively;.
4. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 5.  Switching waveforms and test circuit – Continued.

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4. VERIFICATION

4.1 <u>Sampling and inspection</u>. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 <u>Screening</u>. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 <u>Additional criteria for device class M</u>.

    a.  Burn-in test, method 1015 of MIL-STD-883.

        (1)  Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

        (2)  $T_A$ = +125°C, minimum.

    b.  Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 <u>Additional criteria for device classes Q and V</u>.

    a.  The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

    b.  Interim and final electrical test parameters shall be as specified in table II herein.

    c.  Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 <u>Qualification inspection for device classes Q and V</u>. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 <u>Conformance inspection</u>. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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TABLE II.  Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | - - - | - - - | 1 |
| Final electrical parameters (see 4.2) | 1/  1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 | 1/  1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 | 2/  1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 |
| Group A test requirements (see 4.4) | 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 3, 4, 5, 6 | 1, 2, 3, 4, 5, 6 | 1, 2, 3, 4, 7,8, 9, 10, 11 |
| Group D end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 | 1, 2, 3 |
| Group E end-point electrical parameters (see 4.4) | 1, 4, 7, 9 | 1, 4, 7, 9 | 1, 4, 7, 9 |

1/  PDA applies to subgroup 1.
2/  PDA applies to subgroups 1 and 7.

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4.4.1 <u>Group A inspection</u>.

   a.  Tests shall be as specified in table II herein.

   b.  Ground and $V_{CC}$ bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. $V_{OLP}$, $V_{OLV}$, $V_{OHP}$, and $V_{OHV}$ shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The 5 devices to be tested shall be the worst case device type supplied to this drawing. All other device types shall be guaranteed, if not tested, to the limits established for the worst case device type. The package type and device type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DSCC-VA data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each $V_{OLP}$, $V_{OLV}$, $V_{OHP}$, and $V_{OHV}$ from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

       Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DSCC-VA of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DSCC-VA data from testing on both fixtures, that shall include all measured peak values for each device tested and detailed oscilloscope plots for each $V_{OLP}$, $V_{OLV}$, $V_{OHP}$, and $V_{OHV}$ from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

       For $V_{OHP}$, $V_{OHV}$, $V_{OLP}$, and $V_{OLV}$, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types that by design will yield the same test values when tested in accordance with table I, herein. The device manufacturer shall set a functional group limit for the $V_{OHP}$, $V_{OHV}$, $V_{OLP}$, and $V_{OLV}$ tests. The device manufacturer may then test one device function from a functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I, herein. The device manufacturers shall submit to DSCC-VA the device functions listed in each functional group and test results, along with the oscilloscope plots, for each device tested.

   c.  $C_{IN}$, and $C_{OUT}$ shall be measured only for initial qualification and after process or design changes which may affect capacitance. $C_{IN}$ and shall be measured between the designated terminal and GND at a frequency of 1 MHz. For $C_{IN}$, and $C_{OUT}$, test all applicable pins on five devices with zero failures.

   d.  For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 <u>Group C inspection</u>. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 <u>Additional criteria for device class M</u>. Steady-state life test conditions, method 1005 of MIL-STD-883:

   a.  Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

   b.  $T_A$ = +125°C, minimum.

   c.  Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 <u>Additional criteria for device classes Q and V</u>. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

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4.4.3 <u>Group D inspection</u>. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

    a.    End-point electrical parameters shall be as specified in table II herein.

    b.    For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.5 <u>Methods of inspection</u>. Methods of inspection shall be specified as follows:

4.5.1 <u>Voltage and current</u>. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Current given are conventional current and positive when flowing into the referenced terminal.

5.  PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6.  NOTES

6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 <u>Substitutability</u>. Device class Q devices will replace device class M devices.

6.2 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 <u>Record of users</u>. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 <u>Abbreviations, symbols, and definitions</u>. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 <u>Sources of supply</u>.

6.6.1 <u>Sources of supply for device classes Q and V</u>. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 <u>Approved sources of supply for device class M</u>. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 10-03-22

Approved sources of supply for SMD 5962-92210 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-9221001M2A | 3/ | 54FCT163T |
| 5962-9221001MEA | 3/ | 54FCT163TDB |
| 5962-9221001MFA | 3/ | 54FCT163TEB |
| 5962-9221002M2A | OC7V7 | IDT54FCT163TLB |
| 5962-9221002MEA | OC7V7 | IDT54FCT163TDB |
| 5962-9221002MFA | OC7V7 | IDT54FCT163TEB |
| 5962-9221003M2A | 3/ | 54FCT163AT |
| 5962-9221003MEA | 3/ | 54FCT163AT |
| 5962-9221003MFA | 3/ | 54FCT163AT |
| 5962-9221004M2A | OC7V7 | IDT54FCT163ATLB |
| 5962-9221004MEA | OC7V7 | IDT54FCT163ATDB |
| 5962-9221004MFA | OC7V7 | IDT54FCT163ATEB |
| 5962-9221005M2A | 3/ | 54FCT163CT |
| 5962-9221005MEA | 3/ | 54FCT163CT |
| 5962-9221005MFA | 3/ | 54FCT163CT |
| 5962-9221006M2A | OC7V7 | IDT54FCT163CTLB |
| 5962-9221006MEA | OC7V7 | IDT54FCT163CTDB |
| 5962-9221006MFA | OC7V7 | IDT54FCT163CTEB |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 0C7V7 | QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051 |

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5962-8956101EA  MC10E446FNG  74HC195N  74HC4516N  74HCT182N  HEF4021BD  HEF4534BP  MC144111P  NLV74HC165ADTR2G  5962-9172201M2A  MC74HC597ADG  MC100EP142MNG  MC100EP016AMNG  5962-9172201MFA  MC74HC164BDR2G  TC74HC165AP(F)  74AHC164T14-13  MC74LV594ADR2G  NLV14094BDTR2G  NLV74HC595ADTG  MC74HC165AMNTWG  TPIC6C595PWG4  74VHC164MTCX  CD74HC195M96  CD4073BM96  CD4053BM96  MM74HC595MTCX  74HCT164T14-13  74HCT164S14-13  74HC4094D-Q100J  NLV14014BFELG  NLV74HC165ADR2G  NLV74HC589ADTR2G  NPIC6C595D-Q100,11  NPIC6C595PW,118  NPIC6C596ADJ  NPIC6C596APW-Q100J  NPIC6C596D-Q100,11  BU4094BCF-E2  BU4094BCFV-E2  74HC164D14  74HC164T14-13  TPIC6C596PWRG4  STPIC6D595MTR  STP08CP05MTR  CD74HC123E  74HC164D.653  74HC165D.653  74HCT165D.652  74HCT164D.652