REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes are in accordance with the notice of revision 5962-R138-93. - jak	93-04-14	Monica L. Poelking
B	Changes are in accordance with the notice of revision 5962-R105-94. - tvn	94-08-02	Monica L. Poelking
C	Changes are in accordance with the notice of revision 5962-R165-96. - jak	96-06-28	Monica L. Poelking
D	Incorporate previous notice of revisions. Update the boilerplate to the current requirements of MIL-PRF-38535. - jak	08-04-09	Thomas M. Hess

REV																				
SHEET																				
REV	D	D	D	D	D															
SHEET	15	16	17	18	19															

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Joseph A. Kerby

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Thomas J. Ricciuti

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
93-03-30

REVISION LEVEL
D

MICROCIRCUIT, DIGITAL, FAST CMOS, OCTAL TRANSCEIVER/REGISTER WITH THREE-STATE OUTPUTS, TTL COMPATIBLE INPUTS AND LIMITED OUTPUT VOLTAGE SWING, MONOLITHIC SILICON

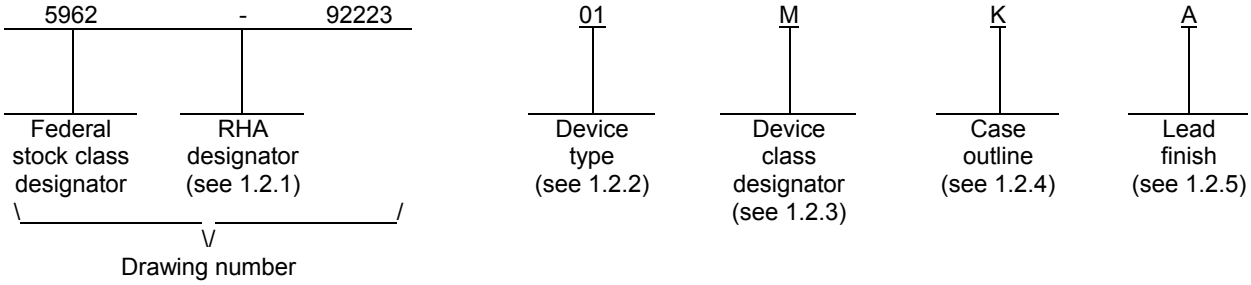
SIZE	CAGE CODE	
A	**67268**	**5962-92223**

SHEET 1 OF 19

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01, 02	54FCT646T	Octal transceiver/register with three-state outputs, TTL compatible inputs and limited output voltage swing
03, 04	54FCT646AT	Octal transceiver/register with three-state outputs, TTL compatible inputs and limited output voltage swing
05, 06	54FCT646CT	Octal transceiver/register with three-state outputs, TTL compatible inputs and limited output voltage swing

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP3-F24 or CDFP4-T24	24	Flat pack
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Leadless-chip-carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

..... Supply voltage range (V_{CC}) ..... -0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc 4/
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc 4/
DC input clamp current (I_{IK}) (V_{IN} = -0.5 V) ..... -20 mA
DC output clamp current (I_{OK}) (V_{OUT} -0.5 V and +7.0 V) ..... ±20 mA
DC output source current (I_{OH}) (per output) ..... -30 mA
DC output sink current (I_{OL}) (per output) ..... +70 mA
DC V_{CC} current (I_{CC}) ..... ±260 mA
Ground current (I_{GND}) ..... +550 mA
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Case temperature under bias (T_{BIAS}) ..... -65°C to +135°C
Maximum power dissipation (P_D) ..... 500 mW
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (Θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC}) ..... +4.5 V dc to +5.5 V dc
Input voltage range (V_{IN}) ..... +0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) ..... +0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL}) ..... 0.8 V
Minimum high level input voltage (V_{IH}) ..... 2.0 V
Case operating temperature range (T_C) ..... -55°C to +125°C
Maximum input rise or fall rate ($\Delta t/\Delta V$):
(from V_{IN} = 0.3 V to 2.7 V, 2.7 V to 0.3 V) ..... 5 ns/V
Maximum high level output current (I_{OH}) ..... -12 mA
Maximum low level output current (I_{OL}) ..... 48 mA

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ For $V_{CC} \geq 6.5$ V, the upper limit on the range is limited to 7.0 V.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Ground bounce load circuit and waveforms. The ground bounce load circuit and waveforms shall be as specified on figure 4.

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 37 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
High level output voltage 3006	V_{OH1} 4/	For all inputs affecting output under test V_{IN} = 2.0 V or 0.8 V For all other inputs $V_{IN} = V_{CC}$ or GND I_{OH} = -300 µA	All	4.5 V	1, 2, 3	3.0	V_{CC}-0.5	V
	V_{OH2}	For all inputs affecting output under test V_{IN} = 2.0 V or 0.8 V For all other inputs $V_{IN} = V_{CC}$ or GND I_{OH} = -12 mA	All	4.5 V	1, 2, 3	2.4	V_{CC}-0.5	V
Low level output voltage 3007	V_{OL1} 4/	For all inputs affecting output under test V_{IN} = 2.0 V or 0.8 V For all other inputs $V_{IN} = V_{CC}$ or GND I_{OL} = 300 µA	All	4.5 V	1, 2, 3		0.20	V
	V_{OL2}	For all inputs affecting output under test V_{IN} = 2.0 V or 0.8 V For all other inputs $V_{IN} = V_{CC}$ or GND I_{OL} = 48 mA	All	4.5 V	1, 2, 3		0.55	V
Three-state output leakage current high 3021	I_{OZH} 5/ 6/	$\overline{G} = V_{IH}$ or V_{IL} V_{IH} = 2.0 V, V_{IL} = 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND $V_{OUT} = V_{CC}$	01, 03, 05	5.5 V	1, 2		0.1	µA
					3		10.0	
			02, 04, 06		1, 2		0.1	
					3		2.0	
Three-state output leakage current low 3020	I_{OZL} 5/ 6/	$\overline{G} = V_{IH}$ or V_{IL} V_{IH} = 2.0 V, V_{IL} = 0.8 V For all other inputs, $V_{IN} = V_{CC}$ or GND V_{OUT} = GND	01, 03, 05	5.5 V	1, 2		-1.0	µA
					3		-10.0	
			02, 04, 06		1, 2		-0.1	
					3		-2.0	
Negative input clamp voltage 3022	V_{IC-}	For input under test, I_{IN} = -18 mA	01, 03, 05	4.5 V	1, 2, 3		-1.2	V
		For input under test, I_{IN} = -15 mA	02, 04, 06				-1.3	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
							Min	Max	
Input current high 3010	I_{IH}	For input under test, $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND	control inputs	01, 03, 05	5.5 V	1, 2		1.0	µA
						3		5.0	
			I/O pins			1, 2		1.0	µA
						3		15.0	
			control inputs	02, 04, 06	5.5 V	1, 2		0.1	µA
						3		1.0	
			I/O pins			1, 2		0.2	µA
						3		3.0	
Input current low 3009	I_{IL}	For input under test, $V_{IN} = GND$ For all other inputs, $V_{IN} = V_{CC}$ or GND	control inputs	01, 03, 05	5.5 V	1, 2		-1.0	µA
						3		-5.0	
			I/O pins			1, 2		-1.0	µA
						3		-15.0	
			control inputs	02, 04, 06	5.5 V	1, 2		-0.1	µA
						3		-1.0	
			I/O pins			1, 2		-0.2	µA
						3		-3.0	
Input capacitance 3012	C_{IN} 7/	See 4.4.1c $T_C = +25°C$		All	GND	4		10	pF
Input/output capacitance 3012	$C_{I/O}$ 7/	See 4.4.1c $T_C = +25°C$		All	GND	4		12	pF
Short circuit output current 3005	I_{OS} 8/	For all inputs, $V_{IN} = V_{CC}$ or GND $V_{OUT} = GND$		All	5.5 V	1, 2, 3	-60	-225	mA
Dynamic power supply current	I_{CCD} 4/ 9/	Outputs open		All	5.5 V	4, 5, 6		0.25	mA/ MHz•Bit
Quiescent supply current delta, TTL input level 3005	ΔI_{CC} 10/	For input under test $V_{IN} = V_{CC} - 2.1\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND		All	5.5 V	1, 2, 3		2.0	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
							Min	Max	
Quiescent supply current, output high 3005	I_{CCH}	$\overline{G}$ = GND For all other inputs, $V_{IN} = V_{CC}$ or GND		All	5.5 V	1, 2, 3		1.5	mA
Quiescent supply current, output low 3005	I_{CCL}	$\overline{G}$ = GND For all other inputs, $V_{IN} = V_{CC}$ or GND		All	5.5 V	1, 2, 3		1.5	mA
Quiescent supply current, output three-state 3005	I_{CCZ} 5/	$\overline{G} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND		All	5.5 V	1, 2, 3		1.5	mA
Total supply current	I_{CCT1} 11/	Outputs open $\overline{G}$ = DIR = GND f_{CP} = 10 MHz 50% duty cycle One bit toggling f_i = 5 MHz 50% duty cycle For nonswitching inputs, $V_{IN} = V_{CC}$ or GND	For switching inputs, $V_{IN} = V_{CC}$ or GND	All	5.5 V	4, 5, 6		4.0	mA
			For switching inputs, V_{IN} = 3.4 V or GND		5.5 V	4, 5, 6		6.0	
		Outputs open $\overline{G}$ = DIR = GND f_{CP} = 10 MHz 50% duty cycle Eight bits toggling f_i = 5 MHz 50% duty cycle For nonswitching input, $V_{IN} = V_{CC}$ or GND	For switching inputs, $V_{IN} = V_{CC}$ or GND		5.5 V	4, 5, 6		12.8	
			For switching inputs, V_{IN} = 3.4 V or GND		5.5 V	4, 5, 6		21.8	
Low level ground bounce noise	V_{OLP} 7/ 12/	V_{IH} = 3.0 V V_{IL} = 0.0 V T_A = +25°C See figure 4 See 4.4.1b		01, 03, 05	5.0 V	4		1900	mV
				02, 04, 06				620	
	V_{OLV} 7/ 12/			01, 03, 05	5.0 V	4		-1500	
				02, 04, 06				-740	
High level V_{CC} bounce noise	V_{OHP} 7/ 12/			01, 03, 05	5.0 V	4		1300	mV
				02, 04, 06				380	
	V_{OHV} 7/ 12/			01, 03, 05	5.0 V	4		-700	
				02, 04, 06				-240	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Functional test 3014	13/	V_{IH} = 2.0 V, V_{IL} = 0.8 V Verify output V_O See 4.4.1d	All	4.5 V	7, 8	L	H	
				5.5 V	7, 8	L	H	
Propagation delay time, data to output, An to Bn, Bn to An 3003	t_{PLH}, t_{PHL} 14/	C_L = 50 pF minimum R_L = 500Ω See figure 5	01, 02	4.5 V	9, 10, 11	2.0	11.0	ns
			03, 04		9, 10, 11	2.0	7.7	
			05, 06		9, 10, 11	1.5	6.0	
Propagation delay time, SBA to An, SAB to Bn 3003	t_{PLH}, t_{PHL} 14/		01, 02	4.5 V	9, 10, 11	2.0	12.0	ns
			03, 04		9, 10, 11	2.0	8.4	
			05, 06		9, 10, 11	1.5	7.0	
Propagation delay time, CPBA to An, CPAB to Bn 3003	t_{PLH}, t_{PHL} 14/		01, 02	4.5 V	9, 10, 11	2.0	10.0	ns
			03, 04		9, 10, 11	2.0	7.0	
			05, 06		9, 10, 11	1.5	6.3	
Propagation delay time, output enable, G to An or G to Bn 3003	t_{PZH}, t_{PZL} 14/		01, 02	4.5 V	9, 10, 11	2.0	15.0	ns
			03, 04		9, 10, 11	1.5	10.5	
			05, 06		9, 10, 11	1.5	8.9	
Propagation delay time, output disable, G to An or G to Bn 3003	t_{PHZ}, t_{PLZ} 14/		01, 02	4.5 V	9, 10, 11	2.0	11.0	ns
			03, 04		9, 10, 11	2.0	7.7	
			05, 06		9, 10, 11	1.5	7.7	
Propagation delay time, output enable, DIR to An, DIR to Bn 3003	t_{PZH}, t_{PZL} 4/		01, 02	4.5 V	9, 10, 11	2.0	15.0	ns
			03, 04		9, 10, 11	2.0	10.5	
			05, 06		9, 10, 11	1.5	8.9	
Propagation delay time, output disable, DIR to An, DIR to Bn 3003	t_{PHZ}, t_{PLZ} 4/		01, 02	4.5 V	9, 10, 11	2.0	11.0	ns
			03, 04		9, 10, 11	2.0	7.7	
			05, 06		9, 10, 11	1.5	7.7	
Set-up time, data high or low, An to CPAB, Bn to CPBA	t_s 4/		01, 02	4.5 V	9, 10, 11	4.5		ns
			03, 04		9, 10, 11	2.0		
			05, 06		9, 10, 11	2.0		
Hold time, data high or low, An from CPAB, Bn from CPBA	t_h 4/		01, 02	4.5 V	9, 10, 11	2.0		ns
			03, 04		9, 10, 11	1.5		
			05, 06		9, 10, 11	1.5		
Clock pulse width CPAB, CPBA	t_s 4/		01, 02	4.5 V	9, 10, 11	6.0		ns
			03, 04		9, 10, 11	5.0		
			05, 06		9, 10, 11	5.0		

See footnotes on next sheet.

TABLE I. Electrical performance characteristics - Continued.

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure of 883 under the conditions listed herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I_{CC} and ΔI_{CC} tests, the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I at $4.5\ V \le V_{CC} \le 5.5\ V$.

4/ This parameter is guaranteed, if not tested, to the limits specified in table I.

5/ Three-state output conditions are required.

6/ This test may be performed using $V_{IH} = 3.0$ V. When $V_{IH} = 3.0$ V is used, the test is guaranteed for $V_{IH} = 2.0$ V. This test is guaranteed by the I_{IL} and I_{IH} test.

7/ This test is required only for group A testing, see 4.4.1 herein.

8/ Not more than one output should be shorted at a time. The duration of the short circuit test should not exceed one second.

9/ I_{CCD} may be verified by the following equation:

$$I_{CCD} = \frac{I_{CCT} - I_{CC} - D_H N_T \Delta I_{CC}}{f_{CP}/2 + f_i N_i}$$

where I_{CCT}, I_{CC} (I_{CCL} or I_{CCH} in table I), and ΔI_{CC} shall be the measured values of these parameters, for the device under test, when tested as described in table I, herein. The values for D_H, N_T, f_{CP}, f_i, and N_i shall be as listed in the test conditions column for I_{CCT} in table I, herein.

10/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC} - 2.1$ V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 2.0 mA; and the preferred method and limits are guaranteed.

11/ I_{CCT} is calculated as follows:

$$I_{CCT} = I_{CC} + D_H N_T \Delta I_{CC} + I_{CCD}(f_{CP}/2 + f_i N_i)$$

where:
I_{CC} = Quiescent supply current (any I_{CCL} or I_{CCH})
D_H = Duty cycle for TTL inputs at 3.4 V
N_T = Number of TTL inputs at 3.4 V
ΔI_{CC} = Quiescent supply current delta, TTL inputs at 3.4 V
I_{CCD} = Dynamic power supply current caused by an input transition pair (HLH or LHL)
f_{CP} = Clock frequency for registered devices ($f_{CP} = 0$ for nonregistered devices)
f_i = input frequency
N_i = Number of inputs at f_i

TABLE I. Electrical performance characteristics - Continued.

12/ This test is for qualification only. Ground and V_{CC} bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with 500Ω of load resistance and a minimum of 50 pF of load capacitance (see figure 4). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from V_{CC} to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and V_{CC} bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a 50Ω input impedance.

The device inputs shall be conditioned such that all outputs are at a high nominal V_{OH} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OH} as all other outputs possible are switched from V_{OH} to V_{OL}. V_{OHV} and V_{OHP} are then measured from the nominal V_{OH} level to the largest negative and positive peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from V_{OL} to V_{OH}.

The device inputs shall be conditioned such that all outputs are at a low nominal V_{OL} level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at V_{OL} as all other outputs possible are switched from V_{OL} to V_{OH}. V_{OLP} and V_{OLV} are then measured from the nominal V_{OL} level to the largest positive and negative peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from V_{OH} to V_{OL}.

13/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. For outputs, L < 1.5 V, H ≥ 1.5 V.

14/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum propagation delay time limits for V_{CC} = 4.5 V and 5.5 V are guaranteed, if not tested, to the limits specified in table I, herein. For propagation delay tests, all paths must be tested.

Device types	All	
Case outlines	L and K	3
Terminal number	Terminal symbol	
1	CPAB	NC
2	SAB	CPAB
3	DIR	SAB
4	A1	DIR
5	A2	A1
6	A3	A2
7	A4	A3
8	A5	NC
9	A6	A4
10	A7	A5
11	A8	A6
12	GND	A7
13	B8	A8
14	B7	GND
15	B6	NC
16	B5	B8
17	B4	B7
18	B3	B6
19	B2	B5
20	B1	B4
21	$\overline{G}$	B3
22	SBA	NC
23	CPBA	B2
24	V_{CC}	B1
25	- - -	$\overline{G}$
26	- - -	SBA
27	- - -	CPBA
28	- - -	V_{CC}

Terminal descriptions	
Terminal symbol	Description
DIR, $\overline{G}$	Output enable control inputs
SAB, SBA	Output data source select inputs
CPAB, CPBA	Clock pulse timing inputs
An (n = 1 to 8)	Data register A inputs Data register B outputs
Bn (n = 1 to 8)	Data register B inputs Data register A outputs

FIGURE 1. Terminal connections.

Inputs						Data I/O 1/		Function
G	DIR	CPAB	CPBA	SAB	SBA	A1 - A8	B1 - B8	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X	Input	Input	Store A and B data
L	L	X	X	X	L	Output	Input	Real time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

1/ The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every low-to-high transition of the clock inputs.

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance

FIGURE 2. Truth table.

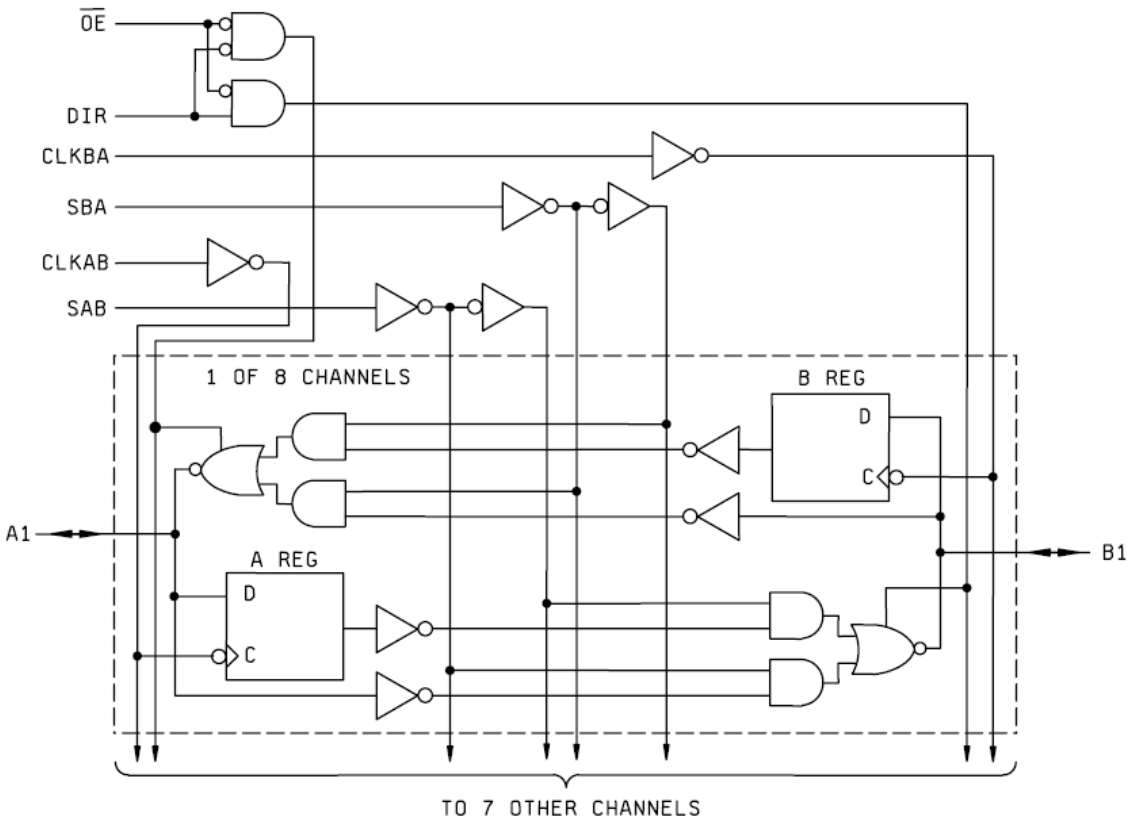
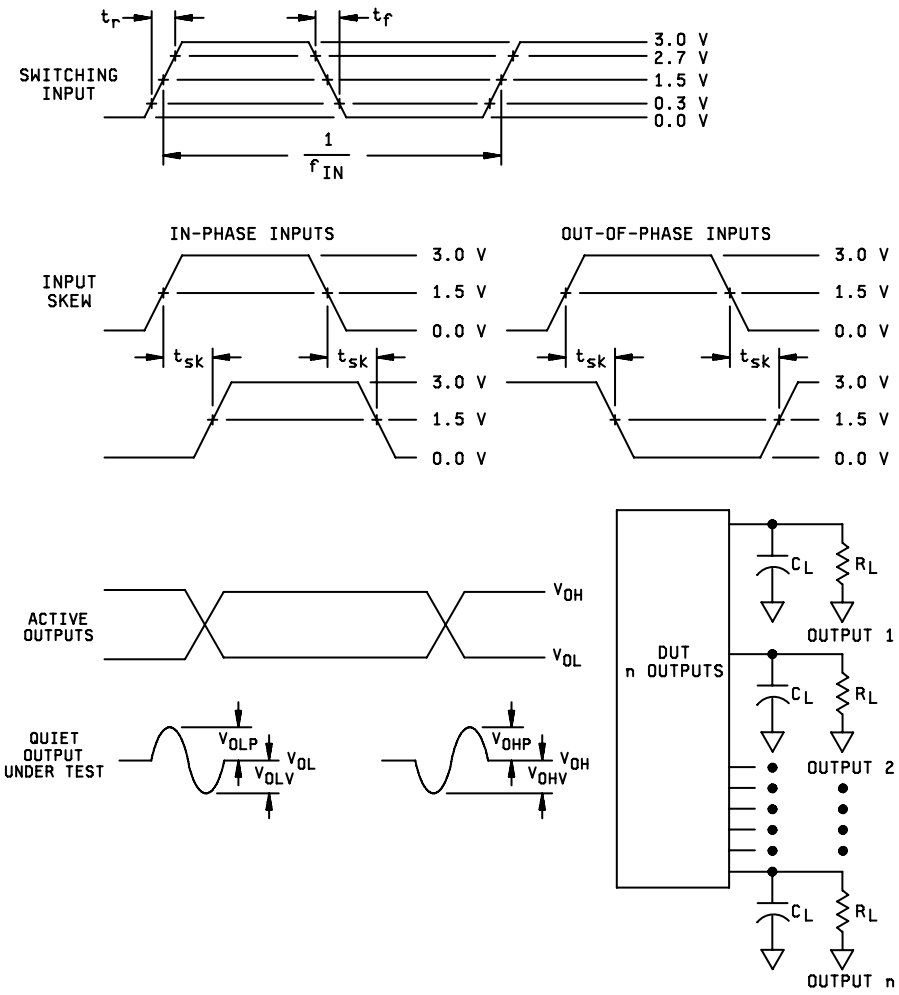


FIGURE 3. Logic diagram.



NOTES:

1. C_L includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2. R_L = 450Ω ±1 percent, chip resistor in series with a 50Ω termination. For monitored outputs, the 50Ω termination shall be the 50Ω characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
   a. V_{IN} = 0.0 V to 3.0 V; duty cycle = 50 percent; $f_{IN} \geq 1$ MHz.
   b. t_r, t_f = 3.0 ns ±1.0 ns. For input signal generators incapable of maintaining these values of t_r and t_f, the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the ±1.0 ns tolerance and guaranteeing the results at 3.0 ns ±1.0 ns; skew between any two switching inputs signals (t_{sk}): ≤ 250 ps.

FIGURE 4. Ground bounce waveforms and test circuit.

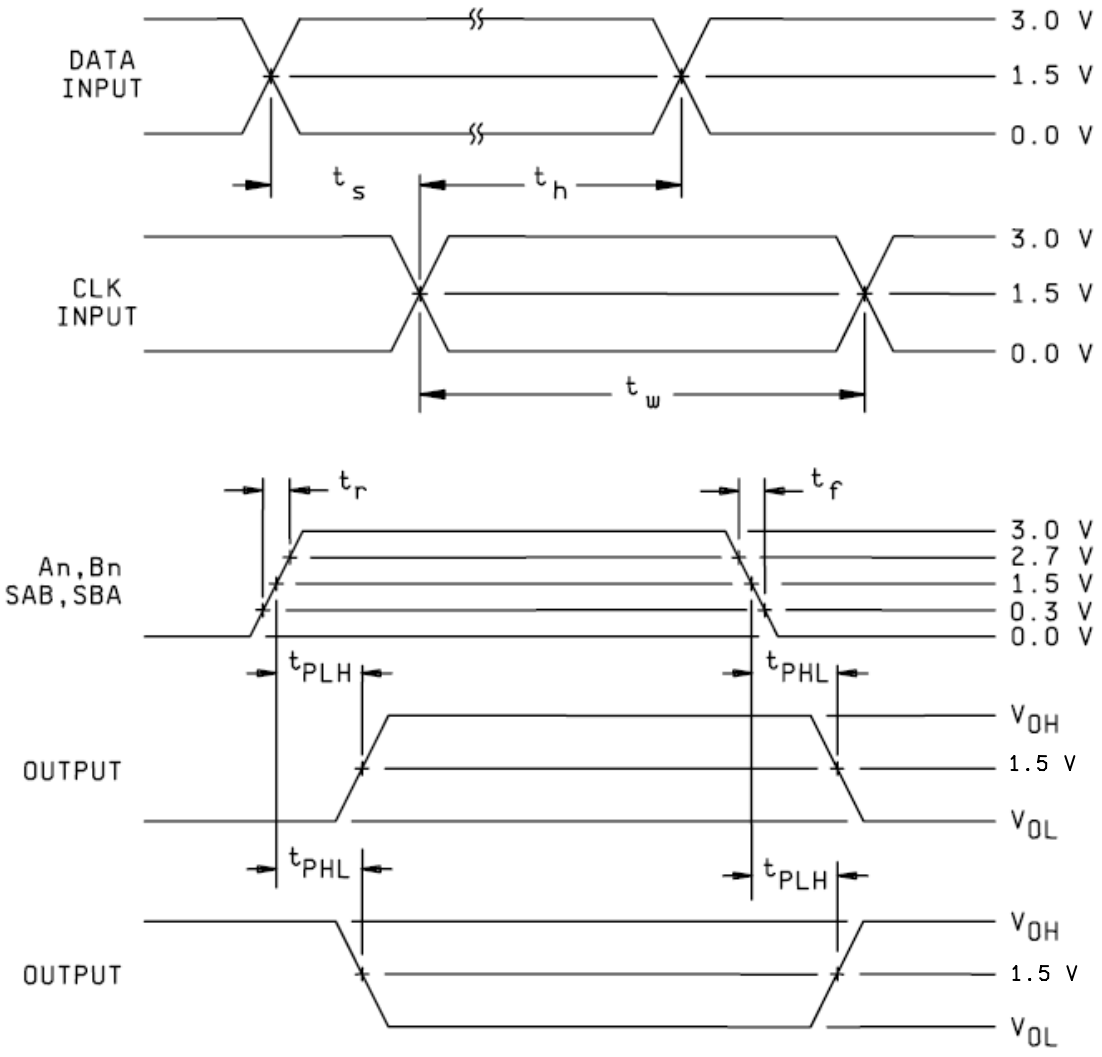
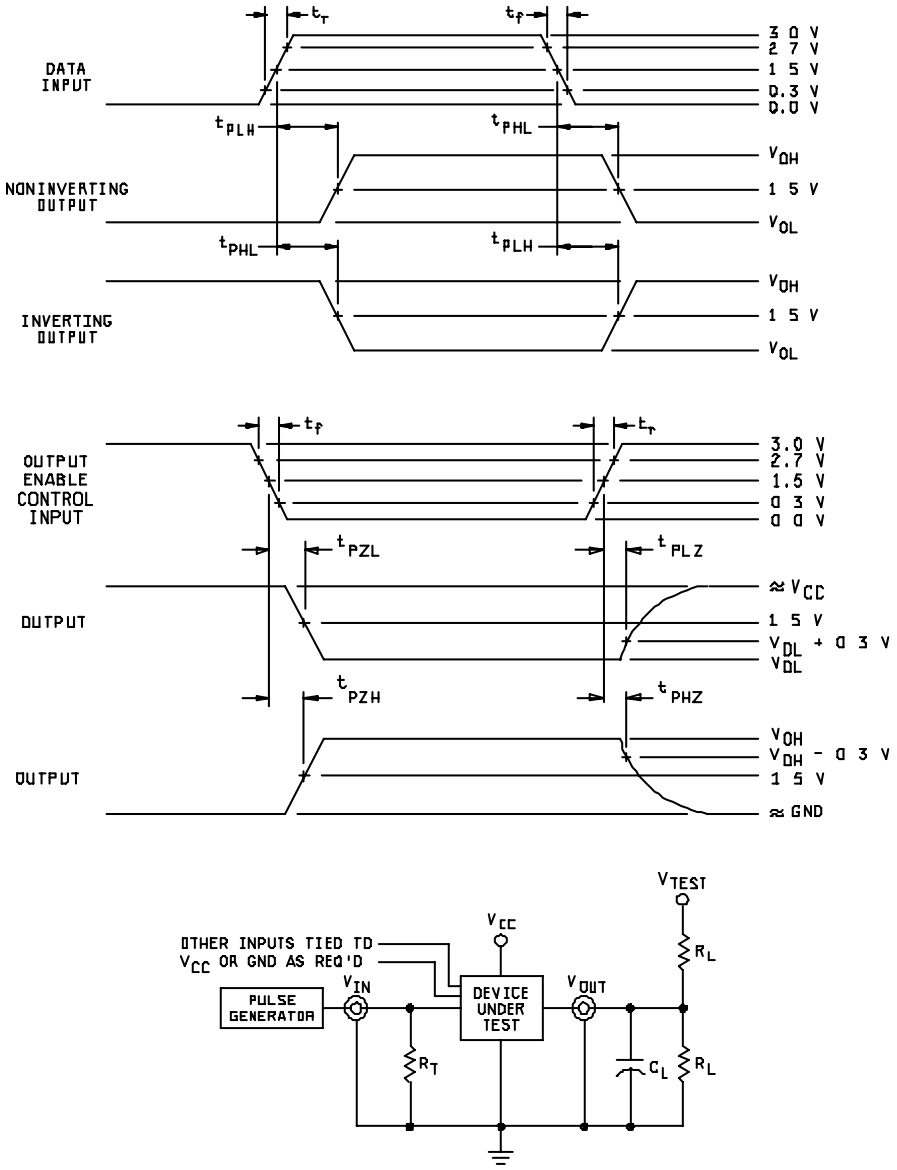


FIGURE 5. Switching waveforms and test circuit.



NOTES:

1. When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 7.0 V.
2. When measuring t_{PHZ}, t_{PZH}, t_{PLH}, and t_{PHL}: V_{TEST} = Open.
3. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
4. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. R_T = 50Ω or equivalent.
6. R_L = 500Ω or equivalent.
7. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; $t_r \leq 2.5$ ns; $t_f \leq 2.5$ ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V respectively; duty cycle = 50 percent.
8. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
9. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit -Continued

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

b. Ground and V_{CC} bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture. V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The package type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DSCC-VA data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DSCC-VA of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DSCC-VA data from testing on both fixtures that shall include all measured peak values for each device tested and detailed oscilloscope plots for each V_{OLP}, V_{OLV}, V_{OHP}, and V_{OHV} from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

c. C_{IN} and $C_{I/O}$ shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and $C_{I/O}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. For C_{IN} and $C_{I/O}$, test all applicable pins on five devices with zero failures.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	1	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1/ 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	2/ 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 5, 6	1, 2, 3, 4, 5, 6	1, 2, 3, 4, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 4, 7, 9	1, 4, 7, 9	1, 4, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-04-09

Approved sources of supply for SMD 5962-92223 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9222301M3A	01295	CY54FCT646TLMB
	0C7V7	IDT54FCT646TLB
5962-9222301MKA	0C7V7	IDT54FCT646TEB
5962-9222301MLA	0C7V7	IDT54FCT646TDB
5962-9222302M3A	3/	54FCT646AT
5962-9222302MLA	3/	54FCT646AT
5962-9222303M3A	01295	CY54FCT646ATLMB
	0C7V7	IDT54FCT646ATLB
5962-9222303MKA	0C7V7	IDT54FCT646ATEB
5962-9222303MLA	01295	CY54FCT646ATDMB
	0C7V7	IDT54FCT646ATDB
5962-9222304M2A	3/	54FCT646AT
5962-9222304MRA	3/	54FCT646AT
5962-9222305M3A	01295	CY54FCT646CTLMB
	0C7V7	IDT54FCT646CTLB
5962-9222305MKA	0C7V7	IDT54FCT646CTEB
5962-9222305MLA	0C7V7	IDT54FCT646CTDB
5962-9222306M2A	3/	54FCT646CT
5962-9222306MRA	3/	54FCT646CT

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Bus Transceivers ***category:***

Click to view products by E2v ***manufacturer:***

Other Similar products are found below :

74LS645N DS8838 FXL4TD245UMX IDT74CBTLV3257PGG 74LVT245BBT20-13 5962-8683401DA PCA9617ADMR2G 5962-8953501KA 5962-86834012A 5962-7802301Q2A 5962-7802002MFA 5962-7802001MFA 74VHCV245FT(BJ) NCV7349D13R2G TC74VCX164245(EL,F MC74LCX245MNTWG TC7WPB8306L8X,LF(S TC7WPB9307FC(TE85L 74FCT16245CTPVG8 74FCT16543CTPVG 74FCT245CTPYG8 MM74HC245AMTCX 74LVCH16245APVG 74LVX245MTC 5962-9221405M2A NTS0102DP-Q100H 74ALVC16245MTDX 74ALVCH32245BF 74FCT163245APVG 74FCT245ATPYG8 74FCT245CTQG 74FCT3245AQG 74LCXR162245MTX 74VHC245M 74VHC245MX TC7WPB9306FC(TE85L TC7WPB9306FK(T5L,F JM38510/65553BRA ST3384EBDR 74LVC1T45GF,132 74AVC4TD245BQ,115 PQJ7980AHN/C0JL,51 MC100EP16VBDG FXL2TD245L10X 74LVC1T45GM,115 TC74AC245P(F) PSB21150F S LLHR SNJ54LS245FK SNJ54AHC245J SNJ54ABT245AFK