REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update drawing to reflect current requirements. Editorial changes throughout. - gap	01-05-04	Raymond Monnin
B	Added case outline Z. Updated boiler plate paragraphs. ksr	05-05-02	Raymond Monnin
C	Boilerplate update, part of 5 year review. ksr	11-01-20	Charles F. Saffle

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C					
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29					

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
93-10-29

REVISION LEVEL
C

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 2K X 9 PARALLEL FIFO, MONOLITHIC SILICON

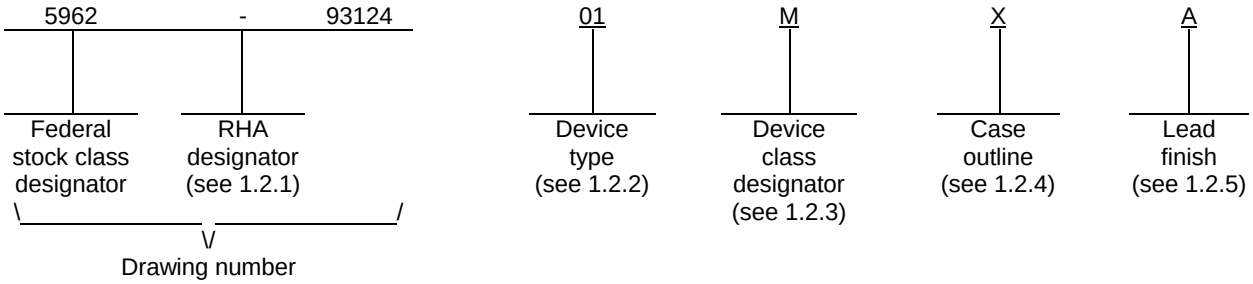
SIZE	CAGE CODE	
A	**67268**	**5962-93124**

SHEET 1 OF 29

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	7C453	2K x 9 Cascadable Clocked FIFO	30 ns
02	7C453	2K x 9 Cascadable Clocked FIFO	20 ns
03	7C453	2K x 9 Clocked FIFO	14 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	32	Dual-in-line
Y	CQCC1-N32	32	Rectangular leadless chip carrier
Z	See figure 1	32	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC voltage applied to the outputs in the high Z state	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
Maximum power dissipation	0.825 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X and Z	11°C/W
Case Y	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the JEDEC Office, 3103 North 10th Street, Arlington, VA 22201-2107; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.0 mA $V_{IN} = V_{IH}(Min), V_{IL}(Max)$	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA $V_{IN} = V_{IH}(Min), V_{IL}(Max)$	1, 2, 3	All		0.4	V
Input high voltage 1/, 2/	V_{IH}		1, 2, 3	All	2.2		V
Input low voltage 1/, 2/	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{CC}= Max	1, 2, 3	All	-10	+10	µA
Output leakage current	I_{OZ}	$OE \ge V_{IH}$ $V_{OUT} = V_{SS}$ to V_{CC}	1, 2, 3	All	-10	+10	µA
Power supply current 3/	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = 0 to 3.0 V	1, 2, 3	01		110	mA
				02		130	
				03		150	
Power supply current 4/	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = 0 to 3.0 V	1, 2, 3	All		80	mA
Standby current 5/	I_{CC3}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, All inputs = V_{CC}	1, 2, 3	All		30	mA
Input capacitance 6/	C_{IN}	V_{CC} = 5.0 V, T = 25°C, f = 1 MHz, (see 4.4.1e)	4	All		10	pF
Output capacitance 6/	C_{OUT}	V_{CC} = 5.0 V, T = 25°C, f = 1 MHz (see 4.4.1e)	4	All		12	pF
Functional testing 7/		See 4.4.1c	7, 8A, 8B	All			
Write clock cycle	t_{CKW}	See figures 4 and 5 8/	9, 10, 11	01	30		ns
				02	20		
				03	14		
Read clock cycle	t_{CKR}		9, 10, 11	01	30		ns
				02	20		
				03	14		
Clock high	t_{CKH}		9, 10, 11	01	12		ns
				02	9		
				03	6.5		

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Clock low	t_{CKL}	See figures 4 and 5 8/	9, 10, 11	01	12		ns
				02	9		
				03	6.5		
Data access time 9/	t_A		9, 10, 11	01		20	ns
				02		15	
				03		10	
Previous output data hold after read high	t_{OH}		9, 10, 11	All	0		ns
Previous flag hold after read/write high	t_{FH}		9, 10, 11	All	0		ns
Data set-up	t_{SD}		9, 10, 11	01	12		ns
				02	9		
				03	7		
Data hold	t_{HD}		9, 10, 11	All	0		ns
Enable set-up	t_{SEN}		9, 10, 11	01	12		ns
				02	9		
				03	7		
Enable hold	t_{HEN}		9, 10, 11	All	0		ns
$\overline{OE}$ low to output data valid 10/	t_{OE}		9, 10, 11	01		20	ns
				02		15	
				03		10	
$\overline{OE}$ low to output data in low Z 6/, 10/	t_{OLZ}		9, 10, 11	All	0		ns
$\overline{OE}$ high to output data in high Z 6/, 11/, 12/	t_{OHZ}		9, 10, 11	01		20	ns
				02		15	
				03		10	
Read high to parity generation	t_{PG}		9, 10, 11	01		20	ns
				02		15	
				03		10	
Read high to parity error flag	t_{PE}		9, 10, 11	01		20	ns
				02		15	
				03		10	
Flag Delay	t_{FD}		9, 10, 11	01		20	ns
				02		15	
				03		10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Opposite clock after clock 13/	t_{SKEW1}	See figures 4 and 5 8/	9,10,11	All	0		ns
Opposite clock before clock 14/	t_{SKEW2}		9,10,11	01	30		ns
				02	20		
				03	14		
Master preset pulse width ($\overline{MR}$ low)	t_{PMR}		9,10,11	01	30		ns
				02	20		
				03	14		
Last valid clock low set-up to $\overline{MR}$ low	t_{SCMR}		9,10,11	All	0		ns
Data hold from $\overline{MR}$ low	t_{OHMR}		9,10,11	All	0		ns
Master reset recovery ($\overline{MR}$ high set-up to first enabled write/read)	t_{MRR}		9,10,11	01	30		ns
				02	20		
				03	14		
$\overline{MR}$ high to flags valid	t_{MRF}		9,10,11	01		30	ns
				02		20	
				03		14	
$\overline{MR}$ high to data outputs low	t_{AMR}		9,10,11	01		30	ns
				02		20	
				03		14	
Program mode - $\overline{MR}$ low set-up	t_{SMRP}		9,10,11	01	30		ns
				02	20		
				03	14		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Program mode - $\overline{MR}$ low hold	t_{HMRP}	See figures 4 and 5 8/	9,10,11	01	25		ns
				02	15		
				03	10		
Program Mode - write high to read high	t_{FTP}		9,10,11	01	30		ns
				02	20		
				03	14		
Program mode - data access time	t_{AP}		9,10,11	01		30	ns
				02		20	
				03		14	
Program mode - data hold time from $\overline{MR}$ high	t_{OHP}		9,10,11	All	0		ns

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

2/ The V_{IH} and V_{IL} specifications apply for all inputs except $\overline{XI}$ and $\overline{FL}$. The $\overline{XI}$ pin is not a TTL input. It is connected to either $\overline{XO}$ of the previous device or V_{SS}. $\overline{FL}$ must be connected to either V_{SS} or V_{CC}.

3/ Clocks and clock enables switch at maximum frequency (f_{MAX}), while data inputs switch at $f_{MAX}/2$.

4/ Clocks and clock enables switch at 20 MHz, while the data inputs switch at 10 MHz.

5/ Read and write clocks switch at maximum frequency.

6/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

7/ The 03 device cannot be cascaded. The total propagation delay to transfer data from one FIFO to another FIFO is greater than the 14 ns access time.

8/ AC tests are performed with input rise and fall times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load in figure 4A unless otherwise noted.

9/ Access time includes all data outputs switching simultaneously.

10/ t_{OE} and t_{OLZ} are measured at ±100 mV from the steady state.

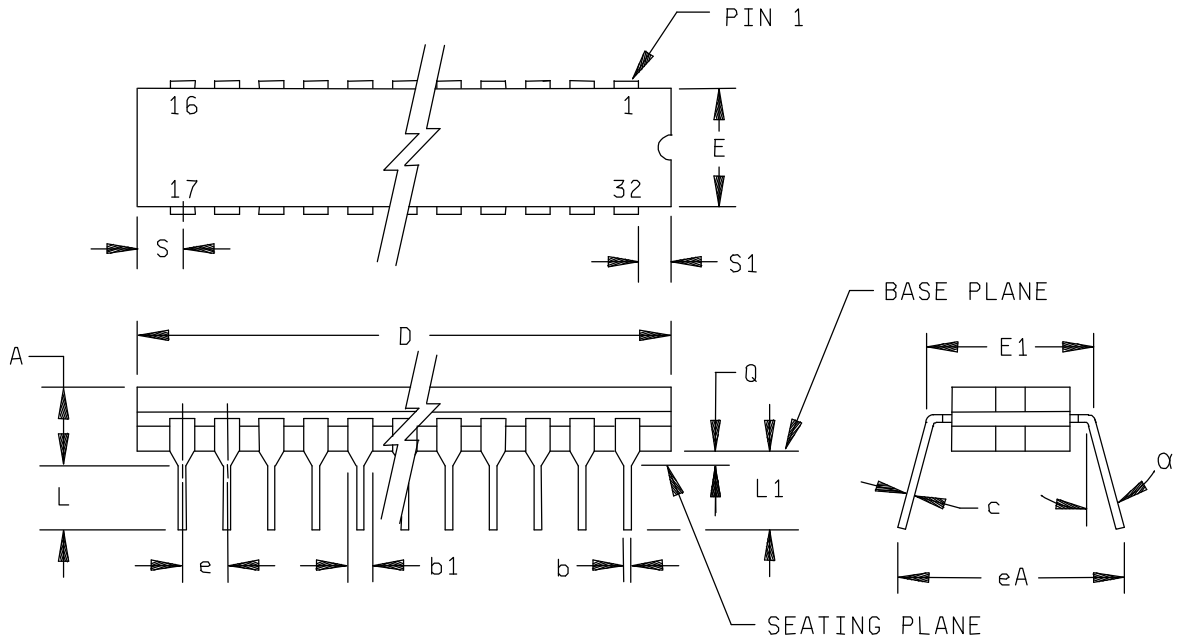
11/ C_L= 5pF for t_{OHZ}. See ouput load in figure 4B.

12/ t_{OHZ} is measured at +500 mV from V_{OL} and -500 mV from V_{OH}.

13/ t_{SKEW1} is the minimum time an opposite clock can occur after a clock and still be guaranteed not to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW1} after the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary. The opposite clock is the signal to which a flag is not synchronized; i.e., CKW is the opposite clock for Empty and Almost Empty flags, CKR is the opposite clock for the Almost Full, Half Full, and Full flags. The clock is the signal to which a flag is synchronized; i.e., CKW is the clock for the Half Full, Almost Full, and Full flags, CKR is the clock for Empty and Almost Empty flags.

14/ t_{SKEW2} is the minimum time an opposite clock can occur before a clock and still be guaranteed to be included in the current clock cycle (for purposes of flag update). If the opposite clock occurs less than t_{SKEW2} before the clock, the decision of whether or not to include the opposite clock in the current clock cycle is arbitrary.

Case X (see note)

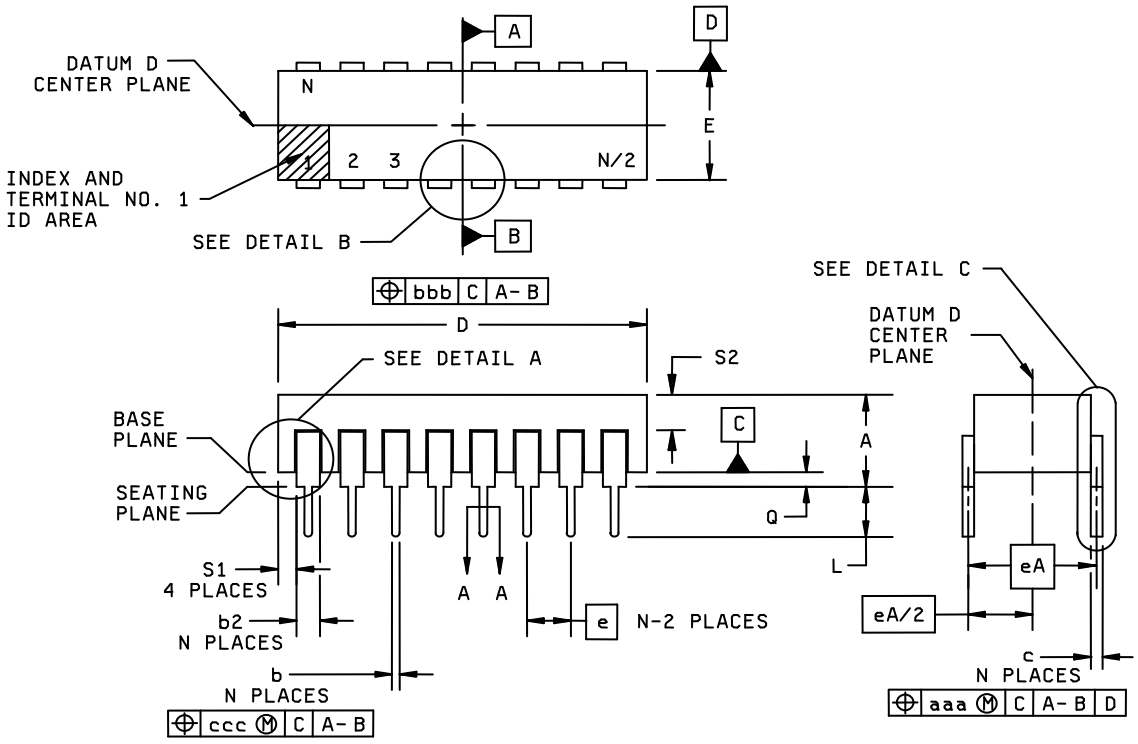


SYMBOL	DIMENSIONS			
	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.94	5.08	0.155	0.200
b	0.38	0.51	0.015	0.020
b1	1.14	1.65	0.045	0.065
c	0.23	0.30	0.009	0.012
D	41.9	42.8	1.650	1.685
E	6.22	7.87	0.245	0.310
E1	7.37	8.13	0.29	0.32
e	2.29	2.79	0.09	0.11
eA	8.38	9.91	0.33	0.39
L	3.18	5.08	0.125	0.200
L1	3.18	5.08	0.125	0.200
α	3°	15°	3°	15°
Q	0.38	1.52	0.015	0.06
S	1.65	2.41	0.065	0.095
S1	0.13		0.005	

Note:The US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.

FIGURE 1. Case Outline.

Case Z



Notes: The US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.

SYMBOL	DIMENSIONS			
	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		5.08		0.200
b 1/	0.36	0.66	0.014	0.026
b1 2/	0.36	0.58	0.014	0.023
b2	1.14	1.65	0.045	0.065
c	0.20	0.46	0.008	0.018
c1	0.20	0.38	0.008	0.015
D		42.8		1.685
E	6.22	7.87	0.245	0.310
e	2.54 BSC		.100 BSC	
eA	7.62 BSC		.300 BSC	
eA/2	3.81 BSC		.150 BSC	

SYMBOL	DIMENSIONS			
	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
L	3.18	5.08	0.125	0.200
Q 3/	0.38	1.78	0.015	0.07
S1 4/	0.13		0.005	
S2 5/	0.13		0.005	
aaa		.38		.015
bbb		.78		.030
ccc		.25		.010
M		.038		.0015
N 6/	32		32	

FIGURE 1. Case Outline - Continued.

1/ The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.

2/ Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.

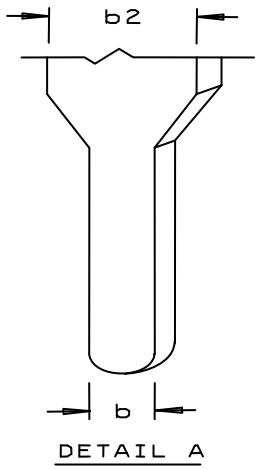
3/ Dimension Q shall be measured from the seating plane to base plane.

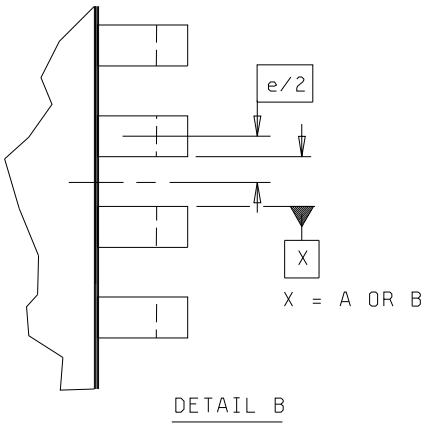
4/ Measure dimension S1 at all four corners.

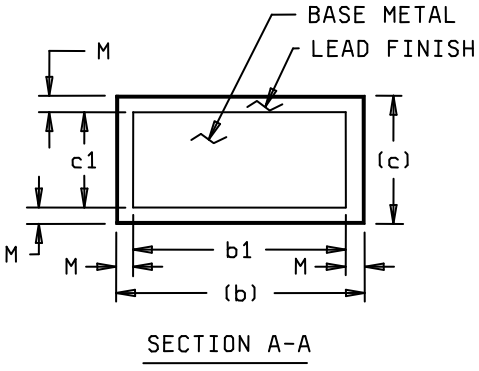
5/ Measure dimension S2 from the top of the ceramic body to the nearest metalization or lead.

6/ N is the maximum number of terminal positions.

7/ Braze fillet shall be concave. The maximum dimensions of this fillet include solder dip or tin plate lead finish, if applied.







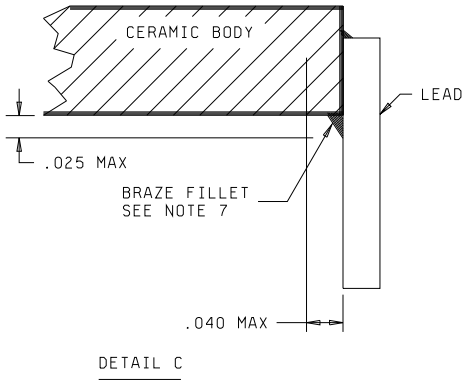


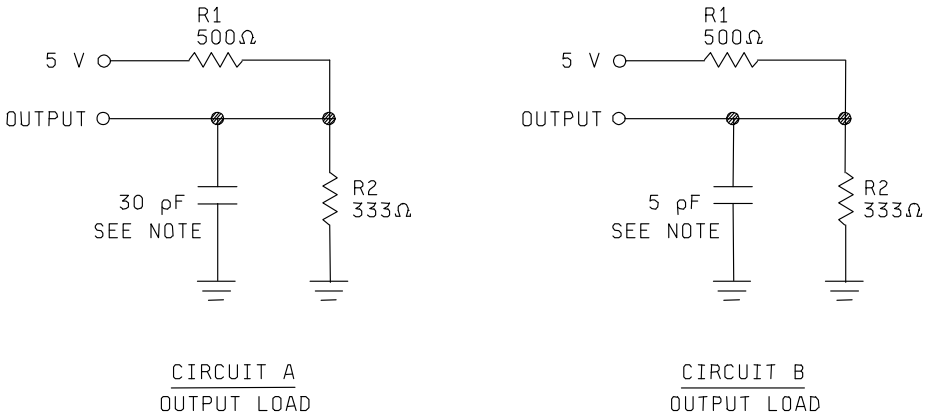
FIGURE 1. Case Outline - Continued.

Device Types	ALL
Case Outlines	X, Y, Z
Terminal Number	Terminal Symbol
1	D_3
2	D_2
3	D_1
4	D_0
5	$\overline{XI}$
6	$\overline{ENW}$
7	CKW
8	V_{CC}
9	V_{SS}
10	$\overline{HF}$
11	$\overline{E/F}$
12	$\overline{PAFE}$ / $\overline{XO}$
13	Q_0
14	Q_1
15	Q_2
16	Q_3
17	Q_4
18	Q_5
19	Q_6
20	Q_7
21	Q_8/PG/$\overline{PE}$
22	$\overline{OE}$
23	$\overline{ENR}$
24	CKR
25	V_{SS}
26	$\overline{MR}$
27	$\overline{FL}$
28	D_8
29	D_7
30	D_6
31	D_5
32	D_4

FIGURE 2. Terminal connections.

$\overline{E/F}$	$\overline{PAFE}$	$\overline{HF}$	State
0	0	1	Empty
1	0	1	Almost Empty
1	1	1	Less than or Equal to Half Full
1	1	0	Greater than Half Full
1	0	0	Almost Full
0	0	0	Full

Figure 3. Flag truth tables.



Note: Including scope and jig. (minimum values)

AC test conditions:

Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 3 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 4. Output load circuit.

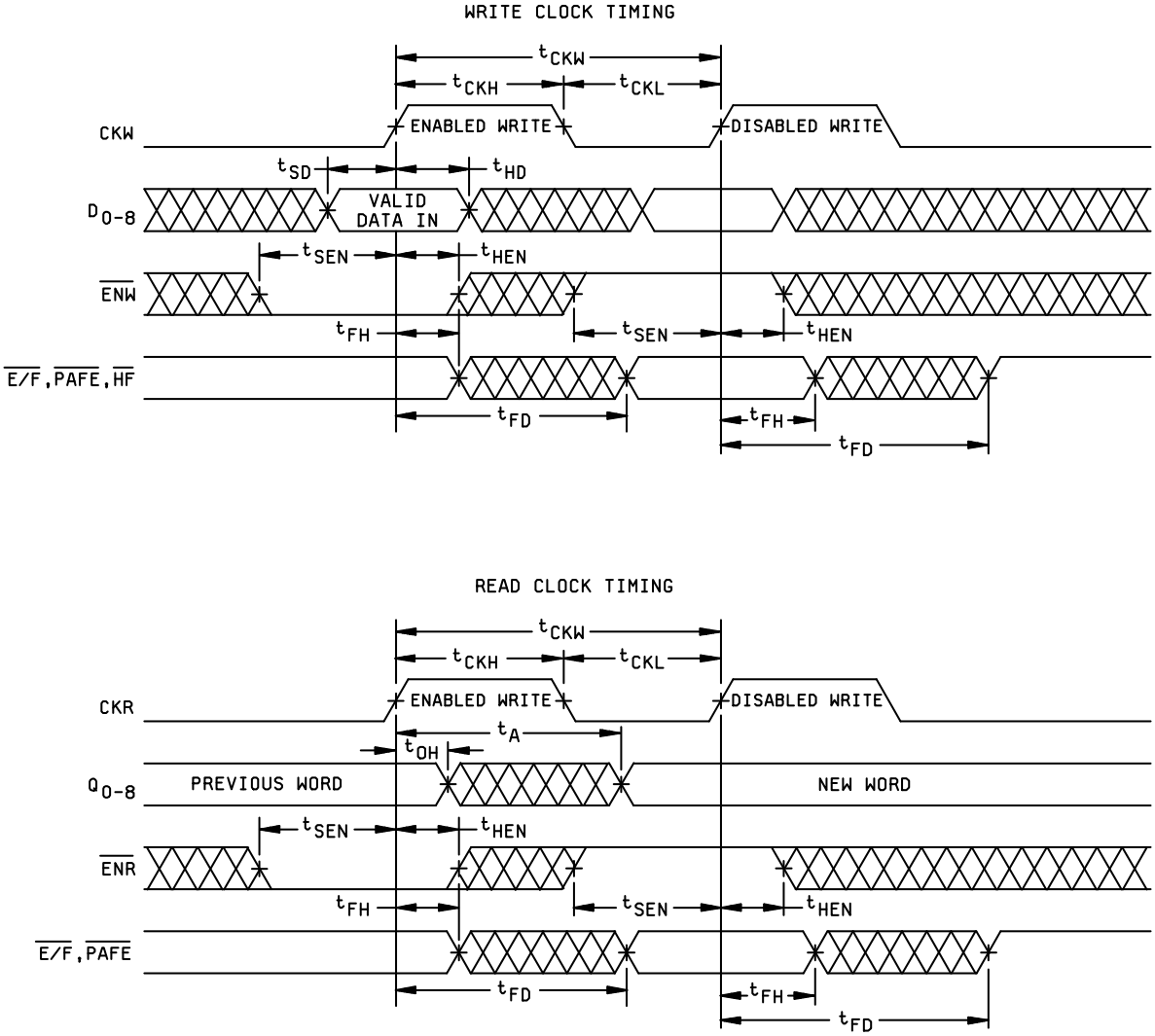


FIGURE 5. Timing waveforms.

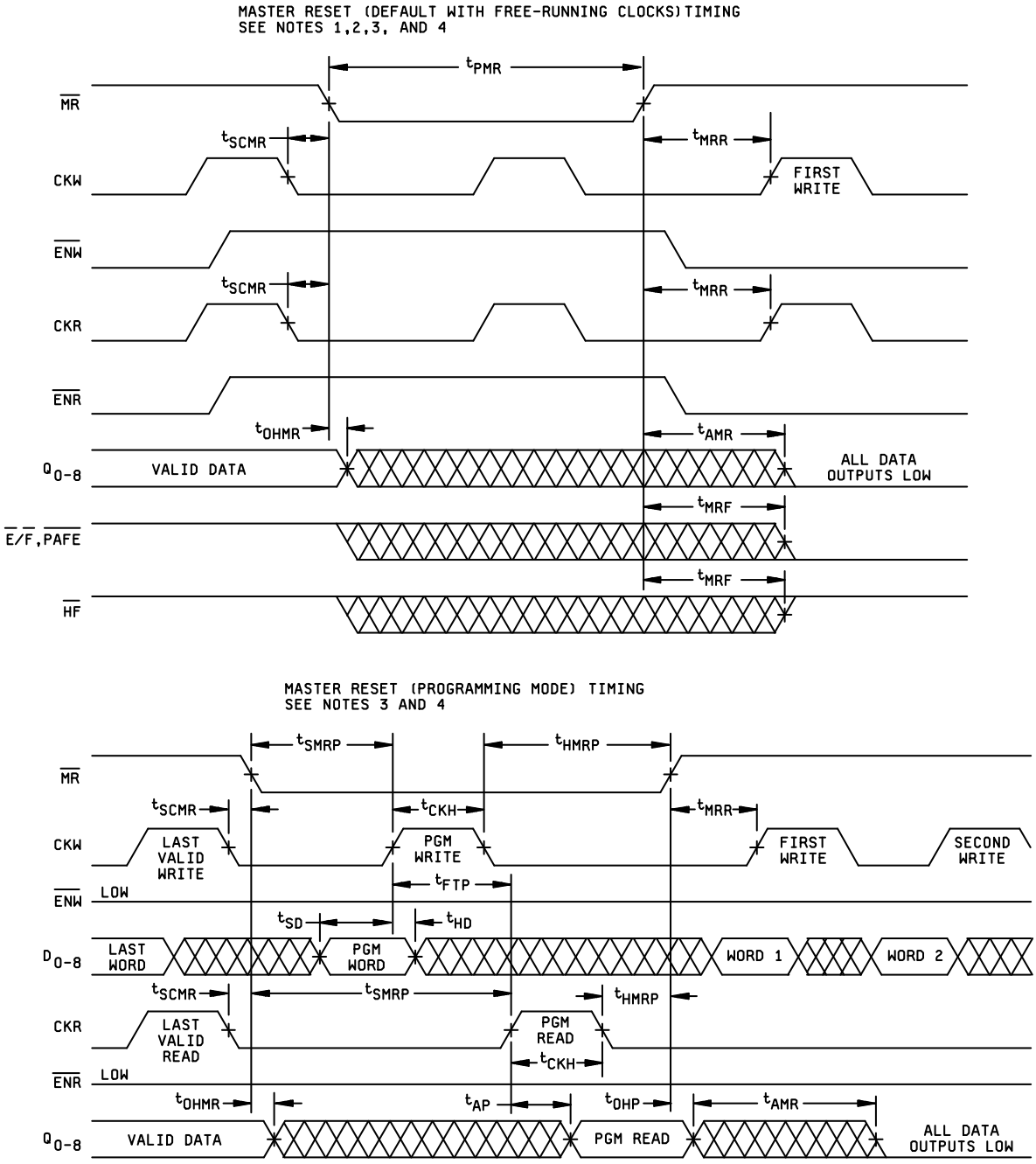


FIGURE 5. Timing waveforms – continued.

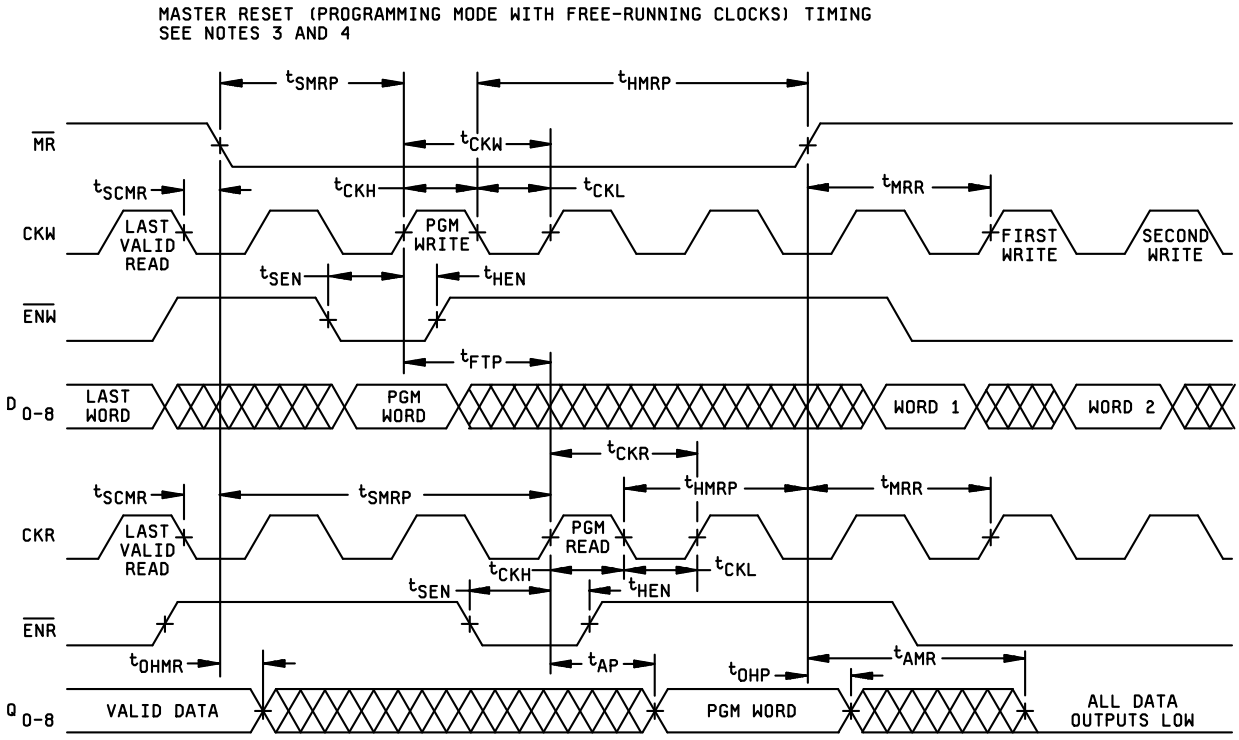
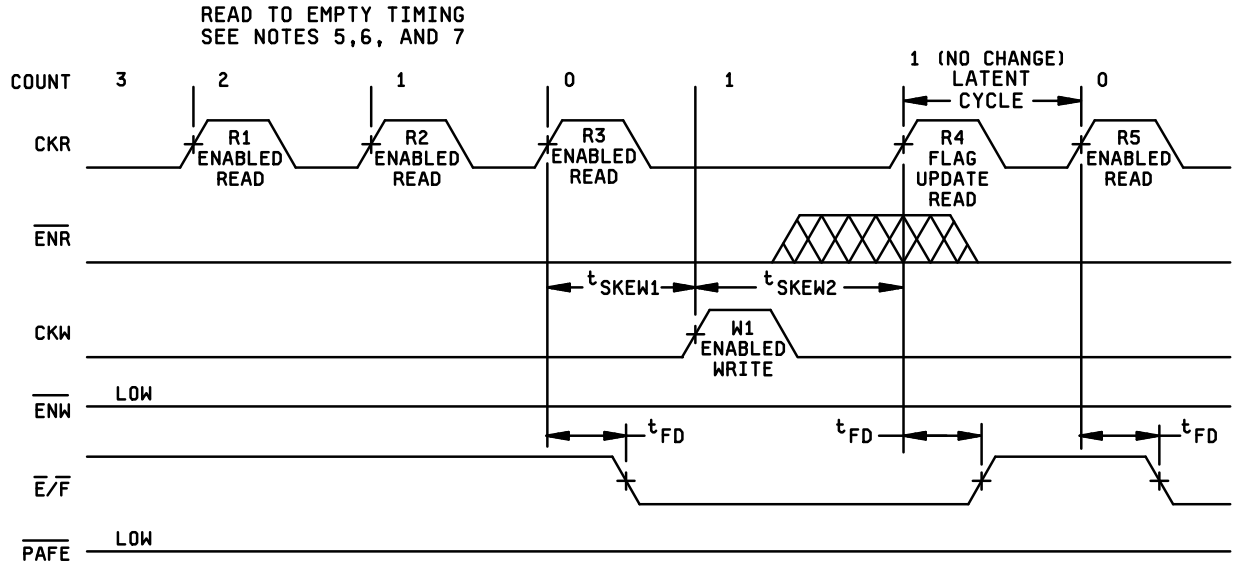


FIGURE 5. Timing waveforms – continued.



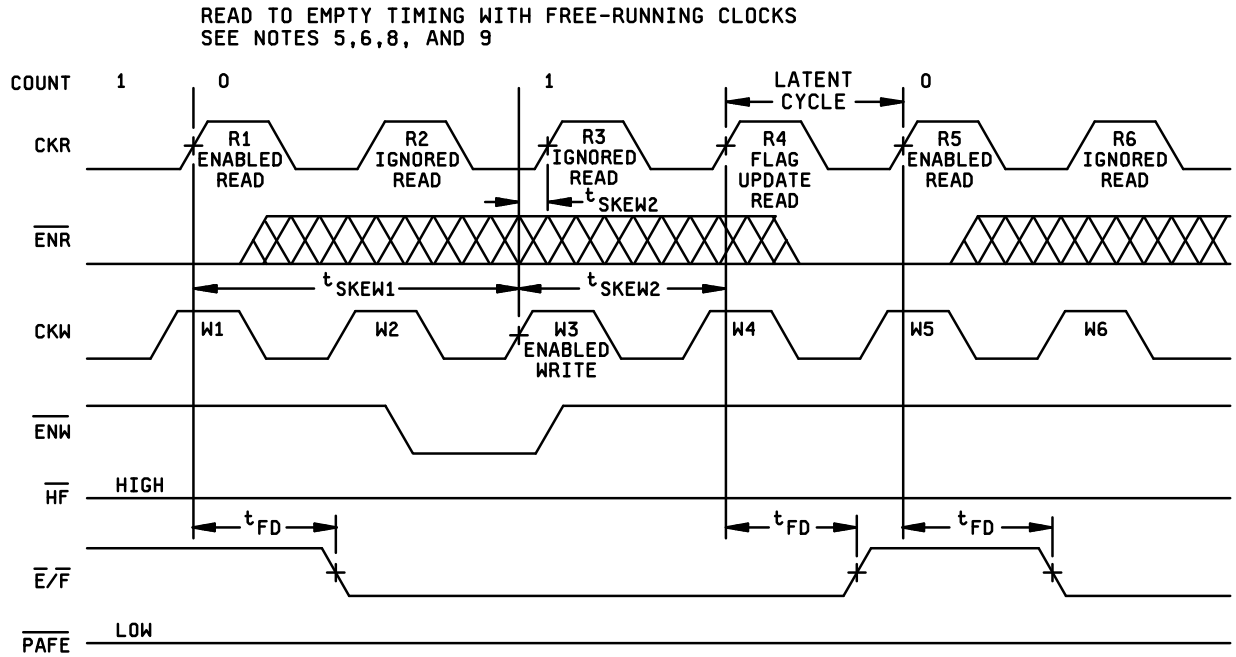


FIGURE 5. Timing waveforms – continued.

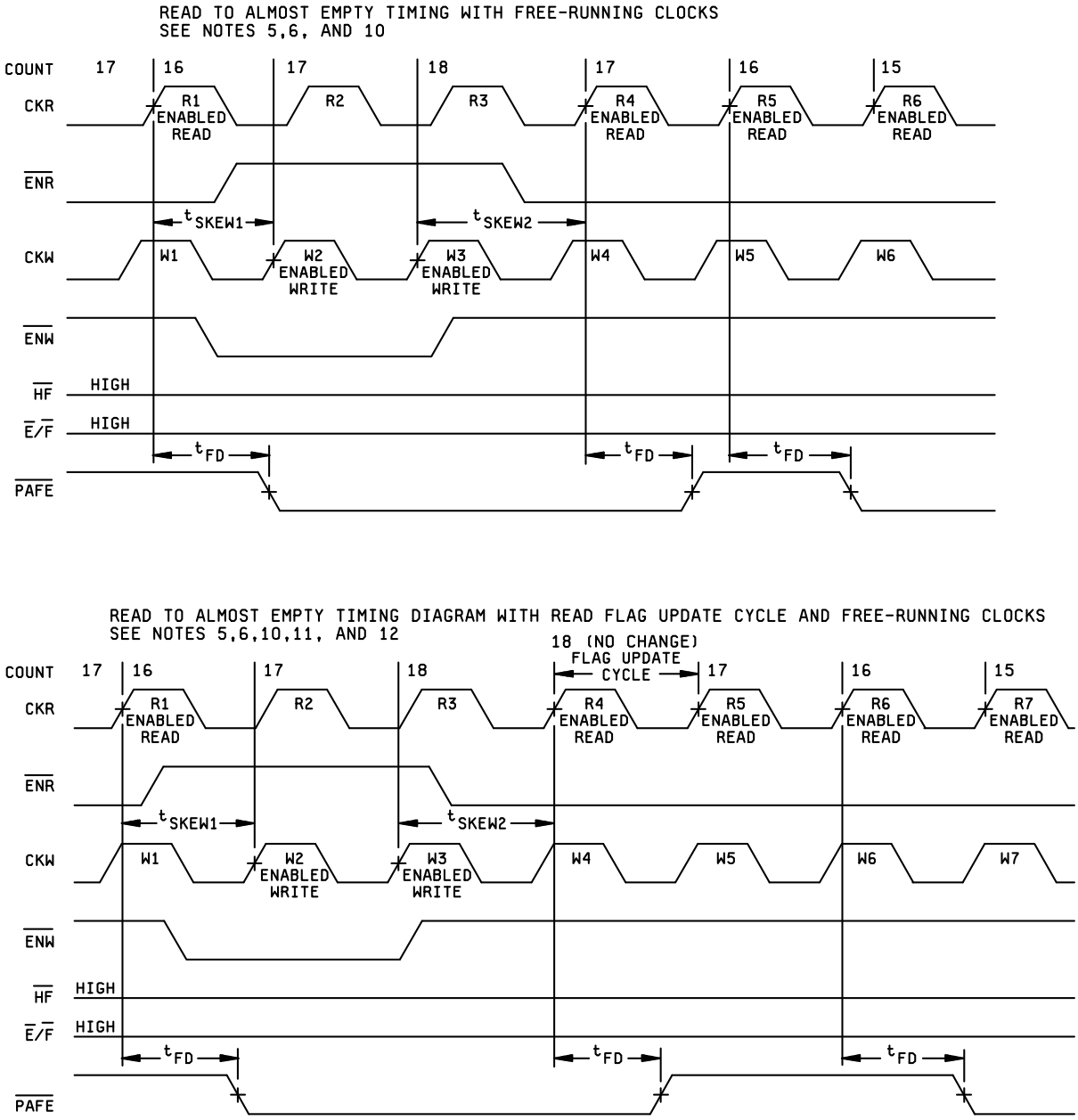


FIGURE 5. Timing waveforms – continued.

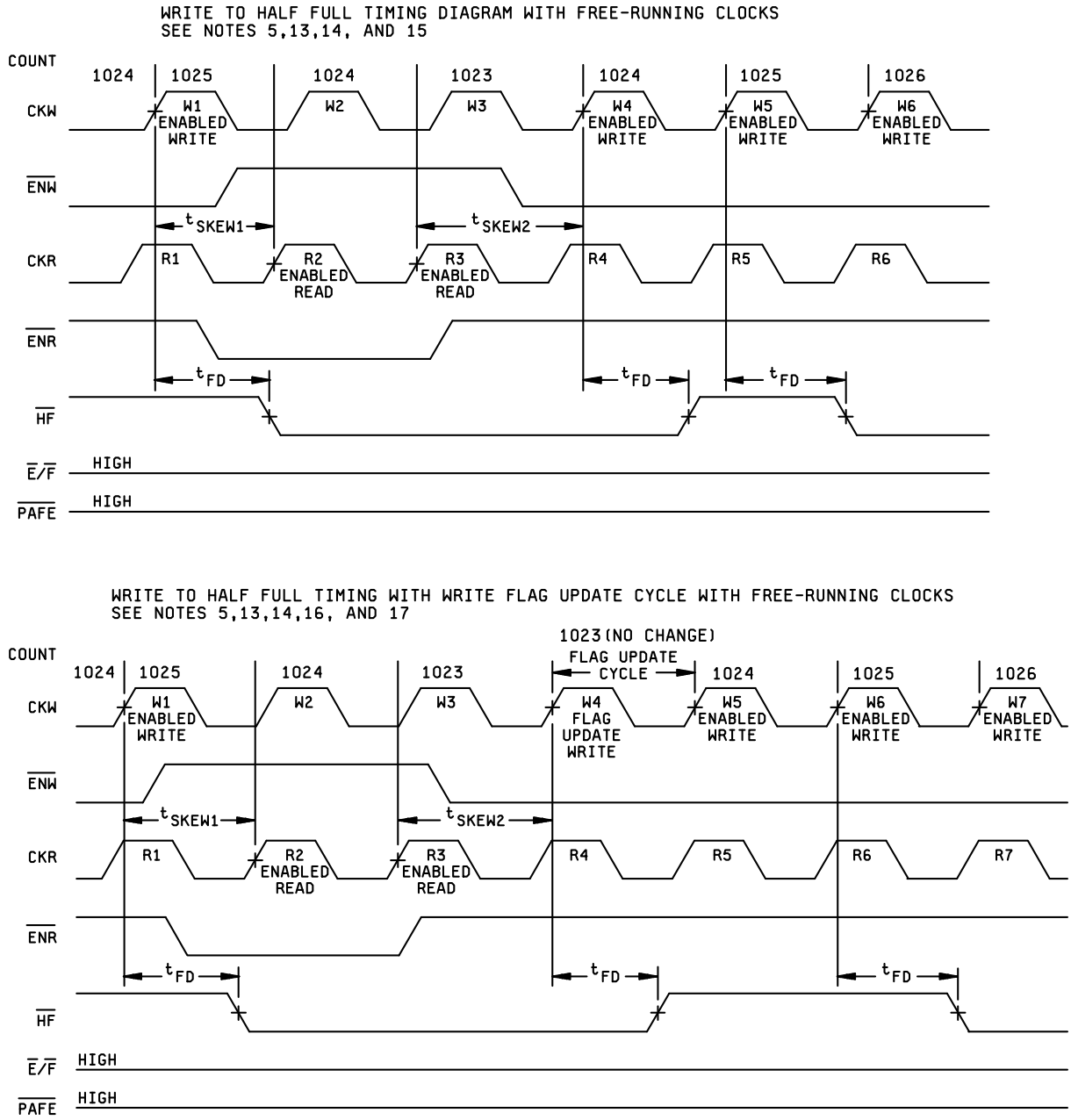


FIGURE 5. Timing waveforms – continued.

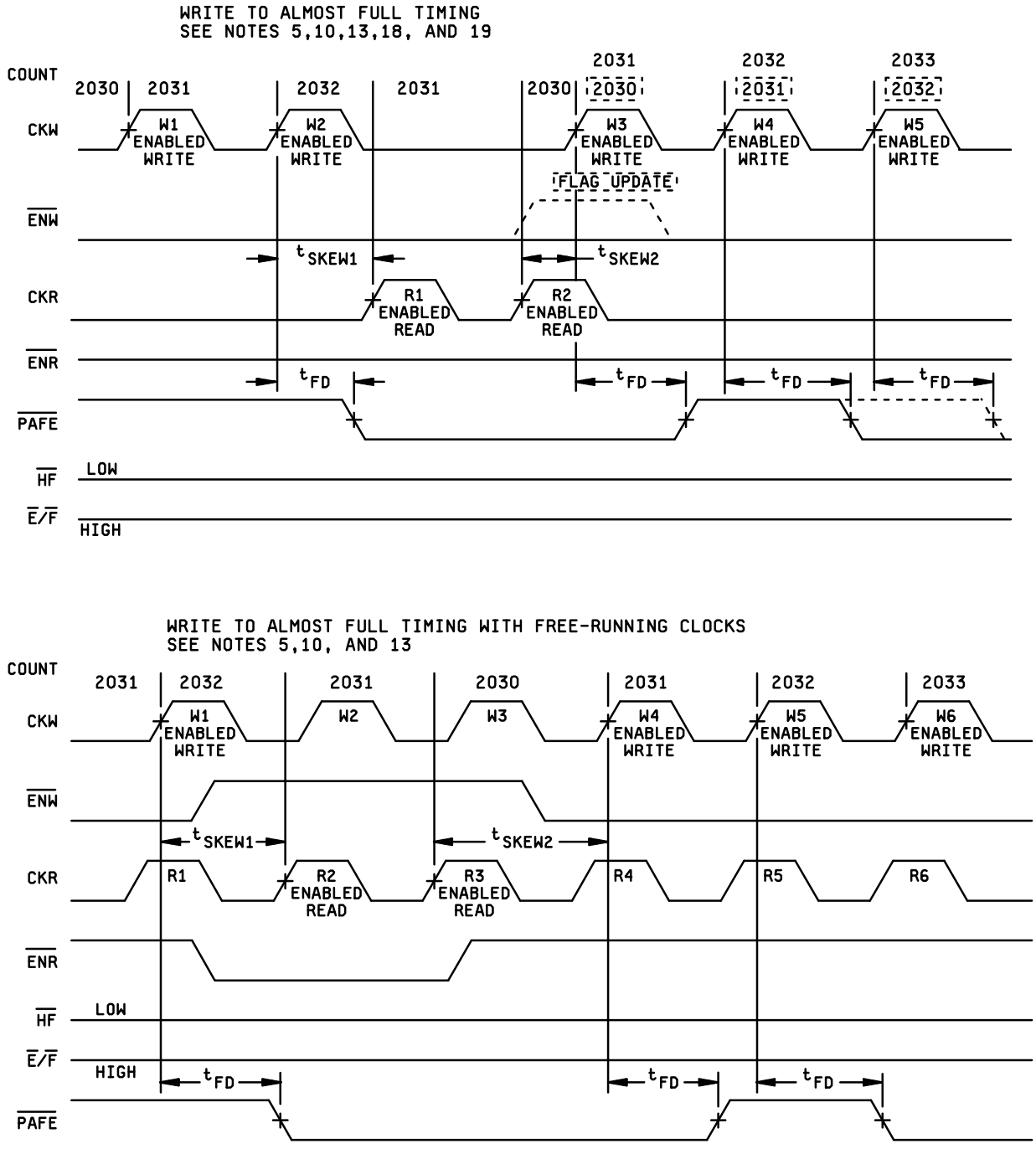
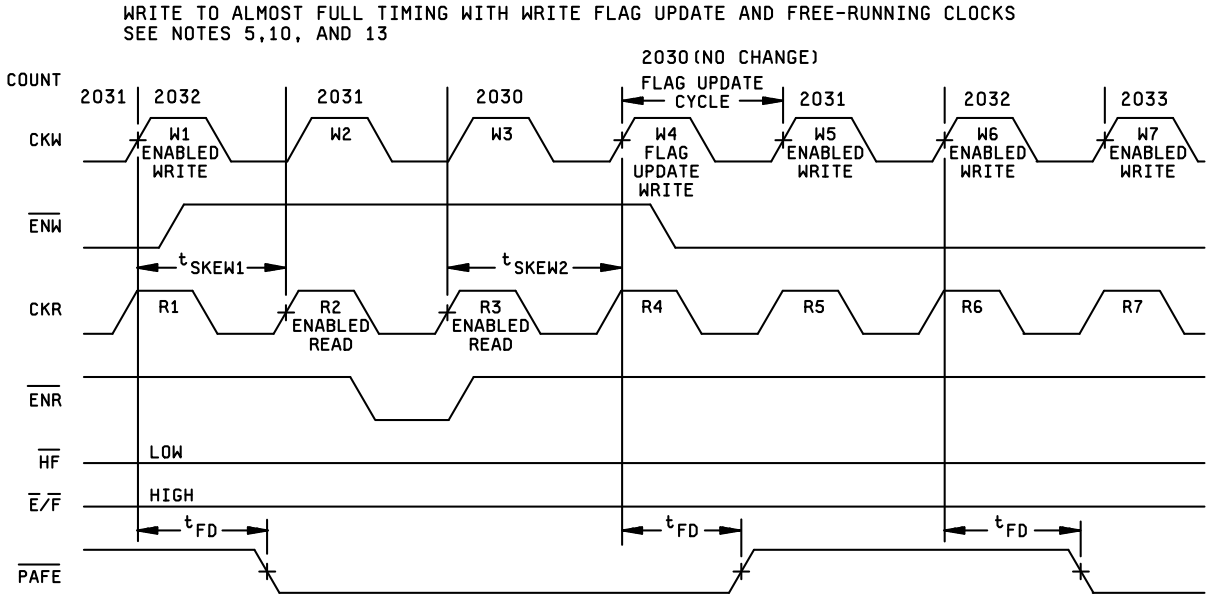


FIGURE 5. Timing waveforms – continued.



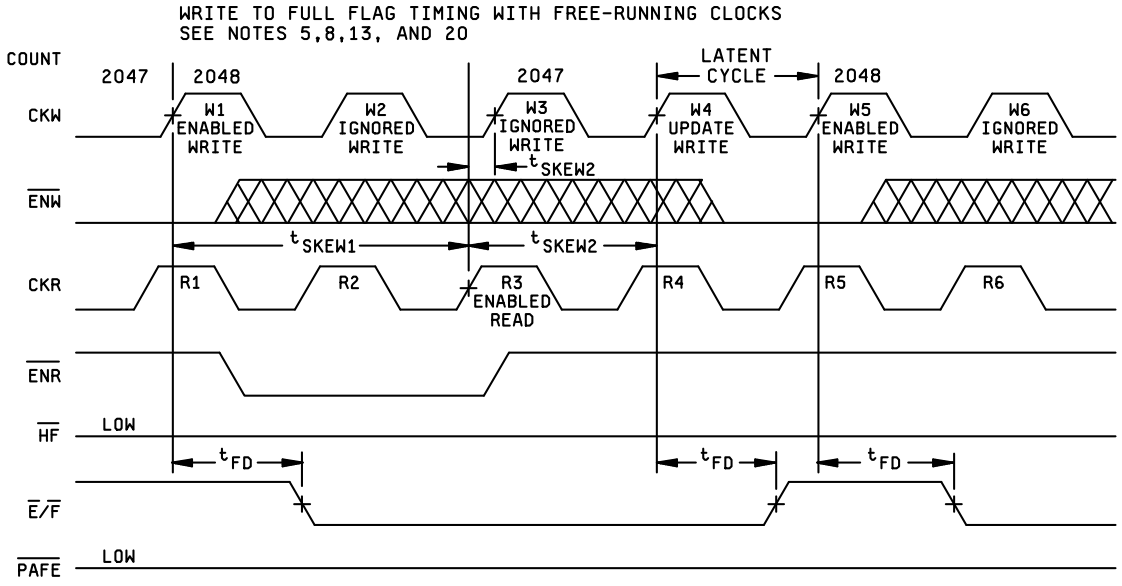


FIGURE 5. Timing waveforms – continued.

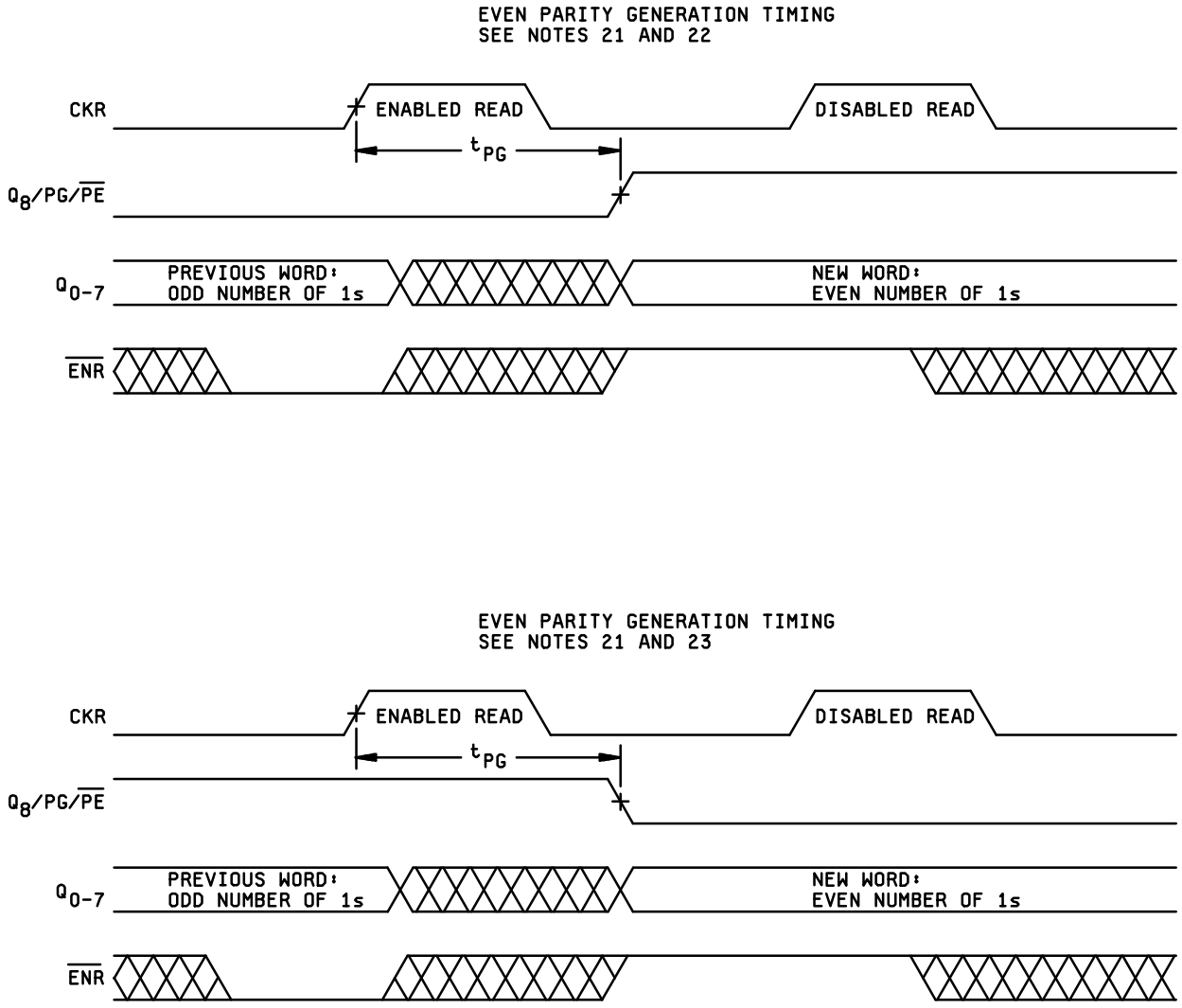
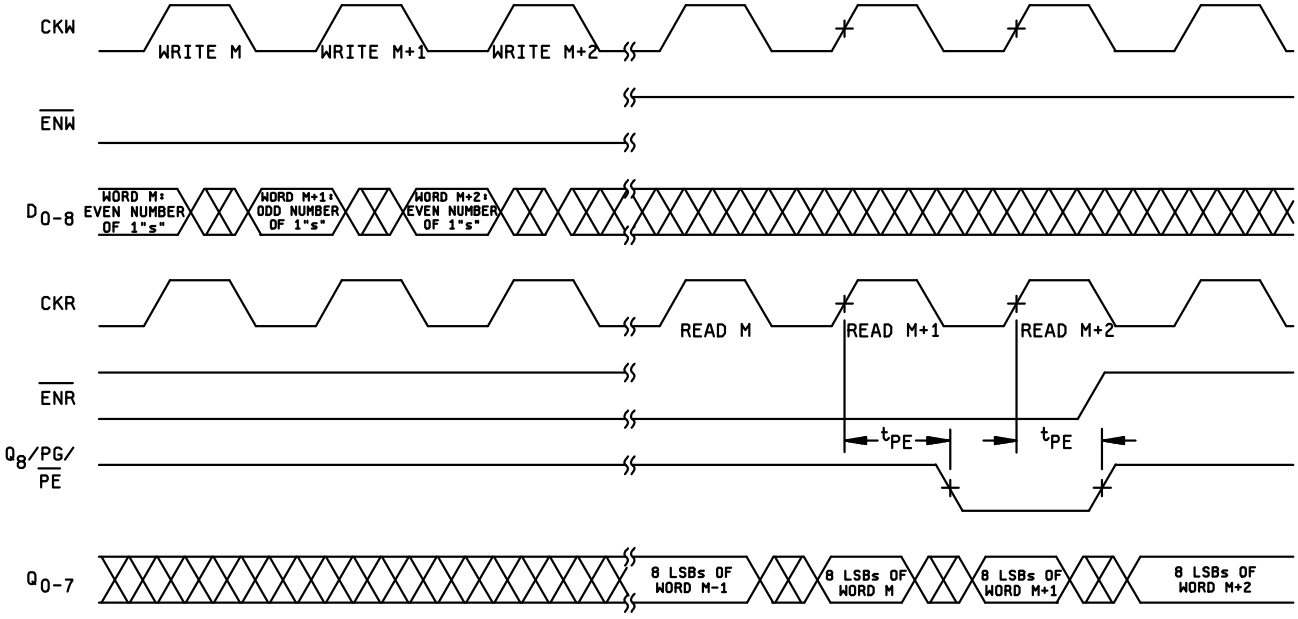


FIGURE 5. Timing waveforms – continued.

EVEN PARITY CHECKING
SEE NOTE 24



OUTPUT ENABLE TIMING
SEE NOTES 25 AND 26

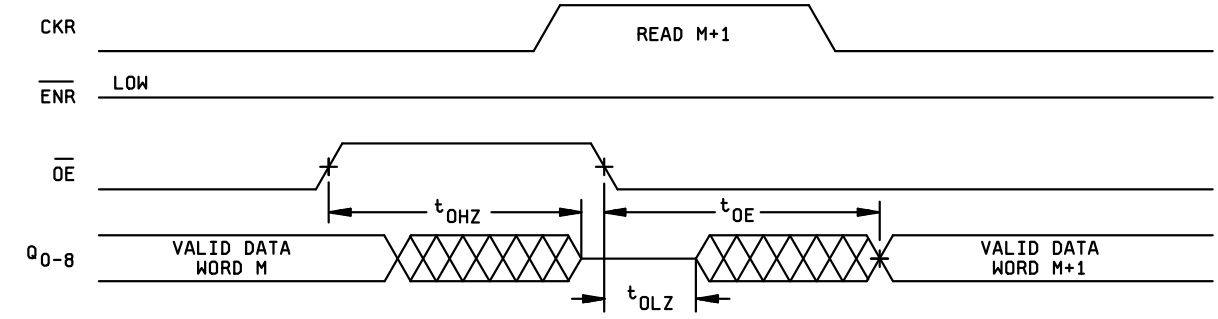


FIGURE 5. Timing waveforms – continued.

NOTES:

1/ To only perform reset (no programming), the following criteria must be met: $\overline{ENW}$ or CKW must be inactive while $\overline{MR}$ is low.

2/ To only perform reset (no programming), the following criteria must be met: $\overline{ENR}$ or CKR must be inactive while $\overline{MR}$ is low.

3/ All data outputs Q_{0-8} go low as a result of the rising edge of $\overline{MR}$ after t_{AMR}.

4/ All data outputs Q_{0-8} will remain valid until t_{OHMR} if either the first read shown did not occur or if the read occurred soon enough such that the valid data was caused by it.

5/ "Count" is the number of words in the FIFO.

6/ CKR is clock; CKW is opposite clock.

7/ R3 updates the flag to the empty state by asserting $\overline{E/F}$. Because W1 occurs greater than t_{SKEW1} after R3, R3 does not recognize W1 when updating flag status. But because W1 occurs greater than t_{SKEW2} before R4, R4 includes W1 in the flag update and, therefore, updates FIFO to almost empty state. It is important to note that R4 is a latent cycle; i.e., it only updates the flag status regardless of the state of $\overline{ENR}$. It does not change the count or the FIFO's data outputs.

8/ The FIFO is assumed to be programmed with P > 0 (i.e., $\overline{PAFE}$ does not transition at empty or full).

9/ R2 is ignored because the FIFO is empty (count = 0). It is important to note that R3 is also ignored because W3, the first enabled write after empty, occurs less than t_{SKEW2} before R3. Therefore, the FIFO still appears empty when R3 occurs. Because W3 occurs greater than t_{SKEW2} before R4, R4 includes W3 in the flag update.

10/ The FIFO is assumed to be programmed to its default flag values. Empty is 16 words from empty; almost full is 16 locations from full.

11/ R4 only updates the flag status. It does not affect the count because $\overline{ENR}$ is high.

12/ When making the transition from almost empty to intermediate, the count must increase by two (16 $\rightarrow$ 18; two enabled writes: W2, W3) before a read (R4) can update flags to the less than half full state.

13/ CKW is clock and CKR is opposite clock.

14/ Count = 257 indicates half full.

15/ When the FIFO contains 256 words, the rising edge of the next enabled write causes the $\overline{HF}$ to be true (low).

16/ The $\overline{HF}$ write flag update cycle does not affect the count because $\overline{ENW}$ is high. It only updates $\overline{HF}$ to high.

17/ When making the transition from half full to less than half full, the count must decrease by two (257 $\rightarrow$ 255; two enabled reads: R2 and R3) before a write (W4) can update flags to less than half full.

18/ W2 updates the flag to the almost full state by asserting $\overline{PAFE}$. Because R1 occurs greater than t_{SKEW1} after W2 does not recognize R1 when updating the flag status. W3 includes R2 in the flag update because R2 occurs greater than t_{SKEW2} before W3. Note that W3 does not have to be enabled to update flags.

19/ The dashed lines show W3 as a flag update write rather than an enabled write because $\overline{ENW}$ is deasserted.

20/ W2 is ignored because the FIFO is full (count = 512). It is important to note that W3 is also ignored because R3, the first enabled read after full, occurs less than t_{SKEW2} before W3. Therefore, the FIFO still appears full when W3 occurs. Because R3 occurs greater than t_{SKEW2} before W4, W4 includes R3 in the flag update.

21/ The FIFO is assumed to be programmed to generate even parity.

22/ If Q_{0-7} "new word" also has an even number of 1s, then PG stays low.

23/ If Q_{0-7} "new word" also has an odd number of 1s, then PG stays high.

24/ The FIFO is assumed to be programmed to check for even parity.

25/ This example assumes that the time from the CKR rising edge to valid word M + 1 $\geq t_A$.

26/ If ENR was high around the rising edge of CKR (i.e., read disabled), the valid data at the far right would once again be word M instead of work M + 1.

FIGURE 5. Timing waveforms – continued.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (per MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Test 1/	Device types
	All
I_{IX}	±10% of specified value in table I
I_{OZ}	±10% of specified value in table I
I_{CC3}	±10% of specified value in table I

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.5 Delta measurements for device class Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-0544.

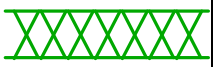
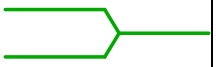
6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

C_{IN} ..... Input terminal capacitance.
C_{OUT} ..... Output terminal capacitance.
I_{CC} ..... Supply current.
I_{IX} ..... Input current.
I_{OZ} ..... Output current.
T_C ..... Case temperature.
V_{CC} ..... Positive supply voltage (5.0 V).

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-01-20

Approved sources of supply for SMD 5962-93124 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9312401MXA	3/	CY7C453-30DMB
5962-9312401MYA	3/	CY7C453-30LMB
	0C7V7	7C453-30/MYA
5962-9312401MZA	0C7V7	7C453-30/MZA
5962-9312402MXA	3/	CY7C453-20DMB
5962-9312402MYA	3/	CY7C453-20LMB
	0C7V7	7C453-20/MYA
5962-9312402MZA	0C7V7	7C453-20/MZA
5962-9312403MXA	3/	7C453-14/MXA
	3/	CY7C453-14DMB
5962-9312403MYA	0C7V7	7C453-14/MYA
	3/	CY7C453-14LMB
5962-9312403MZA	0C7V7	7C453-14/MZA

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

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