

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Corrected CAGE code typo, 67264 changed to 67268. Updated boilerplate. ksr	02-03-19	Raymond Monnin
B	Boilerplate update and part of five year review. tcr	08-02-28	Robert M. Heber

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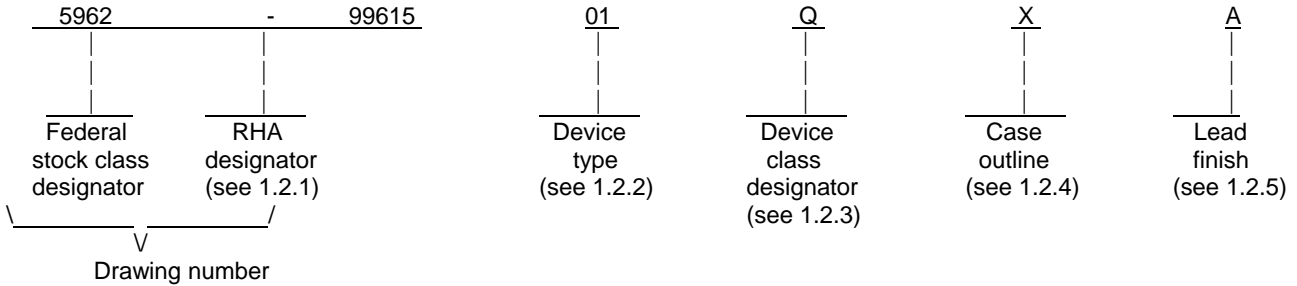
REV																			
SHEET																			
REV	B	B	B	B	B	B	B												
SHEET	15	16	17	18	19	20	21												
REV STATUS OF SHEETS				REV				B	B	B	B	B	B	B	B	B	B	B	B
				SHEET				1	2	3	4	5	6	7	8	9	10	11	12

PMIC N/A	PREPARED BY Gary L. Gross				<p align="center"><b>DEFENSE SUPPLY CENTER COLUMBUS</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.dsccl.dla.mil">http://www.dsccl.dla.mil</a></p>														
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p align="center">THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Jeff Bowling																		
	APPROVED BY Raymond Monnin				<p align="center">MICROCIRCUIT, MEMORY, DIGITAL, CMOS,          64K x 9 ASYNCHRONOUS, CASCADABLE          FIFO, MONOLITHIC SILICON</p>														
	DRAWING APPROVAL DATE 99-10-06																		
	REVISION LEVEL B				SIZE A	CAGE CODE <b>67268</b>	<b>5962-99615</b>												
				SHEET 1 OF 21															

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number 1/</u>	<u>Circuit function</u>	<u>Access time</u>
01	7C466A	64K X 9 cascable FIFO	25 ns
02	7C466A	64K X 9 cascable FIFO	15 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
Y	CQCC1-N32	32	Rectangular leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are also listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 and QML-38535 (see 6.6.2 herein).

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	SIZE <b>A</b>		<b>5962-99615</b>
		REVISION LEVEL B	SHEET 2

1.3 Absolute maximum ratings. 2/

Supply voltage range to ground potential ( $V_{CC}$ ).....	-0.5 V dc to +7.0 V dc
DC voltage range applied to outputs in high-Z state .....	-0.5 V dc to +7.0 V dc
DC input voltage range ( $V_{IN}$ ) .....	-3.0 V dc to +7.0 V dc
DC output current.....	20 mA
Maximum power dissipation .....	1.0 W
Lead temperature (soldering, 10 seconds).....	+260°C
Thermal resistance, junction-to-case ( $\theta_{JC}$ ) .....	See MIL-STD-1835
Junction temperature ( $T_J$ ).....	+175°C
Storage temperature range ( $T_{STG}$ ) .....	-65°C to +150°C
Temperature under bias range.....	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ ) .....	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND) .....	0 V dc
Input high voltage ( $V_{IH}$ ).....	2.2 V dc minimum
Input low voltage ( $V_{IL}$ ) .....	0.8 V dc maximum
Case operating temperature range ( $T_C$ ) .....	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, method 5012) .....	100 percent
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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.  
 MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).  
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	SIZE <b>A</b>		<b>5962-99615</b>
		REVISION LEVEL <b>B</b>	SHEET <b>3</b>

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-00 - Standard Guide for the Measurement of Single Event Phenomena Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; <http://www.astm.org>.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201; <http://www.jedec.org>.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	SIZE <b>A</b>		<b>5962-99615</b>
		REVISION LEVEL B	SHEET 4

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

#### 4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

##### 4.2.1 Additional criteria for device class M.

- a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.
- b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.
  - (1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D) using the circuit referenced (see 4.2.1b herein).
- c. Interim and final electrical parameters shall be as specified in table IIA herein.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	<b>SIZE A</b>		<b>5962-99615</b>
		REVISION LEVEL B	SHEET 5

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions <u>1/</u> -55°C ≤ T <sub>A</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -2.0 mA V <sub>IN</sub> = V <sub>IH</sub> , V <sub>IL</sub>	1,2,3	All	2.4		V
Output low voltage	V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 8.0 mA V <sub>IN</sub> = V <sub>IH</sub> , V <sub>IL</sub>	1,2,3	All		0.4	V
Input high voltage <u>2/</u>	V <sub>IH</sub>		1,2,3	All	2.2		V
Input low voltage <u>2/</u>	V <sub>IL</sub>		1,2,3	All		0.8	V
Input leakage current	I <sub>IX</sub>	V <sub>IN</sub> = 5.5 V to GND	1,2,3	All	-10	10	μA
Output leakage current	I <sub>OZ</sub>	V <sub>CC</sub> = 5.5 V, R̄ = V <sub>IH</sub> , V <sub>OUT</sub> = 5.5 V and GND	1,2,3	All	-10	10	μA
Operating supply current	I <sub>CC1</sub>	V <sub>CC</sub> = 5.5 V, I <sub>OUT</sub> = 0 mA, f = 20 MHz	1,2,3	All		60	mA
Standby current	I <sub>CC2</sub>	V <sub>CC</sub> = 5.5 V, I <sub>OUT</sub> = 0 mA All inputs = V <sub>IH</sub> minimum	1,2,3	All		12	mA
Power down current	I <sub>CC3</sub>	V <sub>CC</sub> = 5.5 V, I <sub>OUT</sub> = 0 mA All inputs = V <sub>CC</sub> - 0.2 V	1,2,3	All		8	mA
Input capacitance <u>3/</u>	C <sub>IN</sub>	V <sub>CC</sub> = 5.0 V, V <sub>IN</sub> = 0 V T <sub>A</sub> = +25°C, f = 1 MHz See 4.4.1e	4	All		10	pF
Output capacitance <u>3/</u>	C <sub>OUT</sub>	V <sub>CC</sub> = 5.0 V, V <sub>OUT</sub> = 0 V T <sub>A</sub> = +25°C, f = 1 MHz See 4.4.1e	4	All		12	pF
Functional tests		See 4.4.1c	7,8A,8B	All			

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	<b>SIZE A</b>		<b>5962-99615</b>
		REVISION LEVEL B	SHEET 6

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Test conditions <u>1/</u> -55°C ≤ T <sub>A</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle time	t <sub>RC</sub>	See figure 3.	9,10,11	01	35		ns
				02	25		
Access time	t <sub>A</sub>		9,10,11	01		25	ns
				02		15	
Read recovery time	t <sub>RR</sub>		9,10,11	All	10		ns
Read low to low-Z <u>3/ 4/</u>	t <sub>LZR</sub>		9,10,11	All	3		ns
Read high to data valid	t <sub>DVR</sub>		9,10,11	All	3		ns
Read high to high-Z <u>3/ 4/</u>	t <sub>HZR</sub>		9,10,11	01		18	ns
				02		15	
Read pulse width <u>5/</u>	t <sub>PR</sub>		9,10,11	01	25		ns
				02	15		
Write cycle time	t <sub>WC</sub>		9,10,11	01	35		ns
				02	25		
Write pulse width <u>5/</u>	t <sub>PW</sub>		9,10,11	01	25		ns
				02	15		
Write high to low-Z <u>3/ 4/ 6/</u>	t <sub>HWZ</sub>		9,10,11	All	5		ns
Write recovery time	t <sub>WR</sub>		9,10,11	All	10		ns
Data setup time	t <sub>SD</sub>		9,10,11	All	9		ns
Data hold time	t <sub>HD</sub>		9,10,11	All	0		ns
Master reset cycle time	t <sub>MRSC</sub>		9,10,11	01	35		ns
				02	25		
Master reset pulse width <u>5/</u>	t <sub>PMR</sub>		9,10,11	01	25		ns
				02	15		
Master reset recovery time	t <sub>RMR</sub>		9,10,11	All	10		ns
Read high to master reset high <u>7/</u>	t <sub>RPW</sub>		9,10,11	01	25		ns
				02	15		
Write high to master reset high <u>7/</u>	t <sub>WPW</sub>	9,10,11	01	25		ns	
			02	15			
Retransmit cycle time	t <sub>RTC</sub>	9,10,11	01	35		ns	
			02	25			

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	<b>SIZE A</b>		<b>5962-99615</b>
		REVISION LEVEL B	SHEET 7

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Test conditions <u>1/</u> -55°C ≤ T <sub>A</sub> ≤ +125°C +4.5 V ≤ V <sub>CC</sub> ≤ +5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Retransmit pulse width <u>4/</u>	t <sub>PRT</sub>	See figure 3.	9,10,11	01	25		ns
				02	15		
Retransmit recovery time	t <sub>RTR</sub>		9,10,11	All	10		ns
Master reset to empty flag low	t <sub>EFL</sub>		9,10,11	01		35	ns
				02		25	
Master reset to half full flag high	t <sub>HFH</sub>		9,10,11	01		35	ns
				02		25	
Master reset to full flag high	t <sub>FFH</sub>		9,10,11	01		35	ns
				02		25	
Read low to empty flag low	t <sub>REF</sub>		9,10,11	01		25	ns
				02		15	
Read high to full flag high	t <sub>RFF</sub>		9,10,11	01		25	ns
				02		15	
Write high to empty flag high	t <sub>WEF</sub>		9,10,11	01		25	ns
				02		15	
Write low to full flag low	t <sub>WFF</sub>		9,10,11	01		25	ns
				02		15	
Write low to half-full flag low	t <sub>WHF</sub>		9,10,11	01		35	ns
				02		15	
Read high to half-full flag high	t <sub>RHF</sub>		9,10,11	01		35	ns
		02			15		
Effective read from write high	t <sub>RAE</sub>	9,10,11	01		25	ns	
			02		15		
Effective read pulse width after empty flag high	t <sub>RPE</sub>	9,10,11	01	25		ns	
			02	15			
Effective write from read high	t <sub>WAF</sub>	9,10,11	01		25	ns	
			02		15		
Effective write pulse width after full flag high	t <sub>WPF</sub>	9,10,11	01	25		ns	
			02	15			
Expansion out low delay from clock <u>3/</u>	t <sub>XOL</sub>	9,10,11	01		25	ns	
			02		15		
Expansion out high delay from clock <u>3/</u>	t <sub>XOH</sub>	9,10,11	01		25	ns	
			02		15		

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	<b>SIZE A</b>		<b>5962-99615</b>
		REVISION LEVEL B	SHEET 8



TABLE I. Electrical performance characteristics – continued.

- 1/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load in figure 4, circuit A, unless otherwise specified.
- 2/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
- 3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
- 4/ Transition is measured at steady state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input, with output load figure 4 circuit B.
- 5/ Pulse widths less than minimum are not allowed.
- 6/ Only applies to read data flow-through mode.
- 7/ Values guaranteed by design and not currently tested.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	<b>SIZE A</b>		<b>5962-99615</b>
		REVISION LEVEL B	SHEET 9

Device types	
Case outlines	Y
Terminal number	Terminal symbol
1	NC
2	W
3	D <sub>8</sub>
4	D <sub>3</sub>
5	D <sub>2</sub>
6	D <sub>1</sub>
7	D <sub>0</sub>
8	$\overline{XI}$
9	$\overline{FF}$
10	Q <sub>0</sub>
11	Q <sub>1</sub>
12	NC
13	Q <sub>2</sub>
14	Q <sub>3</sub>
15	Q <sub>8</sub>
16	GND
17	NC
18	$\overline{R}$
19	Q <sub>4</sub>
20	Q <sub>5</sub>
21	Q <sub>6</sub>
22	Q <sub>7</sub>
23	$\overline{XO}/\overline{HF}$
24	$\overline{EF}$
25	$\overline{MR}$
26	$\overline{FL}/\overline{RT}$
27	NC
28	D <sub>7</sub>
29	D <sub>6</sub>
30	D <sub>5</sub>
31	D <sub>4</sub>
32	V <sub>CC</sub>

NC = no connection

FIGURE 1. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	<b>SIZE A</b>		<b>5962-99615</b>
		<b>REVISION LEVEL B</b>	<b>SHEET 10</b>

Reset and retransmit  
Single device configuration/width expansion mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{\text{MR}}$	$\overline{\text{RT}}$	$\overline{\text{XI}}$	Read Pointer	Write Pointer	$\overline{\text{EF}}$	$\overline{\text{FF}}$	$\overline{\text{HF}}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment <u>1</u> /	Increment <u>1</u> /	X	X	X

1/ Pointer will increment if flag is high.

Reset and first load truth table  
Depth expansion/compound expansion mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{\text{MR}}$	$\overline{\text{FL}}$	$\overline{\text{XI}}$	Read Pointer	Write Pointer	$\overline{\text{EF}}$	$\overline{\text{FF}}$
Reset first device	0	0	<u>1</u> /	Location zero	Location zero	0	1
Reset all other devices	0	1	<u>1</u> /	Location zero	Location zero	0	1
Read/Write	1	X	<u>1</u> /	X	X	X	X

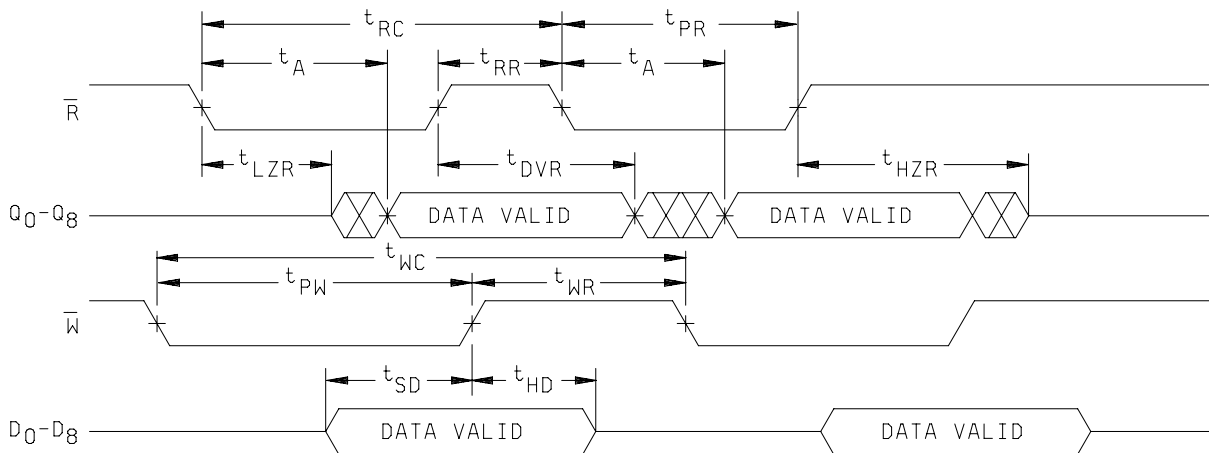
1/ XI is connected to XO of previous device.

NOTE: MR = Reset input, FL/RT = First load/retransmit EF = Empty flag output,  
 $\overline{\text{FF}}$  = Full flag output,  $\overline{\text{XI}}$  = Expansion input, and  $\overline{\text{HF}}$  = Half-full flag output  
 0 = Low level voltage  
 1 = High level voltage  
 X = Don't care

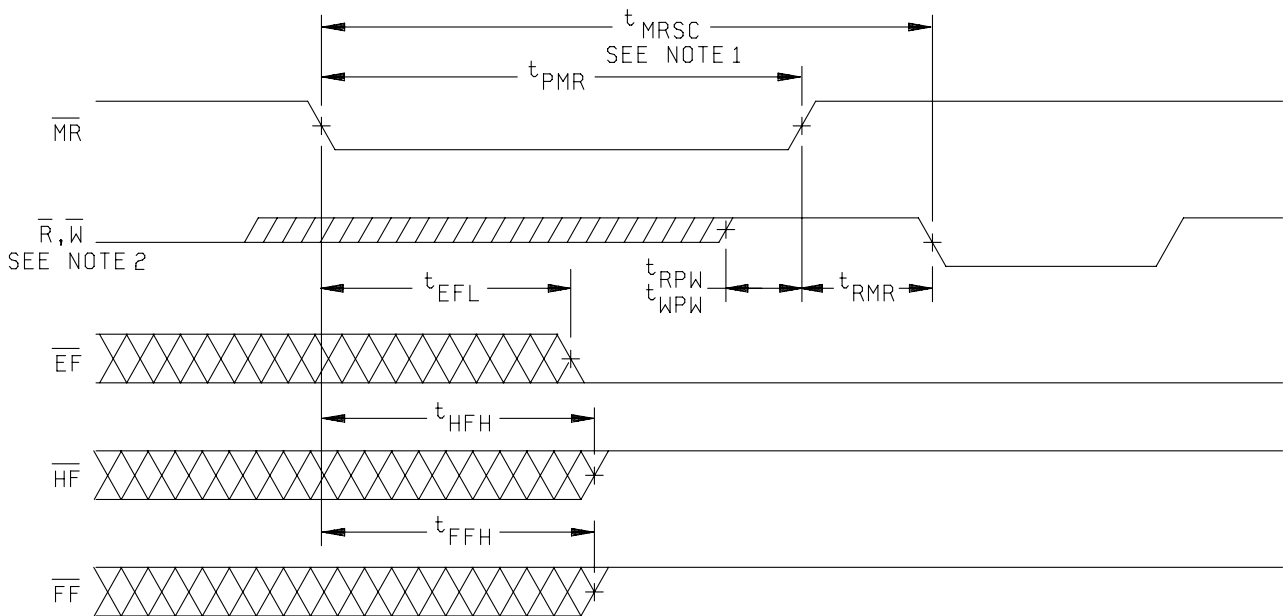
FIGURE 2. Truth tables.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	SIZE <b>A</b>		<b>5962-99615</b>
		REVISION LEVEL B	SHEET 11

Asynchronous read and write timing diagram.



Master reset timing diagram.



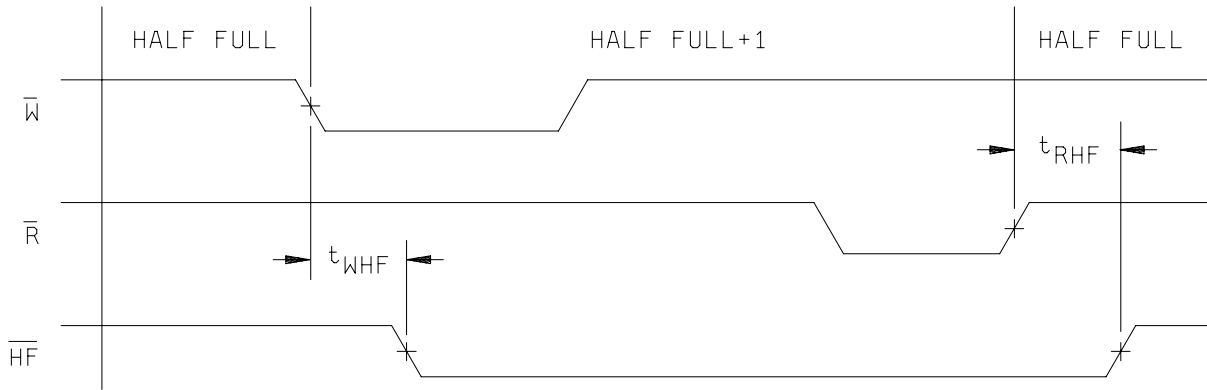
NOTES: 1.  $t_{MRSC} = t_{PMR} + t_{RMR}$ .

2.  $\bar{W}$  and  $\bar{R} = V_{IH}$  around the rising edge of  $\bar{MR}$ .

FIGURE 3. Switching waveforms.

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		REVISION LEVEL B	SHEET 12

Half-full flag timing diagram.



Last write to first read full flag timing diagram.

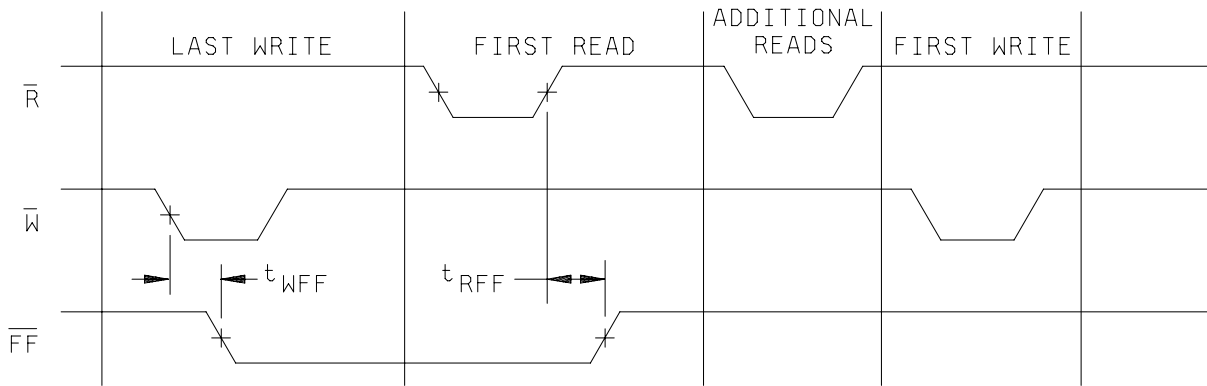
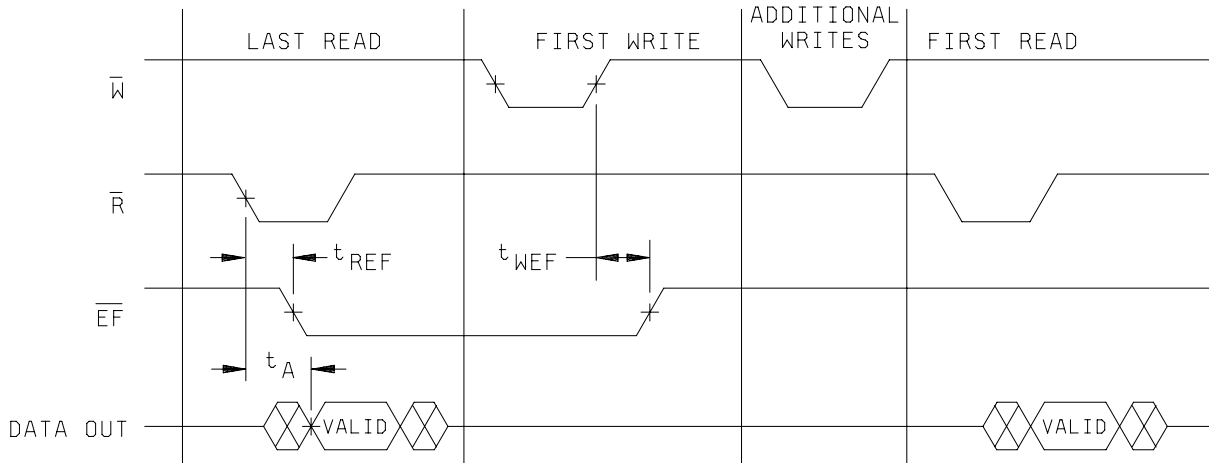


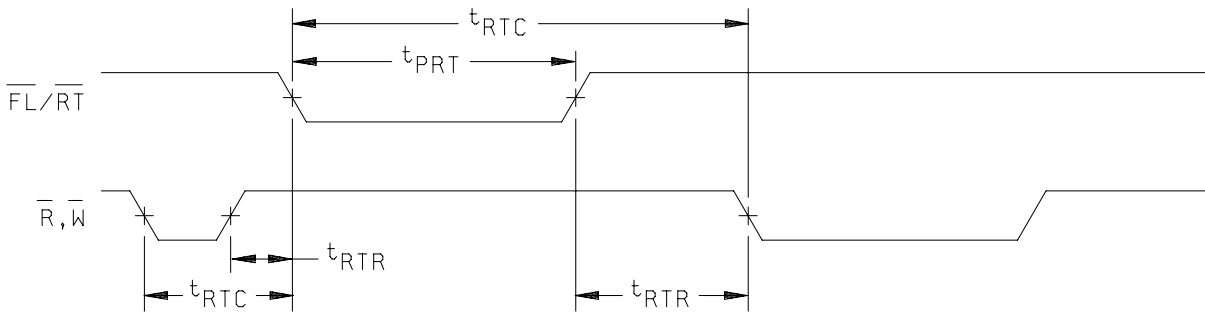
FIGURE 3. Switching waveforms - continued.

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		REVISION LEVEL B	SHEET 13

Last read to first write empty flag timing diagram.



Retransmit timing diagram.  
(see notes 1 and 2)

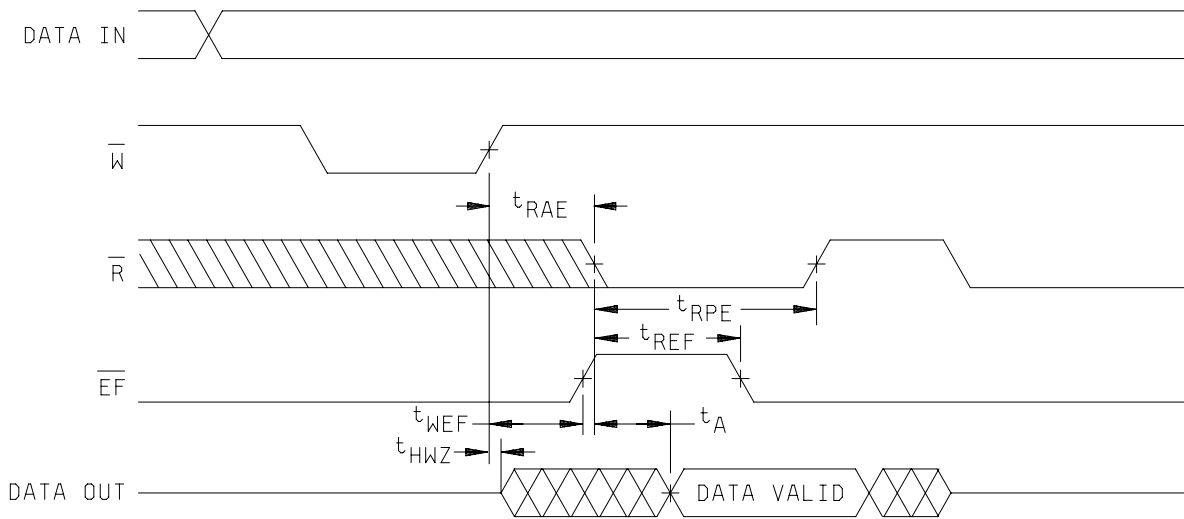


- NOTES: 1.  $t_{RTC} = t_{PRT} + t_{RTR}$ .
2.  $\overline{EF}$ ,  $\overline{HF}$  and  $\overline{FF}$  may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at  $t_{RTC}$ , with the exception of device types 03 and 06, whose flags will be valid after  $t_{RTC} + 10$  ns.

FIGURE 4. Switching waveforms - continued.

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		REVISION LEVEL B	SHEET 14

Empty flag and read data flow-through mode timing diagram.



Full flag and write data flow-through mode timing diagram

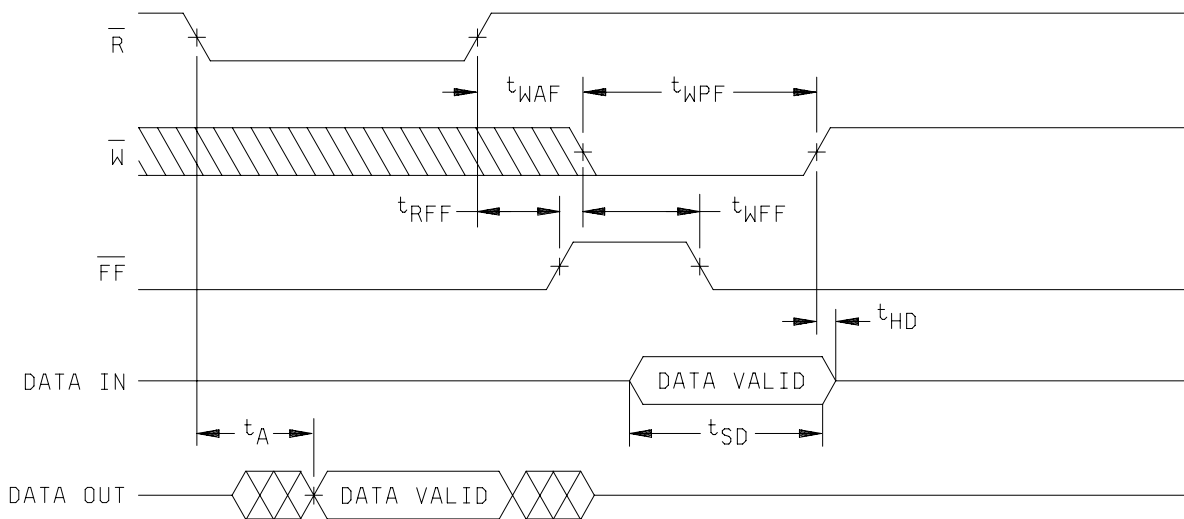
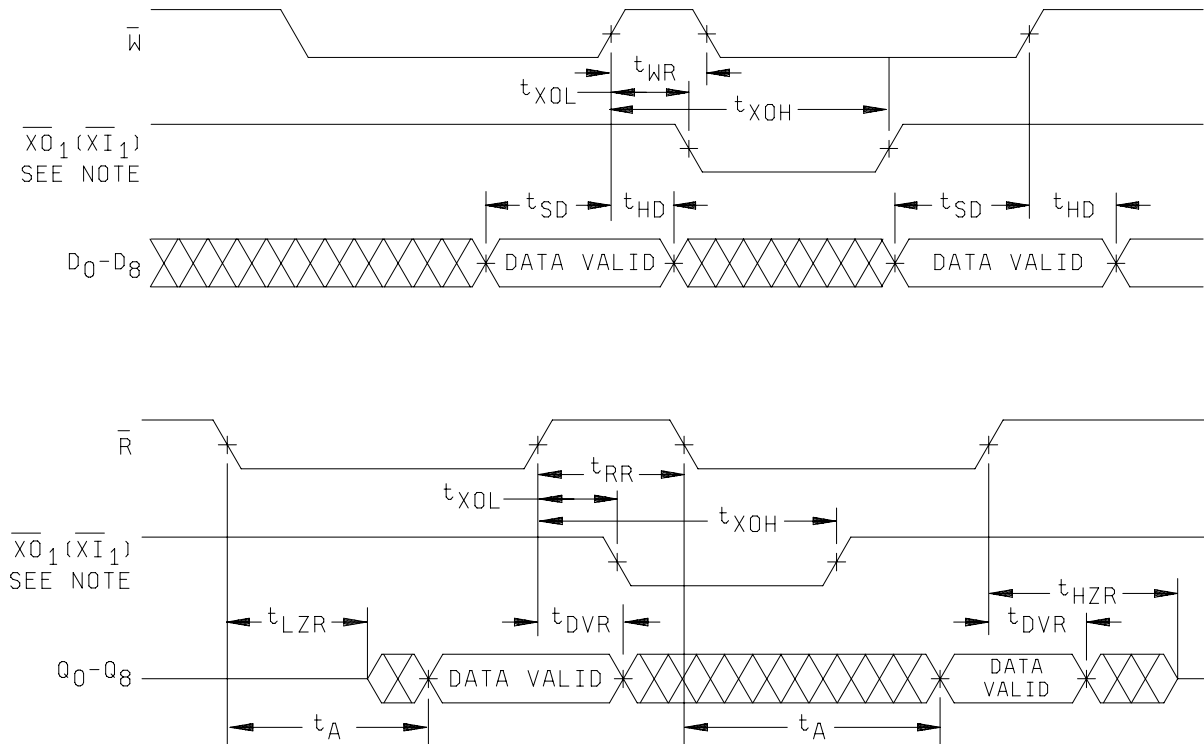


FIGURE 3. Switching waveforms - Continued.

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		REVISION LEVEL B	SHEET 15

Expansion timing diagrams.

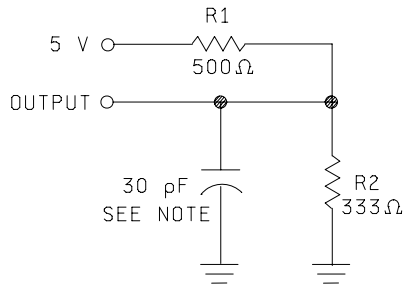


NOTE: Expansion out of device 1 (XO<sub>1</sub>) is connected to expansion in of device 2 (XI<sub>2</sub>).

FIGURE 3. Switching waveforms - Continued.

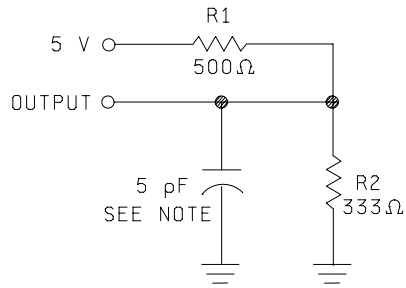
<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	<b>SIZE A</b>		<b>5962-99615</b>
		REVISION LEVEL B	SHEET 16





CIRCUIT A

NORMAL OUTPUT LOAD



CIRCUIT B

HIGH-IMPEDANCE OUTPUT LOAD

NOTE: Including scope and jig (minimum values).

AC test conditions	
Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

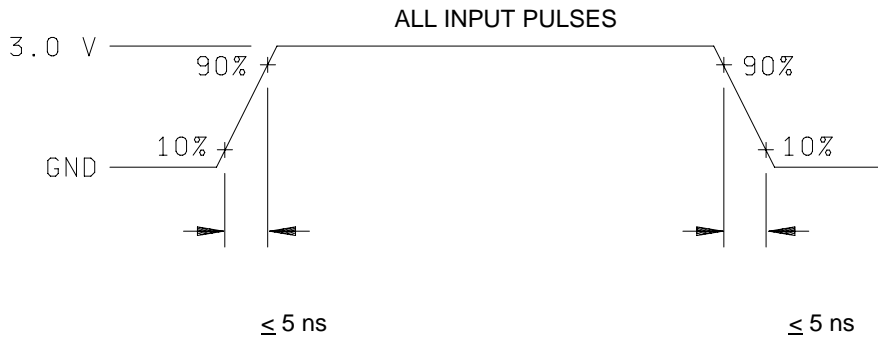


FIGURE 4. Output load circuit and test conditions.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	SIZE <b>A</b>		<b>5962-99615</b>
		REVISION LEVEL <b>B</b>	SHEET 17

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device class M, subgroups 7, 8A, and 8B tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, method 5012 (see 1.5 herein).
- d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, performance of O/V (latch-up) testing shall be as specified in the manufacturer's QM plan, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.
- e. Subgroup 4 (C<sub>IN</sub> and C<sub>OUT</sub> measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	<b>SIZE A</b>		<b>5962-99615</b>
		REVISION LEVEL B	SHEET 18

4.4.2.1 Additional criteria for device class M.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

- (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005.
- (2)  $T_A = +125^\circ\text{C}$ , minimum.
- (3) Test duration: 1,000 hours, except as specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table I)	Subgroups (per MIL-PRF-38535, table III)	
		Device Class M	Device Class Q	Device Class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I method 1015	Not required	Not required	Not required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements	1,2,3,4**,7,8A, 8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	1,2,3,7, 8A,8B,9,10, 11 Δ
9	Group D end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.

4/ \* indicates PDA applies to subgroups 1 and 7.

5/ \*\* see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

For device classes Q and V performance of delta limits shall be as specified in the manufacturer's QM plan.

7/ See 4.4.1d.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	SIZE <b>A</b>		<b>5962-99615</b>
		REVISION LEVEL B	SHEET 19

TABLE IIB. Delta limits at +25°C.

Test 1/	All device types
I <sub>CC2</sub> standby	± 10% of specified value in table I
I <sub>IX</sub>	± 10% of specified value in table I
I <sub>OZ</sub>	± 10% of specified value in table I

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T<sub>A</sub> = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replacability. Microcircuits covered by this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	SIZE <b>A</b>		<b>5962-99615</b>
		REVISION LEVEL B	SHEET 20

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

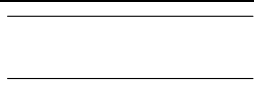
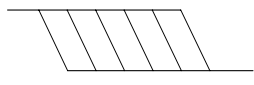
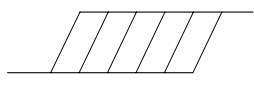
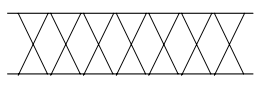
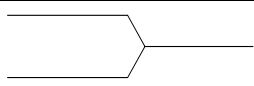
6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-STD-1331, and as follows.

- C<sub>IN</sub>.....Input terminal capacitance.
- C<sub>OUT</sub>.....Output and bidirectional output terminal capacitance.
- GND.....Ground zero voltage potential.
- I<sub>CC</sub>.....Supply current.
- I<sub>IX</sub>.....Input current.
- I<sub>OZ</sub>.....Output current.
- T<sub>C</sub>.....Case temperature.
- V<sub>CC</sub>.....Positive supply voltage.

6.5.1 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990</b>	SIZE <b>A</b>		<b>5962-99615</b>
		REVISION LEVEL B	SHEET 21

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 08-02-28

Approved sources of supply for SMD 5962-99615 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at <http://www.dscclia.mil/Programs/Smcr/>.

Standard Microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor Similar PIN <u>2/</u>
5962-9961501QYA	65786	CY7C466A-25LMB
	0C7V7	CY7C466A-25LMB
5962-9961502QYA	0C7V7	CY7C466A-15LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for the part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

Vendor name and address

65786

Cypress Semiconductor  
3901 North First Street  
San Jose, CA 95134

0C7V7

QP Semiconductor  
2945 Oakmead Village Court  
Santa Clara, CA 95051

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