REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Update boilerplate to MIL-PRF-38535 requirements. Correct title to accurately reflect device function. - CFS	05-04-06	Thomas M. Hess

CURRENT CAGE CODE 67268.

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A					
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28					

REV STATUS OF SHEETS																
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

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DRAWING APPROVAL DATE
86-05-14

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, COUNTER/TIMER AND PARALLEL I/O UNIT, N-CHANNEL, MONOLITHIC SILICON GATE

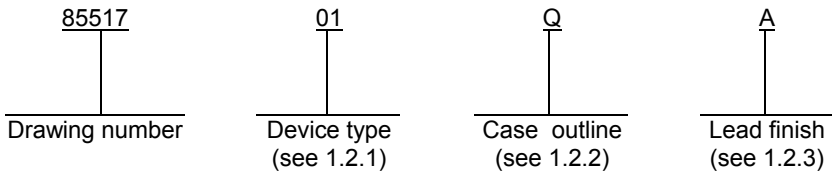
SIZE	CAGE CODE	
A	**14933**	**85517**

SHEET 1 OF 28

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	Z8036A	6.0 MHz	Counter timer and parallel I/O unit
02	Z8036	4.0 MHz	Counter timer and parallel I/O unit

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Q	GDIP1-T40 or CDIP2-T40	40	Dual-in-line
Y	CQCC1-N44	44	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range (V_{CC}) (referenced to ground) ..... -0.3 V dc to +7.0 V dc
Voltage on any pin (referenced to ground) ..... -0.3 V dc to +7.0 V dc
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) at -55°C ..... 1.2 W
Lead temperature (soldering, 10 seconds) ..... +270°C
Maximum junction temperature (T_J) at T_C = +125°C ..... +148°C
Thermal resistance, junction-to-case (θ_{JC}):
Cases Q and Y ..... See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... +4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH}) ..... 2.2 V dc
Maximum low level input voltage (V_{IL}) ..... 0.8 V dc
Frequency of operation:
Device type 01 ..... 0.5 to 6.0 MHz
Device type 02 ..... 0.5 to 4.0 MHz
Case operating temperature range (T_C) ..... -55°C to +125°C
Clock rise and fall times:
Device type 01 ..... 10 ns maximum fall; 15 ns maximum rise
Device type 02 ..... 20 ns maximum

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figures 3 (3a – 3g).

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions V_{CC} = 5.0 V ±10%, -55ºC ≤ T_C ≤ +125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
High level input voltage	V_{IH}		All	1, 2, 3	2.2	V_{CC} + 0.3 1/	V
Low level input voltage	V_{IL}				-0.3 1/	0.8	
Low level output voltage	V_{OL}	I_{OL} = 2.0 mA				0.4	
High level output voltage	V_{OH}	I_{OH} = -250 µA			2.4		
Power supply current	I_{CC}	V_{CC} = 5.5 V T_C = -55°C	All	1, 2, 3		200	mA
Output leakage current low	I_{LOL}	V_{IN} = 0.4 V	All	1, 2, 3	-10	+10	µA
Output leakage current high	I_{LOH}	V_{IN} = 2.4 V			-10	+10	
Input low current	I_{IL}	V_{IN} = 0.4 V			-10	+10	
Input high current	I_{IH}	V_{IN} = 2.4 V			-10	+10	
Maximum frequency low output current 1/	f_{MAX}		01	9, 10, 11	6.0		MHz
			02		4.0		
Input capacitance 2/	C_{IN}		All	4		10	pF
Output capacitance 2/	C_{OUT}					15	
Bidirectional capacitance 2/	$C_{I/O}$					20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{CC} = 5.0 V ±10%, -55ºC ≤ T_C ≤ +125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
AS low width	TwAS	Reference number 1. 3/ 4/ 5/	01	9, 10, 11	50	2000	ns
			02		70	2000	
Address to $\overline{AS}$ ↑ setup time 6/	TsA(AS)	Reference number 2. 3/ 4/ 5/	01	9, 10, 11	10		ns
			02		30		
Address to $\overline{AS}$ ↑ hold time 6/	ThA(AS)	Reference number 3. 3/ 4/ 5/	01	9, 10, 11	30		ns
			02		50		
Address to $\overline{DS}$ ↓ setup time 2/ 6/	TsA(DS)	Reference number 4. 3/ 4/ 5/	01	9, 10, 11	100		ns
			02		130		
$\overline{CS0}$ to $\overline{AS}$ ↑ hold time 2/ 6/	TsCS0(AS)	Reference number 5. 3/ 4/ 5/	01	9, 10, 11	0		ns
			02		0		
$\overline{CS0}$ to $\overline{AS}$ ↑ hold time 6/	ThCS0(AS)	Reference number 6. 3/ 4/ 5/	01	9, 10, 11	40 2/		ns
			02		60		
$\overline{AS}$ ↑ to $\overline{DS}$ ↓ delay 2/ 6/	TdAS(DS)	Reference number 7. 3/ 4/ 5/	01	9, 10, 11	55		ns
			02		85		
CS1 to $\overline{DS}$ ↓ setup time	TsCS1(DS)	Reference number 8. 3/ 4/ 5/	01	9, 10, 11	80 2/		ns
			02		100		
R/$\overline{W}$ (Read) to $\overline{DS}$ ↓ setup time	TsRWR(DS)	Reference number 9. 3/ 4/ 5/	01	9, 10, 11	80		ns
			02		100		
R/$\overline{W}$ (Write) to $\overline{DS}$ ↓ setup time 2/	TsRWW(DS)	Reference number 10. 3/ 4/ 5/	01	9, 10, 11	0		ns
			02		0		
$\overline{DS}$ low width 2/	TwDS	Reference number 11. 3/ 4/ 5/	01	9, 10, 11	250		ns
			02		390		
Write data to $\overline{DS}$ ↓ setup time 2/	TsDW(DSf)	Reference number 12. 3/ 4/ 5/	01	9, 10, 11	20		ns
			02		30		
$\overline{DS}$ (Read) ↓ to address data bus driven 2/	TdDS(DRV)	Reference number 13. 3/ 4/ 5/	01	9, 10, 11	0		ns
			02		0		
$\overline{DS}$ ↓ to read data valid delay 2/	TdDSf(DR)	Reference number 14. 3/ 4/ 5/	01	9, 10, 11		180	ns
			02			250	
Write data to $\overline{DS}$ ↑ hold time 2/	ThDW(DS)	Reference number 15. 3/ 4/ 5/	01	9, 10, 11	20		ns
			02		30		
$\overline{DS}$ ↑ to read data not valid delay 2/	TdDSr(DR)	Reference number 16. 3/ 4/ 5/	01	9, 10, 11	0		ns
			02		0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{CC} = 5.0 V ±10%, -55ºC ≤ T_C ≤ +125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
$\overline{DS}$ ↑ to read data float delay 2/ 7/	TdDS(DRz)	Reference number 17. 3/ 4/ 5/	01	9, 10, 11		45	ns
			02			70	
R/$\overline{W}$ to $\overline{DS}$ ↑ hold time 2/	ThRW(DS)	Reference number 18. 3/ 4/ 5/	01	9, 10, 11	40		ns
			02		55		
CS1 to $\overline{DS}$ ↑ hold time 2/	ThCS1(DS)	Reference number 19. 3/ 4/ 5/	01	9, 10, 11	40		ns
			02		55		
$\overline{DS}$ ↑ to $\overline{AS}$ ↓ delay 2/	TdDS(AS)	Reference number 20. 3/ 4/ 5/	01	9, 10, 11	25		ns
			02		50		
Valid access recovery time 2/ 8/	TrC	Reference number 21. 3/ 4/ 5/	01	9, 10, 11	650		ns
			02		1000		
Pattern match to $\overline{INT}$ delay (bit port) 2/ 9/	TdPM(INT)	Reference number 22. 3/ 4/ 5/	01	9, 10, 11		1 + 800	ns
			02			1 + 800	
$\overline{ACKIN}$ to $\overline{INT}$ delay (port with handshake) 2/ 9/ 10/	TdACK(INT)	Reference number 23. 3/ 4/ 5/	01	9, 10, 11		4 + 600	ns
			02			4 + 600	
Counter input to $\overline{INT}$ delay (counter mode) 2/ 9/	TdC1(INT)	Reference number 24. 3/ 4/ 5/	01	9, 10, 11		1 + 700	ns
			02			1 + 700	
PCLK to $\overline{INT}$ delay (timer mode) 2/ 9/	TdPC(INT)	Reference number 25. 3/ 4/ 5/	01	9, 10, 11		1 + 700	ns
			02			1 + 700	
$\overline{AS}$ to $\overline{INT}$ delay 2/	TdAS(INT)	Reference number 26. 3/ 4/ 5/	01	9, 10, 11			ns
			02			300	
$\overline{INTACK}$ to $\overline{AS}$ ↑ setup time	Ts1A(AS)	Reference number 27. 3/ 4/ 5/	01	9, 10, 11	0 2/		ns
			02		0		
$\overline{INTACK}$ to $\overline{AS}$ ↑ hold time	Th1A(AS)	Reference number 28. 3/ 4/ 5/	01	9, 10, 11	250		ns
			02		250		
$\overline{AS}$ ↑ to $\overline{DS}$ (acknowledge) setup time 2/ 11/	TsAS(DSA)	Reference number 29. 3/ 4/ 5/	01	9, 10, 11	250		ns
			02		350		
$\overline{DS}$ (acknowledge) ↓ to read data valid delay 2/	TdDSA(DR)	Reference number 30. 3/ 4/ 5/	01	9, 10, 11		180	ns
			02			250	
$\overline{DS}$ (acknowledge) low width 2/	TwDSA	Reference number 31. 3/ 4/ 5/	01	9, 10, 11	250		ns
			02		390		
$\overline{AS}$ ↑ to IEO ↓ delay $\overline{INTACK}$ cycle 2/ 11/	TdAS(IEO)	Reference number 32. 3/ 4/ 5/	01	9, 10, 11		250	ns
			02			350	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{CC} = 5.0 V ±10%, -55ºC ≤ T_C ≤ +125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
IEI to IEO delay 2/ 11/	TdIEI(IEO)	Reference number 33. 3/ 4/ 5/	01	9, 10, 11		100	ns
			02			150	
IEO to $\overline{DS}$ (acknowledge) ↓ setup time 2/ 11/	TsIEI(DSA)	Reference number 34. 3/ 4/ 5/	01	9, 10, 11	70		ns
			02		100		
IEI to $\overline{DS}$ (acknowledge) ↑ hold time 2/	ThIEI(DSA)	Reference number 35. 3/ 4/ 5/	01	9, 10, 11	70		ns
			02		100		
$\overline{DS}$ (acknowledge) to INT ↑ delay 2/	TdDSA(INT)	Reference number 36. 3/ 4/ 5/	01	9, 10, 11		600	ns
			02			600	
Data input to $\overline{ACKIN}$ ↓ setup time 2/	TsDI(ACK)	Reference number 1. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		
Data input to $\overline{ACKIN}$ ↓ hold time – strobed handshake 2/	ThDI(ACK)	Reference number 2. 3/ 4/ 12/	01	9, 10, 11			ns
			02		500		
$\overline{ACKIN}$ ↓ to RFD ↓ delay 2/	TdACKf(RFD)	Reference number 3. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		
$\overline{ACKIN}$ low width – strobed handshake 2/	TwACKI	Reference number 4. 3/ 4/ 12/	01	9, 10, 11			ns
			02		250		
$\overline{ACKIN}$ high width – strobed handshake 2/	TwACKI	Reference number 5. 3/ 4/ 12/	01	9, 10, 11			ns
			02		250		
RFD ↑ to $\overline{ACKIN}$ ↓ delay 2/	TdRFDr(ACK)	Reference number 6. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		
Data out to $\overline{DAV}$ ↓ setup time 2/ 13/	TsDO(DAV)	Reference number 7. 3/ 4/ 12/	01	9, 10, 11	20		ns
			02		25		
$\overline{DAV}$ ↓ to $\overline{ACKIN}$ ↓ delay 2/	TdDAVf(ACK)	Reference number 8. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		
Data out to $\overline{ACKIN}$ ↓ hold time 2/ 14/	ThDO(ACK)	Reference number 9. 3/ 4/ 12/	01	9, 10, 11	1		ns
			02		1		
$\overline{ACKIN}$ ↓ to $\overline{DAV}$ ↑ delay 2/ 14/	TdACK(DAV)	Reference number 10. 3/ 4/ 12/	01	9, 10, 11	1		ns
			02		1		
Data input to RFD ↓ hold time – interlocked handshake 2/	ThDI(RFD)	Reference number 11. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{CC} = 5.0 V ±10%, -55ºC ≤ T_C ≤ +125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
RFD ↓ to $\overline{\text{ACKIN}}$ ↑ delay – interlocked handshake 2/	TdRFDf(ACK)	Reference number 12. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		
$\overline{\text{ACKIN}}$ ↑ ($\overline{\text{DAV}}$ ↑) to RFD ↑ delay – interlocked and 3-wire handshake 2/	TdACKr(RFD)	Reference number 13. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		
$\overline{\text{DAV}}$ ↑ to $\overline{\text{ACKIN}}$ ↑ (RFD ↑) interlocked and 3-wire handshake 2/	TdDAVr(ACK)	Reference number 14. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		
$\overline{\text{ACKIN}}$ ↑ (RFD ↑) to $\overline{\text{DAV}}$ ↓ delay - interlocked and 3-wire handshake 2/	TdACK(DAV)	Reference number 15. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		
$\overline{\text{DAV}}$ ↓ to DAC ↑ delay input 3-wire handshake 2/	TdDAVlf(DAC)	Reference number 16. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		
Data input to DAC ↑ hold time - 3-wire handshake 2/	ThDI(DAC)	Reference number 17. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		
DAC ↑ to $\overline{\text{DAV}}$ ↑ delay input - 3-wire handshake 2/	TdDACOr(DAV)	Reference number 18. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		
$\overline{\text{DAV}}$ ↑ to DAC ↓ delay input 3-wire handshake 2/	TdDAVIr(DAC)	Reference number 19. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		
$\overline{\text{DAV}}$ ↓ to DAC ↑ delay output 3-wire handshake 2/	TdDAVOf(DAC)	Reference number 20. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		
Data output to DAC ↑ hold time - 3-wire handshake 2/ 14/	ThDO(DAC)	Reference number 21. 3/ 4/ 12/	01	9, 10, 11	1		ns
			02		1		
DAC ↑ to $\overline{\text{DAV}}$ ↑ delay output - 3-wire handshake 2/	TdDACIr(DAV)	Reference number 22. 3/ 4/ 12/	01	9, 10, 11	1		ns
			02		1		
$\overline{\text{DAV}}$ ↑ to DAC ↓ delay output 3-wire handshake 2/	TdDAVOr(DAC)	Reference number 23. 3/ 4/ 12/	01	9, 10, 11	0		ns
			02		0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{CC} = 5.0 V ±10%, -55ºC ≤ T_C ≤ +125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
PCLK cycle time 15/	TcPC	Reference number 1. 3/ 4/ 16/	01	9, 10, 11	165	4000	ns
			02		250	4000	
PCLK high width 2/	TwPCh	Reference number 2. 3/ 4/ 16/	01	9, 10, 11	70	2000	ns
			02		105	2000	
PCLK low width	TwPCl	Reference number 3. 3/ 4/ 16/	01	9, 10, 11	70	2000	ns
			02		105	2000	
PCLK fall time	TfPC	Reference number 4. 3/ 4/ 16/	01	9, 10, 11		10	ns
			02			20 2/	
PCLK rise time 2/	TrPC	Reference number 5. 3/ 4/ 16/	01	9, 10, 11		15	ns
			02			20	
Counter input cycle time 2/	TcCl	Reference number 6. 3/ 4/ 16/	01	9, 10, 11	330		ns
			02		500		
Counter input high width 2/	TClh	Reference number 7. 3/ 4/ 16/	01	9, 10, 11	150		ns
			02		230		
Counter input low width 2/	TwCll	Reference number 8. 3/ 4/ 16/	01	9, 10, 11	150		ns
			02		230		
Counter input fall time 2/	TfCl	Reference number 9. 3/ 4/ 16/	01	9, 10, 11		15	ns
			02			20	
Counter input rise time 2/	TrCl	Reference number 10. 3/ 4/ 16/	01	9, 10, 11		15	ns
			02			20	
Trigger input to PCLK ↓ setup time (timer mode) 2/ 17/	TsTI(PC)	Reference number 11. 3/ 4/ 16/	01	9, 10, 11			ns
			02		150		
Trigger input to counter input ↓ setup time (counter mode) 2/ 17/	TsTI(Cl)	Reference number 12. 3/ 4/ 16/	01	9, 10, 11			ns
			02		150		
Trigger input pulse width (high or low) 2/	TwTI	Reference number 13. 3/ 4/ 16/	01	9, 10, 11			ns
			02		200		
Gate input to PCLK ↓ setup time (timer mode) 2/ 17/	TsGI(PC)	Reference number 14. 3/ 4/ 16/	01	9, 10, 11			ns
			02		100		
Gate input to counter input ↓ setup time (counter mode) 2/ 17/	TsGI(Cl)	Reference number 15. 3/ 4/ 16/	01	9, 10, 11			ns
			02		100		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{CC} = 5.0 V ±10%, -55ºC ≤ T_C ≤ +125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Gate input to PCLK ↓ hold time (timer mode) 2/ 17/	ThGI(PC)	Reference number 16. 3/ 4/ 16/	01	9, 10, 11			ns
			02		100		
Gate input to counter input ↓ hold time (counter mode) 2/ 17/	ThGI(CI)	Reference number 17. 3/ 4/ 16/	01	9, 10, 11			ns
			02		100		
PCLK to counter output delay (timer mode) 2/	TdPC(CO)	Reference number 18. 3/ 4/ 16/	01	9, 10, 11			ns
			02			475	
Counter input to counter output delay (counter mode) 2/	TdCI(CO)	Reference number 19. 3/ 4/ 16/	01	9, 10, 11			ns
			02			475	
$\overline{DS}$ ↓ to REQ ↓ delay 2/	TdDS(REQ)	Reference number 1. 3/ 4/ 18/	01	9, 10, 11			ns
			02			500	
$\overline{DS}$ ↓ to $\overline{WAIT}$ ↓ delay 2/	TdDS(WAIT)	Reference number 2. 3/ 4/ 18/	01	9, 10, 11			ns
			02			500	
PCLK ↓ to REQ ↑ delay 2/	TdPC(REQ)	Reference number 3. 3/ 4/ 18/	01	9, 10, 11			ns
			02			300	
PCLK ↓ to $\overline{WAIT}$ ↑ delay 2/	TdPC(WAIT)	Reference number 4. 3/ 4/ 18/	01	9, 10, 11			ns
			02			300	
$\overline{ACKIN}$ ↓ to REQ ↑ delay 2/ 19/ 20/	TdACK(REQ)	Reference number 5. 3/ 4/ 18/	01	9, 10, 11			ns
			02			3 + 2 +1000	
$\overline{ACKIN}$ ↓ to $\overline{WAIT}$ ↑ delay 2/ 21/	TdACK(WAIT)	Reference number 6. 3/ 4/ 18/	01	9, 10, 11			ns
			02			10 + 600	
Delay from $\overline{DS}$ ↑ to $\overline{AS}$ ↓ for no reset 2/	TdDSQ(AS)	Reference number 1. 3/ 4/ 22/	01	9, 10, 11	15		ns
			02		40		
Delay from $\overline{AS}$ ↑ to $\overline{DS}$ ↓ for no reset 2/	TdASQ(DS)	Reference number 2. 3/ 4/ 22/	01	9, 10, 11	30		ns
			02		50		
Minimum width of $\overline{AS}$ and $\overline{DS}$ both low for reset 23/	TdDSQ(AS)	Reference number 3. 3/ 4/ 22/	01	9, 10, 11	170		ns
			02		250		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions V_{CC} = 5.0 V ±10%, -55ºC ≤ T_C ≤ +125°C unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Any input rise time 2/	TrI	Reference number 1. 3/ 4/ 24/	01	9, 10, 11		100	ns
			02			100	
Any input fall time 2/	TfI	Reference number 2. 3/ 4/ 24/	01	9, 10, 11		100	ns
			02			100	
1's catcher high width 2/ 25/	Tw1's	Reference number 3. 3/ 4/ 24/	01	9, 10, 11	170		ns
			02		250		
Pattern match input valid (bit port) 2/	TwPM	Reference number 4. 3/ 4/ 24/	01	9, 10, 11	500		ns
			02		750		
Data latched on pattern match setup time (bit port) 2/	TsPMD	Reference number 5. 3/ 4/ 24/	01	9, 10, 11	0		ns
			02		0		
Data latched on pattern match hold time (bit port) 2/	ThPMD	Reference number 6. 3/ 4/ 24/	01	9, 10, 11	650		ns
			02		1000		
$I/\overline{O}$ ↑ to RFD/$\overline{DAV}$ high delay 2/	TdIOr(DAV)	Reference number 1. 3/ 4/ 26/	01	9, 10, 11		500	ns
			02			500	
$I/\overline{O}$ ↑ to data float delay 2/	TdIOr(DRZ)	Reference number 2. 3/ 4/ 26/	01	9, 10, 11		500	ns
			02			500	
$I/\overline{O}$ ↑ to $\overline{ACKIN}$ ↓ delay 27/	TdIOr(ACK)	Reference number 3. 3/ 4/ 26/	01	9, 10, 11			ns
			02				
$I/\overline{O}$ ↓ to RFD/$\overline{DAV}$ high delay 2/	TdIOf(RFD)	Reference number 4. 3/ 4/ 26/	01	9, 10, 11		500	ns
			02			500	
$I/\overline{O}$ ↓ to RFD/$\overline{DAV}$ ↓ delay 2/ 28/	TdIOf(DAV)	Reference number 5. 3/ 4/ 26/	01	9, 10, 11	3		ns
			02		3		
$I/\overline{O}$ ↓ to data bus driven 2/ 28/	TdDO(IO)	Reference number 6. 3/ 4/ 26/	01	9, 10, 11	2		ns
			02		2		

See footnotes on next sheet.

TABLE I. Electrical performance characteristics - Continued.

1/ Guaranteed by characterization/design.

2/ Guaranteed if not tested.

3/ The reference number refers to the parameter being measured on figures 3.

4/ C_L = 50 pF ±10% unless otherwise specified.

5/ See figure 3a.

6/ Parameter does not apply to Interrupt Acknowledge transactions.

7/ Float delay is measured to the time when the output has changed 0.5 V with minimum ac load and maximum dc load.

8/ This is the delay from $\overline{DS}$ ↑ of one CIO access to $\overline{DS}$ ↓ of another CIO access.

9/ Units equal to AS cycle + ns.

10/ The delay is from $\overline{DAV}$ ↓ for 3-wire input handshake. The delay is from DAC ↑ for 3-wire output handshake. One additional AS cycle is required for ports in the single buffered mode.

11/ The parameters for the devices in any particular daisy chain must meet the following constraint: The delay from $\overline{AS}$ ↑ to DS ↓ must be greater than the sum of TdAS(IEO) for the highest priority peripheral, TsIEI(DSA) for the lowest priority peripheral, and TdIEI(IEO) for each peripheral separating them in the chain.

12/ See figure 3b.

13/ This time can be extended through the use of the deskew timers.

14/ Units equal to AS cycle.

15/ PCLK is only used with the counter/timers (in timer mode), the deskew timers, and the REQUEST/$\overline{WAIT}$ logic. If these functions are not used, the PCLK input can be held low.

16/ See figure 3c.

17/ These parameters must be met to guarantee the trigger or gate is valid for the next counter/timer cycle.

18/ See figure 3d.

19/ The delay is from $\overline{DAV}$ ↓ for the 3-wire input handshake. The delay is from DAC ↑ for the 3-wire output handshake.

20/ Units equal to AS cycles + PCLK cycles + ns.

21/ Units equal to PCLK cycles + ns.

22/ See figure 3e.

23/ Internal circuitry allows for the reset provided by the Z8 ($\overline{DS}$ held low while $\overline{AS}$ pulses) to be sufficient.

24/ See figure 3f.

25/ If the input is programmed inverting, a low-going pulse of the same width will be detected.

26/ See figure 3g.

27/ Minimum delay is four AS cycles or one AS cycle after the corresponding IP is cleared, whichever is longer.

28/ Units equal to AS cycles.

Device types:	01 and 02		
Case outline:	Q		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AD_4	21	PC_2
2	AD_5	22	PC_3
3	AD_6	23	+5 V
4	AD_7	24	$\overline{INT}$
5	$\overline{DS}$	25	$\overline{INTACK}$
6	$R/\overline{W}$	26	PA_7
7	GND	27	PA_6
8	PB_0	28	PA_5
9	PB_1	29	PA_4
10	PB_2	30	PA_3
11	PB_3	31	PA_2
12	PB_4	32	PA_1
13	PB_5	33	PA_0
14	PB_6	34	$\overline{AS}$
15	PB_7	35	CS_1
16	PCLK	36	$\overline{CS_0}$
17	IEI	37	AD_0
18	IEO	38	AD_1
19	PC_4	39	AD_2
20	PC_1	40	AD_3

FIGURE 1. Terminal connections.

Device types:	01 and 02		
Case outline:	Y		
Terminal number	Terminal name	Terminal number	Terminal name
1	AD_4	23	PC_2
2	AD_5	24	PC_3
3	AD_6	25	+5 V
4	AD_7	26	$\overline{INT}$
5	$\overline{DS}$	27	$\overline{INTACK}$
6	NC	28	NC
7	$R/\overline{W}$	29	NC
8	NC	30	PA_7
9	GND	31	PA_6
10	PB_0	32	PA_5
11	PB_1	33	PA_4
12	PB_2	34	PA_3
13	PB_3	35	PA_2
14	PB_4	36	PA_1
15	PB_5	37	PA_0
16	PB_6	38	$\overline{AS}$
17	PB_7	39	$\overline{CS}$
18	PCLK	40	$\overline{CS_0}$
19	IEI	41	AD_0
20	IEO	42	AD_1
21	PC_0	43	AD_2
22	PC_1	44	AD_3

NC = No connection

FIGURE 1. Terminal connections - Continued.

DEVICE TYPES 01 AND 02

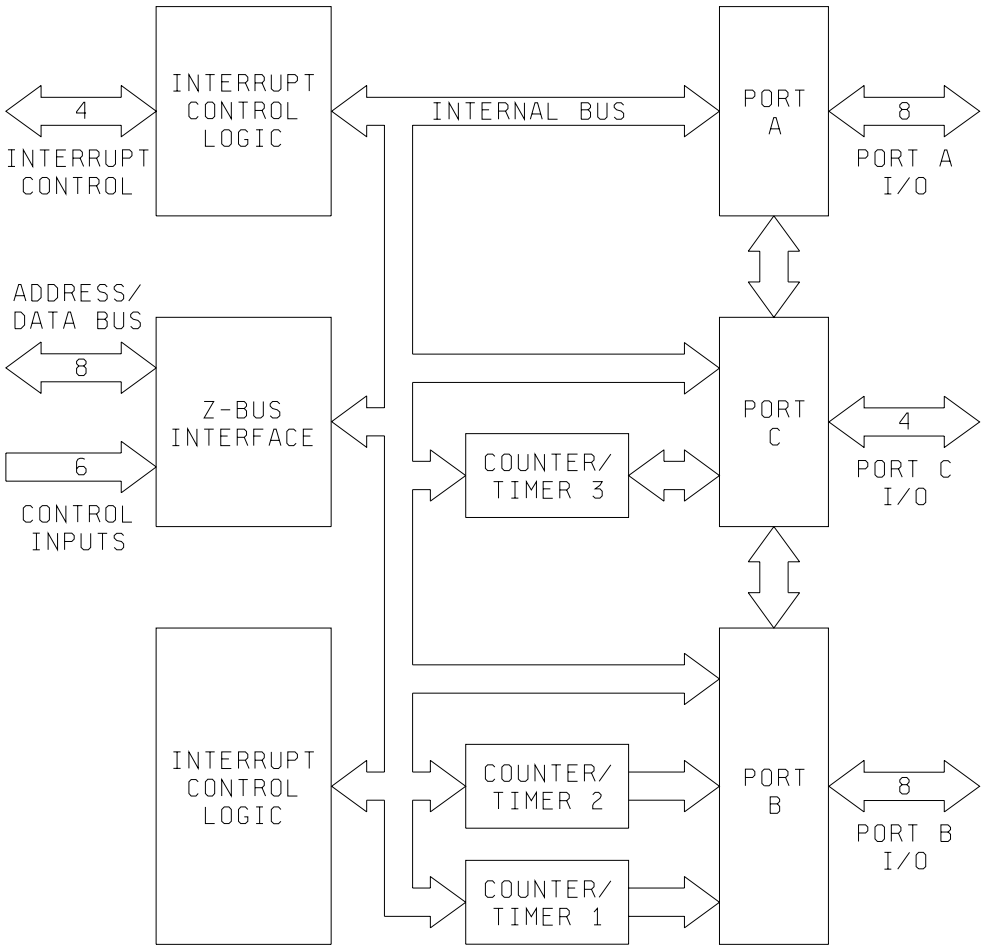


FIGURE 2. Functional block diagram.

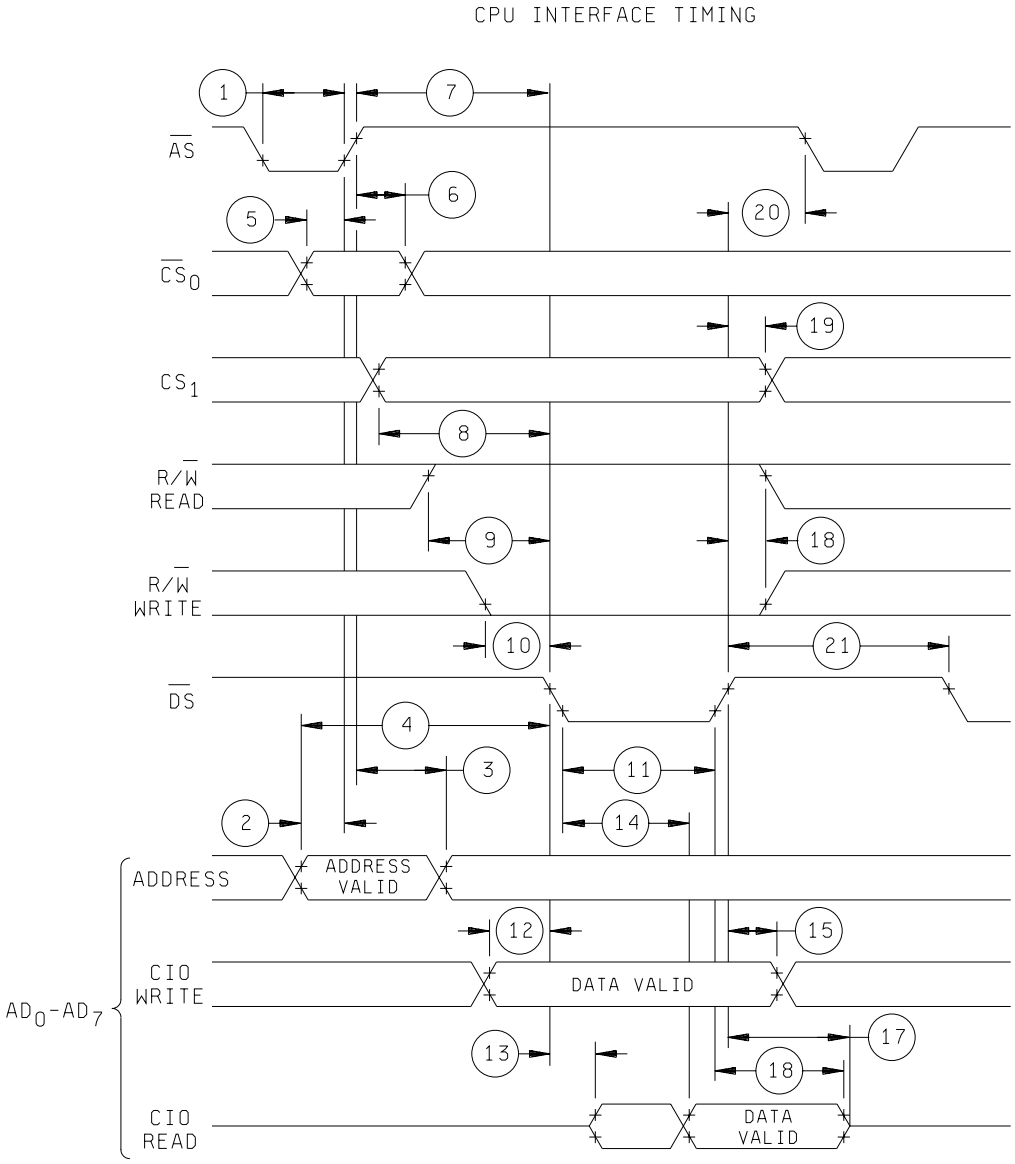


FIGURE 3a. Timing waveforms.

INTERRUPT TIMING

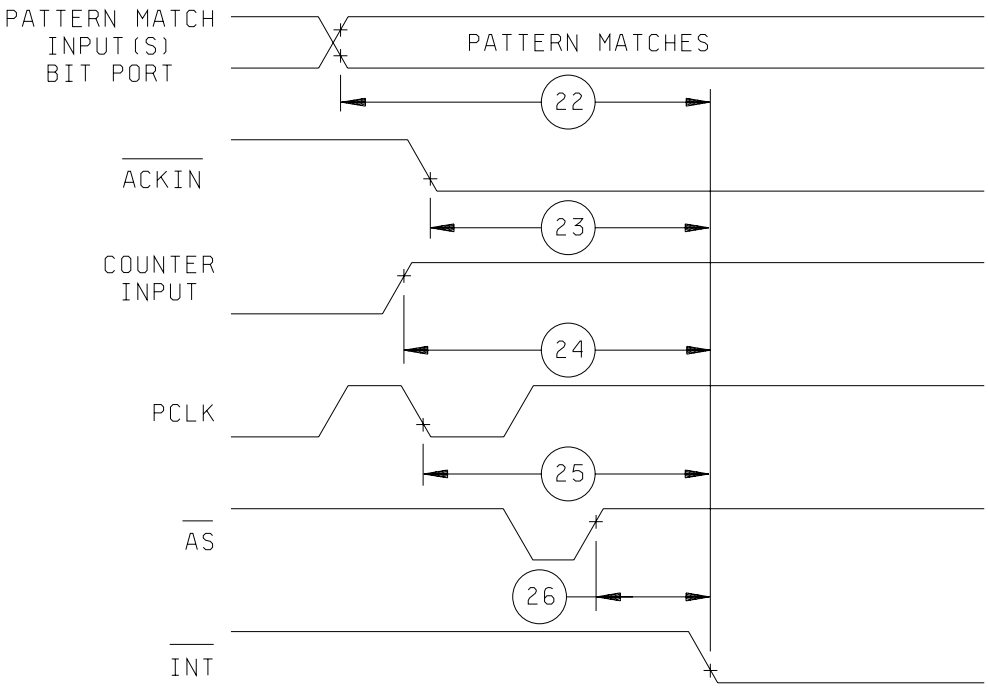


FIGURE 3a. Timing waveforms - Continued.

INTERRUPT ACKNOWLEDGE TIMING

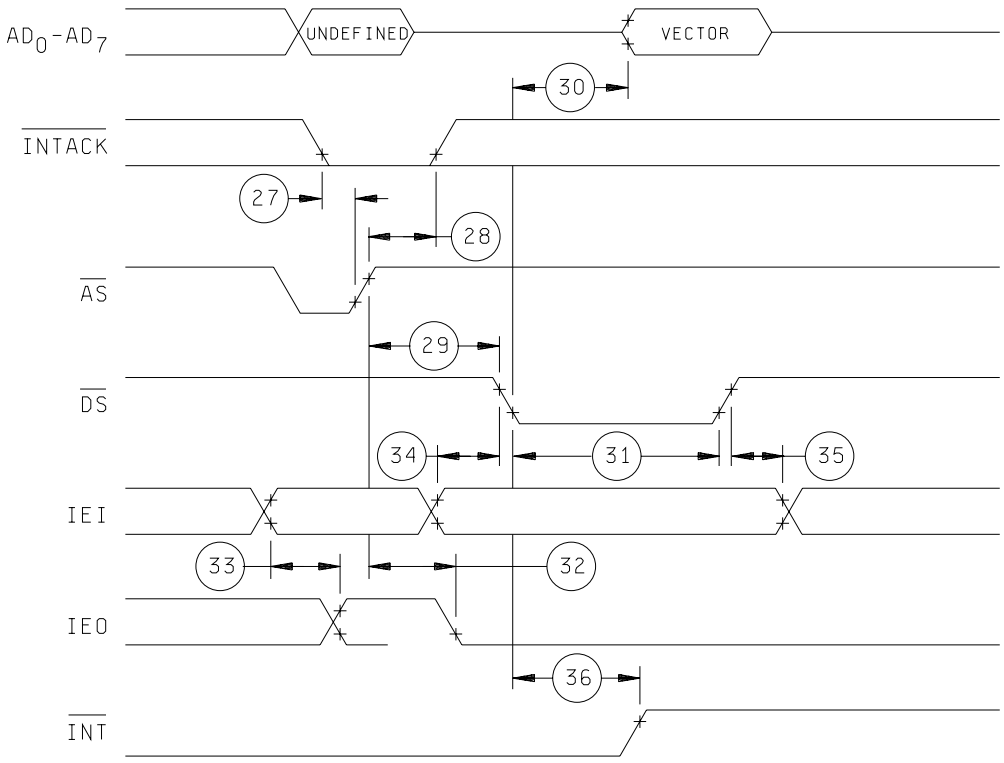


FIGURE 3a. Timing waveforms - Continued.

STROBED HANDSHAKE

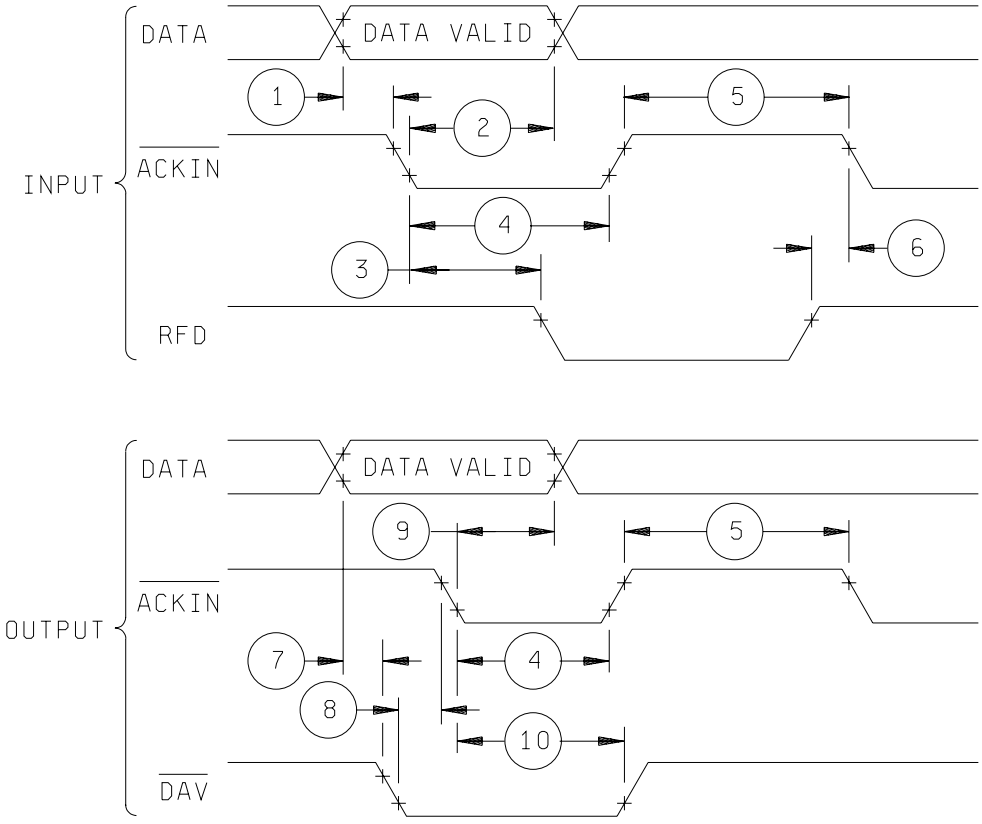


FIGURE 3b. Timing waveforms - Continued.

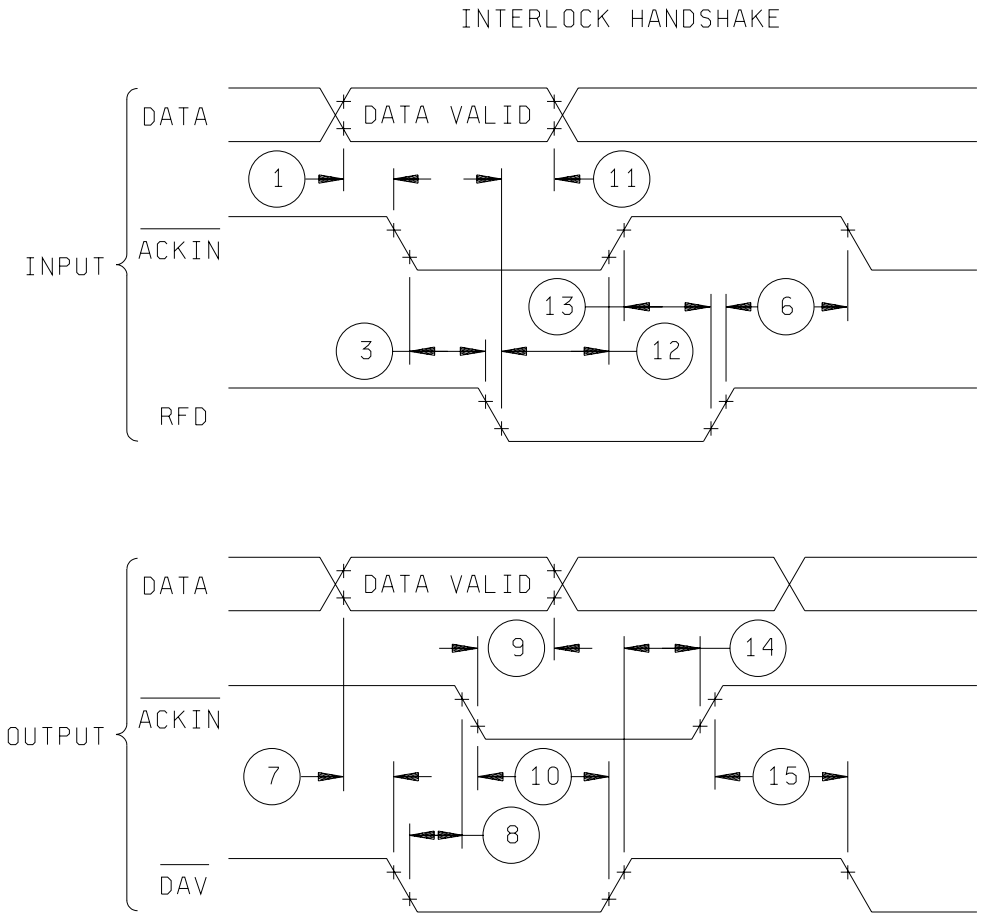


FIGURE 3b. Timing waveforms - Continued.

3-WIRE HANDSHAKE

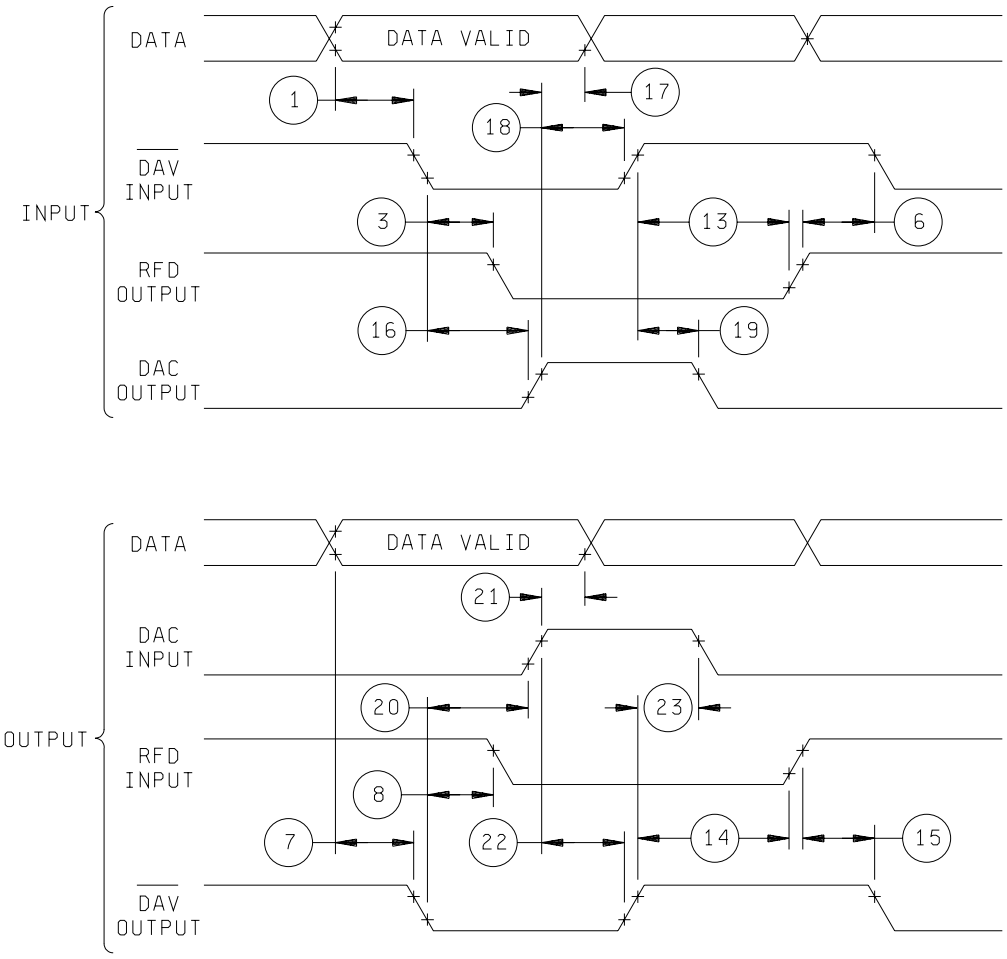


FIGURE 3b. Timing waveforms - Continued.

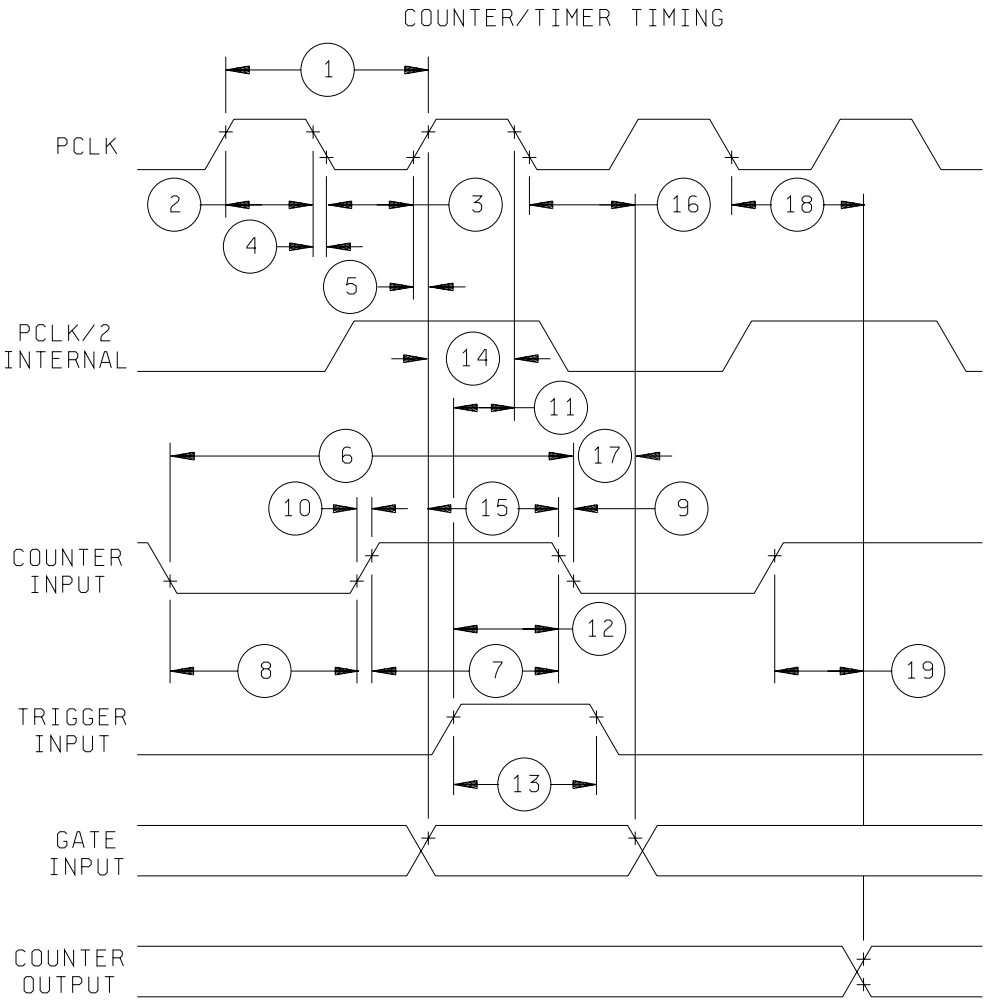


FIGURE 3c. Timing waveforms - Continued.

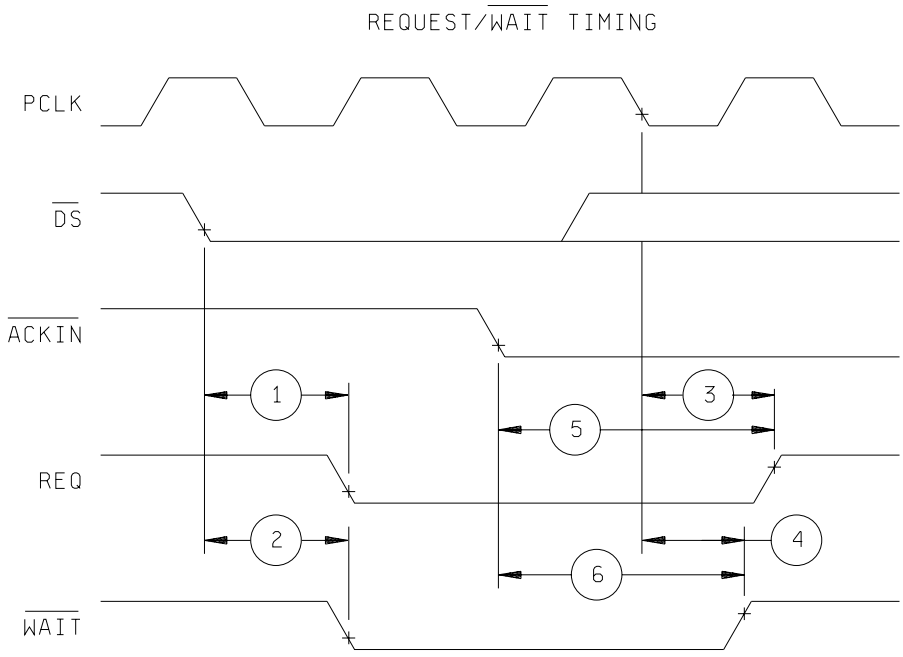


FIGURE 3d. Timing waveforms - Continued.

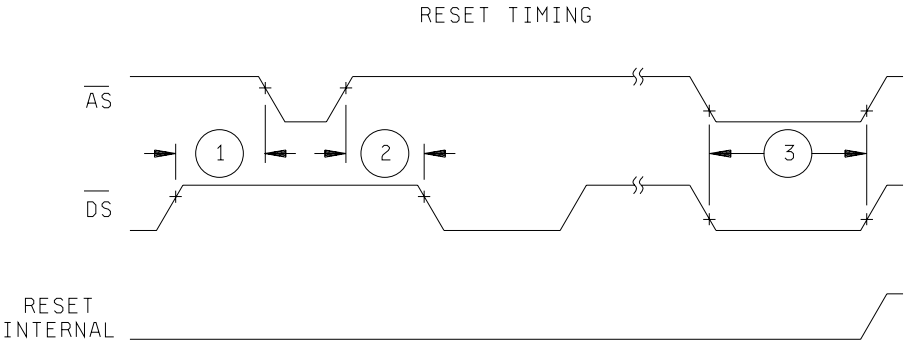


FIGURE 3e. Timing waveforms - Continued.

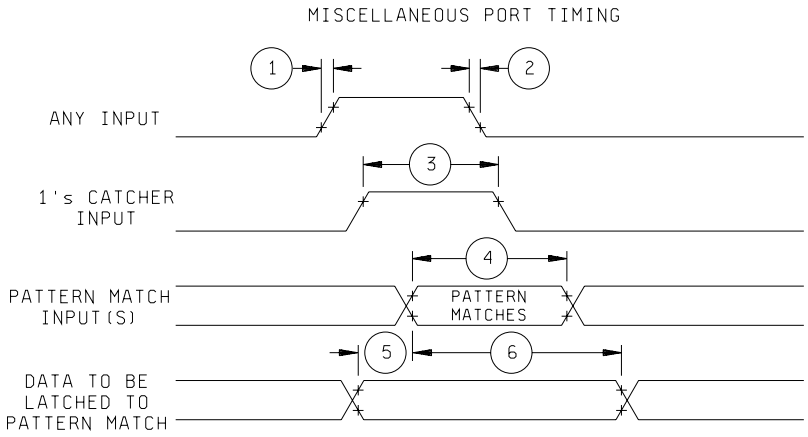


FIGURE 3f. Timing waveforms - Continued.

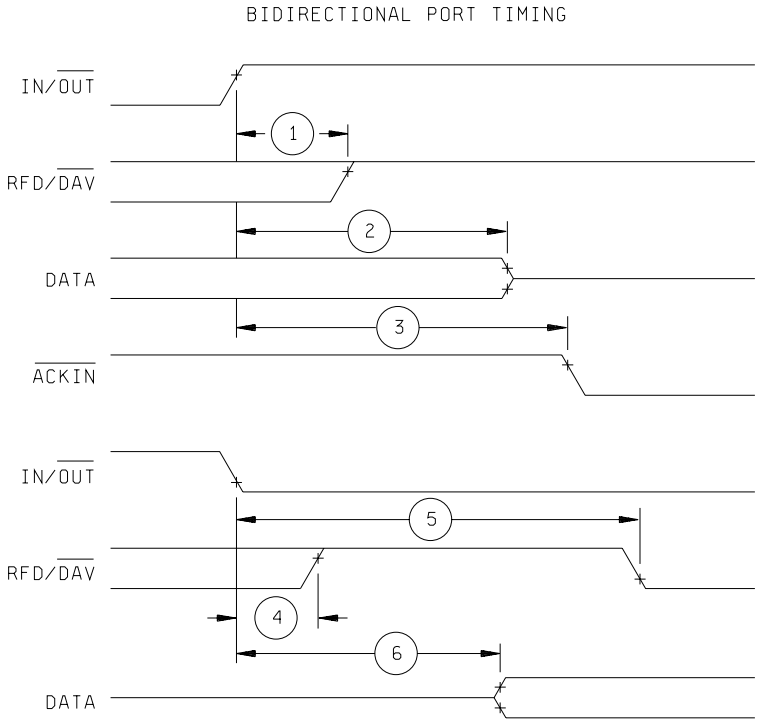


FIGURE 3g. Timing waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125ºC, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 functional test shall include verification of the instruction set.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125ºC, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Terms and definitions. The terms and definitions for this device shall be as follows:

AD_0-AD_7 Z-Bus address/data lines (bidirectional/3-state). These multiplexed address/data lines are used for transfers between the CPU and the device specifications.

$\overline{AS}$* Address strobe (input, active low). Addresses, $\overline{INTACK}$, and $\overline{CS_0}$ are sampled while $\overline{AS}$ is low.

$\overline{CS_0}$, CS_1 Chip select 0 (input, active low) and chip select 1 (input, active high). $\overline{CS_0}$ and CS_1 must be low and high, respectively, in order to select a device. $\overline{CS_0}$ is latched by $\overline{AS}$.

$\overline{DS}$* Data strobe (input, active low). $\overline{DS}$ provides timing for the transfer of data into or out of the device specified herein.

IEI Interrupt enable in (input, active high). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A high IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO Interrupt enable out (output, active high). IEO is high only if IEI is high and the CPU is not servicing an interrupt from the requesting device or is not requesting an interrupt (interrupt acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

$\overline{INT}$ Interrupt request (output, open-drain, active low). This signal is pulled low when the device requests an interrupt.

$\overline{INTACK}$ Interrupt acknowledge (input, active low). This signal indicates to the device that an interrupt acknowledge cycle is in progress. $\overline{INTACK}$ is sampled while $\overline{AS}$ is low.

PA_0-PA_7 Port A I/O lines (bidirectional, 3-state, or open drain). These eight I/O lines transfer information between the device's port A and external devices.

PB_0-PB_7 Port B I/O lines (bidirectional, 3-state, or open drain). These eight I/O lines transfer information between the device's port B and external devices. May also be used to provide external access to counter/timers 1 and 2.

PC_0-PC_3 Port C I/O lines (bidirectional, 3-state, or open drain). These four I/O lines are used to provide handshake, $\overline{WAIT}$, and REQUEST lines for ports A and B, or to provide external access to counter/timer 3 or access to the device's port C.

PCLK Peripheral clock (input, TTL-compatible). This is a peripheral clock that may be, but is not necessarily, the CPU clock. It is used with the timers and the REQUEST/$\overline{WAIT}$ logic.

R/$\overline{W}$ Read/write (input). R/$\overline{W}$ indicates that the CPU is reading from (high) and writing to (low) the device..

* When $\overline{AS}$ and $\overline{DS}$ are detected low at the same time (normally an illegal condition), the device is reset.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-04-06

Approved sources of supply for SMD 85517 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8551701QA	0C7V7	Z8036ACMB
8551701YA	0C7V7	Z8036ALMB
8551702QA	0C7V7	Z8036CMB
8551702YA	0C7V7	Z8036LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0C7V7	QP semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

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