REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Outline letter, Y, case outline changed to F-11 for standardization. Convert to military drawing format. Editorial changes throughout.	88-01-19	Michael A. Frye
B	Make change to table I, table II, 1.2. 2, 3. 3, and 4.3. Add figure 5. Editorial changes throughout. Make change to figure 4.	89-04-04	Michael A. Frye
C	Updated boilerplate. Added device type 02. Removed CAGE 34335 from drawing and added CAGE 0DKS7. - glg	99-10-19	Raymond Monnin
D	Added provisions for the addition of QD certified parts to drawing. Added CAGE OC7V7 as supplier. - glg	00-02-03	Raymond Monnin
E	Corrected marking paragraph 3.5, updated boilerplate paragraphs. ksr	05-04-01	Raymond Monnin
F	Updated body of drawing to reflect current requirements. - glg	11-03-08	Charles Saffle

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

CURRENT CAGE CODE 67268

REV																			
SHEET																			
REV	F	F																	
SHEET	15	16																	

REV STATUS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
31 MARCH 1986

REVISION LEVEL
F

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE
FOR USE BY ALL DEPARTMENTS
AND AGENCIES OF THE
DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUITS, MEMORY, DIGITAL, BIPOLAR, 16-WORD BY 4-BIT, 2-PORT, RAM, MONOLITHIC SILICON

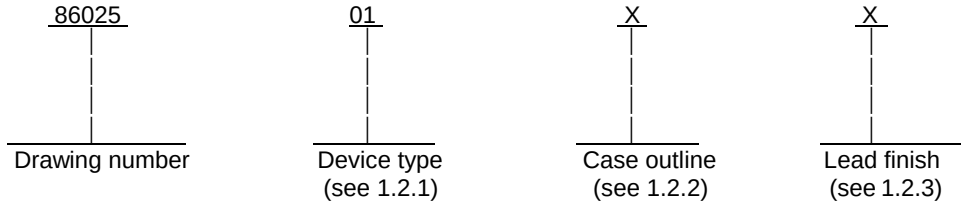
SIZE	CAGE CODE	
A	**14933**	**86025**

SHEET 1 OF 16

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit
01	29705A	16-word by 4-bit, 2-port RAM, 30 ns
02	29705A-35	16-word by 4-bit, 2-port RAM, 35 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	dual-in-line package
Y	GDFP2-F28	28	flat package
3	CQCC1-N28	28	square chip carrier package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Storage temperature	-65°C to +150°C
Supply voltage to ground potential	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs for high output stage	-0.5 V dc to +V_{CC} maximum
DC input voltage	-0.5 V dc to +5.5 V dc
DC output current, into outputs	30 mA
DC input current	-30 mA to +5.0 mA
Maximum power dissipation (P_D) 1/	1.155 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH})	+2.0 V dc
Maximum low level input voltage (V_{IL})	+0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device types	Group A subgroups	Limits		Unit
						Min	Max	
Output high voltage	V_{OH}	V_{CC} = minimum, I_{OH} = -2.0 mA $V_{IN} = V_{IH}$ or V_{IL}		All	1, 2, 3	2.4		V
Output low voltage	V_{OL}	V_{CC} = minimum, I_{OL} = 16 mA $V_{IN} = V_{IH}$ or V_{IL}		All	1, 2, 3		0.5	V
Input high level	V_{IH}	Guaranteed input logical high voltage for all inputs		All	1, 2, 3	2		V
Input low level	V_{IL}	Guaranteed input logical low voltage for all inputs		All	1, 2, 3		0.8	V
Input clamp voltage	V_I	V_{CC} = minimum, I_{IN} = - 18 mA		All	1, 2, 3		-1.5	V
Input low current	I_{IL}	V_{CC} = maximum, V_{IN} = 0.5 V		All	1, 2, 3		-0.36	mA
Input high current	I_{IH}	V_{CC} = maximum, V_{IN} = 2.7 V		All	1, 2, 3		20	µA
	I_I	V_{CC} = maximum, V_{IN} = 5.5 V		All	1, 2, 3		0.1	mA
Off state (high impedance) output current	I_O	V_{CC} = maximum $V_{IN} = V_{IH}$ or V_{IL}	V_O = 2.4 V	All	1, 2, 3		20	µA
			V_O = 0.5 V				-20	
Output short circuit current 1/	I_{OS}	V_{CC} maximum + .5 V, V_O = 0.5 V		All	1, 2, 3	-30	-85	mA
Power supply current	I_{CC}	V_{CC} = maximum (Worst case I_{CC} is at minimum temperature) 2/	T_C = -55°C to +125°C	All	1, 2, 3		210	mA
			T_C = +125°C				150	
Functional tests		See 4.3.1c		All	7,8A,8B			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Access time from: A address stable or B address stable to: YA stable or YB stable	t_{AA}	See figure 4 and 5 C_L = 50 pF, LE = high	01	9, 10, 11		30	ns
			02			35	
Turn-on time from: $\overline{OE-A}$ or $\overline{OE-B}$ low to: YA or YB stable	t_{ON}	See figure 4 and 5 C_L = 50 pF	All	9, 10, 11		20	ns
Turn-off time from: $\overline{OE-A}$ or $\overline{OE-B}$ high to: YA or YB off	t_{OFF}	See figure 4 and 5 C_L = 5 pF 3/	All	9, 10, 11		20	ns
Reset time from: $\overline{A-LO}$ low to: YA low	t_{RES}	See figure 4 and 5 C_L = 50 pF	All	9, 10, 11		20	ns
Latch enable time from: LE high to: YA and YB stable	t_{EN}	See figure 4 and 5 C_L = 50 pF	01	9, 10, 11		22	ns
			02			30	
Transparency 1 from: $\overline{WE}_1$ and $\overline{WE}_2$ low to: YA or YB	t_{PD1}	See figure 4 and 5 C_L = 50 pF, LE = high	01	9, 10, 11		35	ns
			02			40	
Transparency 2 from: D to: YA or YB	t_{PD2}	See figure 4 and 5 C_L = 50 pF, LE = high	01	9, 10, 11		35	ns
			02			40	
Data setup time from: D stable to: Either $\overline{WE}$ high	t_{S1}	See figure 4 and 5 C_L = 50 pF	All	9, 10, 11	15		ns
Data hold time from: Either $\overline{WE}$ high to: D changing	t_{H1}	See figure 4 and 5 C_L = 50 pF	All	9, 10, 11	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Address setup time from: B stable to: Both $\overline{WE}$ low	t_{S2}	See figure 4 and 5 $C_L = 50$ pF	All	9, 10, 11	8		ns
Address hold time from: Either $\overline{WE}$ high to: B changing	t_{H2}	See figure 4 and 5 $C_L = 50$ pF	All	9, 10, 11	0		ns
Latch close before write begin 1 from: LE low to: $\overline{WE}_1$ low	t_{PD3}	$C_L = 50$ pF, $\overline{WE}_2$ low See figure 4 and 5	All	9, 10, 11	0		ns
Latch close before write begin 2 from: LE low to: $\overline{WE}_2$ low	t_{PD4}	$C_L = 50$ pF, $\overline{WE}_1$ low See figure 4 and 5	All	9, 10, 11	0		ns
Address set up before latch closes from: A or B stable to : LE low	t_{S3}	See figure 4 and 5 $C_L = 50$ pF	All	9, 10, 11	15		ns
Write pulse width 1 Input: $\overline{WE}$, Pulse: High-low-high	t_{PW1}	$C_L = 50$ pF, $\overline{WE}_2$ low See figure 4 and 5	All	9, 10, 11	15		ns
Write pulse width 2 Input: $\overline{WE}_2$, Pulse: High-low-high	t_{PW2}	$C_L = 50$ pF, $\overline{WE}_1$ low See figure 4 and 5	All	9, 10, 11	15		ns
A latch reset pulse Input: $\overline{A-LO}$, Pulse: High-low-high	t_{PW3}	See figure 4 and 5 $C_L = 50$ pF	All	9, 10, 11	15		ns
Latch data capture Input: LE Pulse: Low-high-low	t_{PW4}	See figure 4 and 5 $C_L = 50$ pF	All	9, 10, 11	18		ns

1/ Not more than one output should be shorted at a time. Duration of the sort circuit test should not exceed 1 second.

2/ All inputs grounded except $\overline{OE-A}$ and $\overline{OE-B}$ = 2.4 V

3/ Measured from 1.5V at the input to 0.5V change in the output level.

Device type	All
Case outline	X, Y, 3
Terminal number	Terminal symbol
1	D_1
2	D_0
3	$\overline{WE}_1$
4	B_0
5	B_1
6	B_2
7	B_3
8	$\overline{A-LO}$
9	LE
10	YB_0
11	YA_0
12	YB_1
13	YA_1
14	GND
15	YB_2
16	YA_2
17	YB_3
18	YA_3
19	$\overline{OE-B}$
20	$\overline{OE-A}$
21	A_3
22	A_2
23	A_1
24	A_0
25	$\overline{WE}_2$
26	D_3
27	D_2
28	V_{CC}

FIGURE 1. Terminal connections.

Write control

$\overline{WE}_1$	$\overline{WE}_2$	Function	RAM outputs at latch inputs	
			A-port	B-port
L	L	Write D into B	A data (A ≠ B)	Input data
L	L	Write D into B	(A = B) Input data	Input data
X	H	No write	A data	B data
H	X	No write	A data	B data

H = High L = Low X = Don't care

YA READ

Inputs			YA output	Function
$\overline{OE-A}$	$\overline{A-LO}$	LE		
H	X	X	Z	High impedance
L	L	X	L	Force YA low
L	H	H	A-port RAM data	Latches transparent
L	H	L	NC	Latches retain data

H = High
L = Low
X = Don't care
Z = High impedance
NC = No Change

YB READ

Inputs		YB output	Function
$\overline{OE-B}$	LE		
H	X	Z	High impedance
L	H	B-port RAM data	Latches transparent
L	L	NC	Latches retain data

H = High
L = Low
X = Don't care
Z = High impedance
NC = No Change

FIGURE 2. Truth tables.

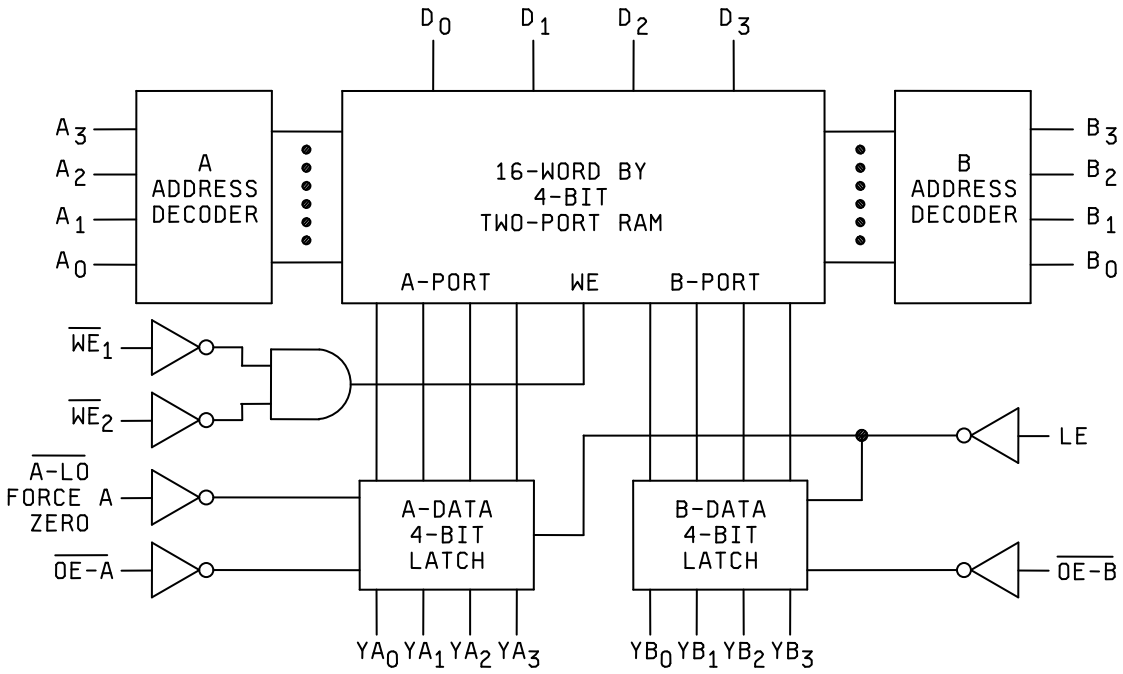
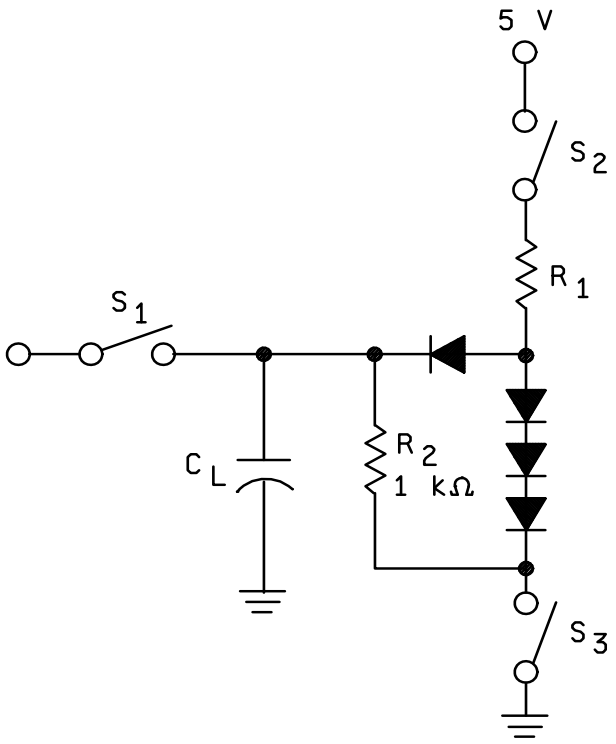


FIGURE 3. Logic diagram.

THREE-STATE OUTPUT



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

NOTES:

1. C_L = 50 pF includes scope probe, wiring and stray capacitances without device in text fixture.
2. S_1, S_2, and S_3 are closed during function tests and all ac tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{en} high test.
   S_1 and S_2 are closed while S_3 is open for t_{en} low test.
4. C_L = 5 pF for output disable test (see table I, t_{OFF}).

Pin label	Test circuit	R1	R2
Y_{A0} -Y_{A3}, Y_{B0} - Y_{B3}	A	230Ω	1 kΩ

FIGURE 4. Test output load configuration.

Write Timing

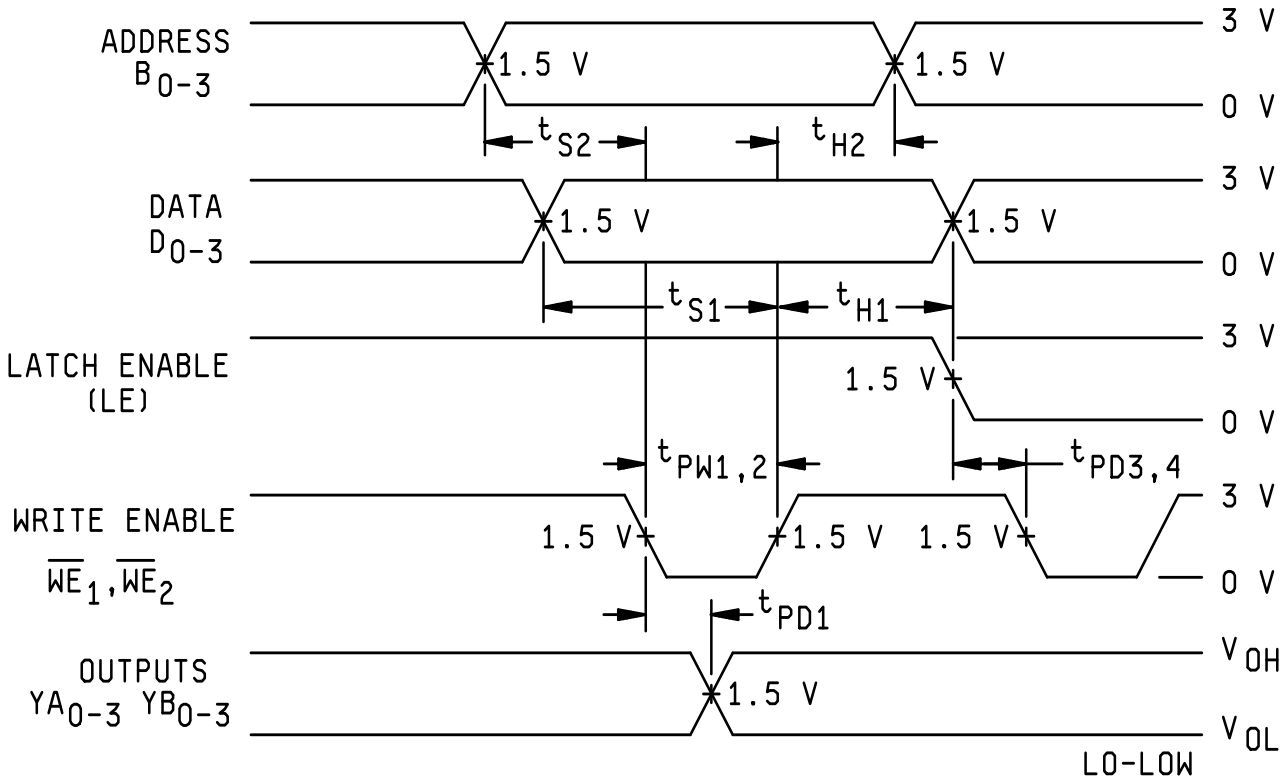


FIGURE 5. Timing waveforms.

Address access, reset timing

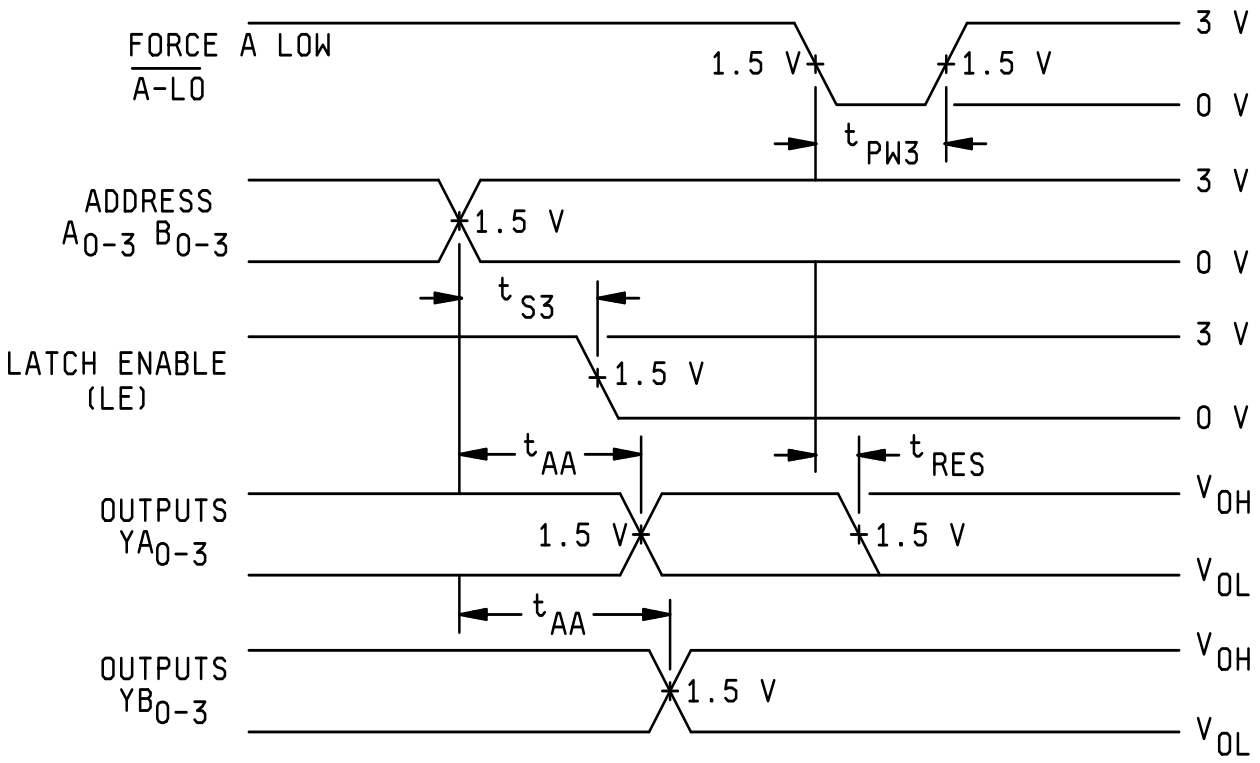
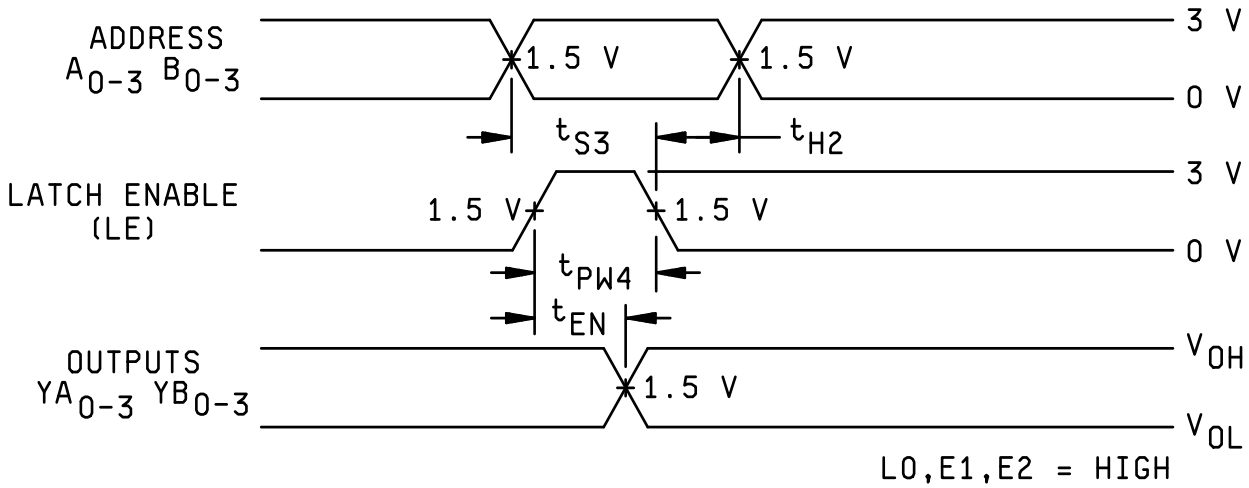


FIGURE 5. Timing waveforms - Continued.

Read timing



Data to output timing

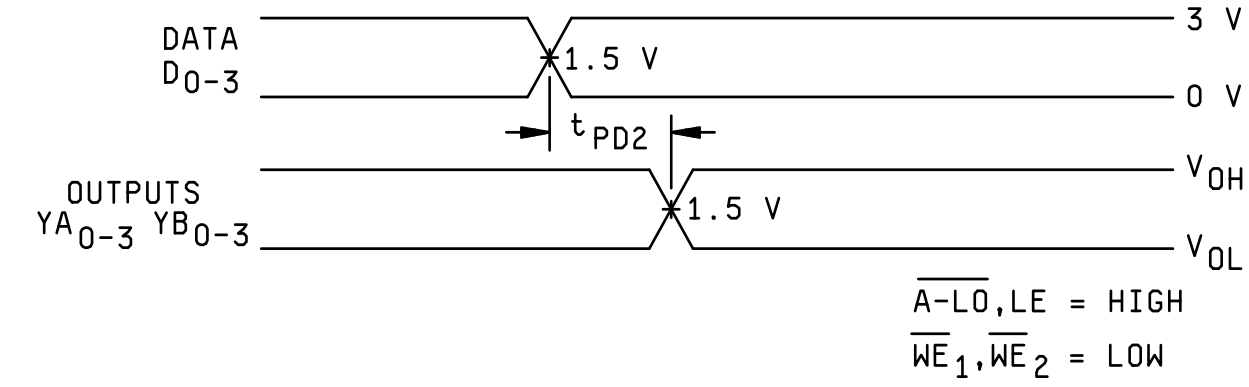


FIGURE 5. Timing waveforms - Continued.

Three-state enable,disable timing

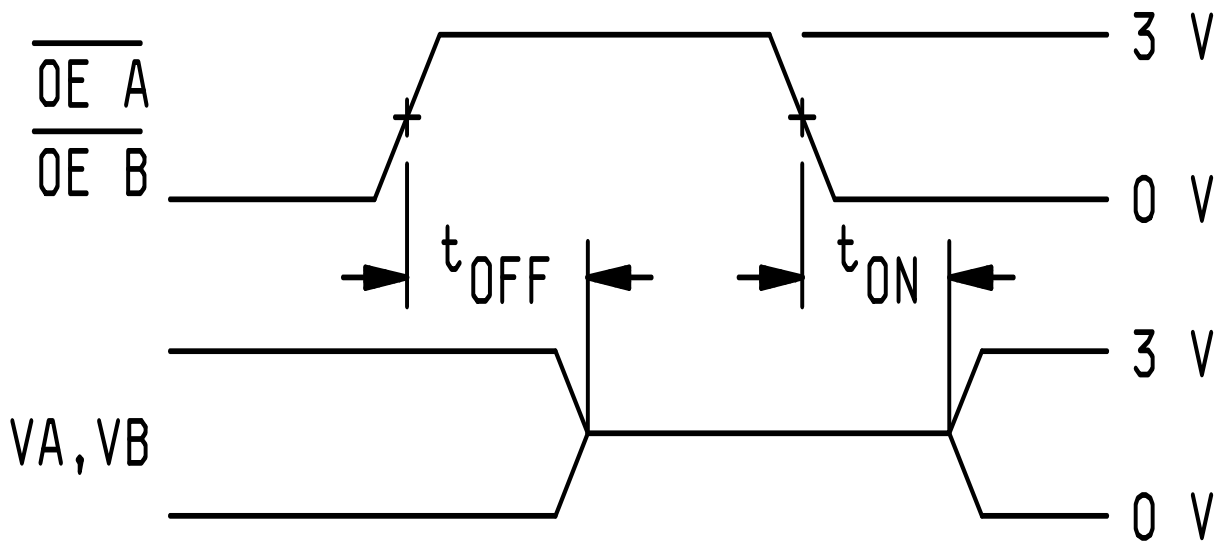


FIGURE 5. Timing waveforms - Continued.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 11-03-08

Approved sources of supply for SMD 86025 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
8602501XA	3/ 0C7V7 3V146	AM29705A/BXA 29705/XA 29705/BXA
8602501YA	3/ 0C7V7 3V146	AM29705A/BYA 29705/YA 29705/BYA
86025013A	3/ 3V146	AM29705A/B3A 29705/B3A
8602502XA	0DKS7	GEM10702QXA
8602502YA	0DKS7	GEM10702QYA
86025023A	0DKS7	GEM10702Q3A
8602502XC	0DKS7	GEM10702QXC
8602502YC	0DKS7	GEM10702QYC
86025023C	0DKS7	GEM10702Q3C

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source.

Vendor CAGE number	Vendor name and address
0DKS7	Sarnoff, David Research Center 201 Washington Road Princeton, NJ 08540-6449
0C7V7	E2V Aerospace and Defense, Inc. dba QP Semiconductor, Inc. 2945 Oakmead Village Court Santa Clara, CA 95051
3V146	Rochester Electronics Inc. 16 Malcolm Hoyt Drive Newburyport, MA 01950

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