INCH-POUND
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SUPERSEDING
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16 December 2003

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR, TTL, MONOSTABLE MULTIVIBRATORS, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

Inactive for new design as of September 07, 1995.

The requirement for acquiring the product herein shall consist of this specification sheet and MIL-PRF-38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, bipolar, TTL, monostable multivibrators microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.3).

1.2 Part or Identifying number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are as follows:

Device type	Circuit
01	Single monostable multivibrator, with Schmitt trigger input
02	Single retriggerable monostable multivibrator with clear
03	Dual retriggerable monostable multivibrator with clear
04	One shot multivibrator
05	Dual one shot multivibrator
06	Single monostable multivibrator, with Schmitt trigger input 1/

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outline. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
A 2/	GDFP5-F14 or CDFP6-F14	14	Flat pack
B 2/	GDFP4-14	14	Flat pack
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
E	GDIP1-T16 or CDIP2-T16	16	Dual in line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack

1/ For device type 06, the $t_{P(OUT)1}$ maximum test limit under TABLE I and TABLE III is 168 ns at -55°C, 125°C.
2/ Inactive package case outline. Acceptable only for use in equipment designed or redesigned on or before 29 November 1986.

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, 3990 East Broad St., Columbus, OH 43218-3990, or email bipolar@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -12 mA to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) per multivibrator:	
Device types 01 and 06	200 mW 3/
Device type 02	170 mW 3/
Device type 03	190 mW 3/
Device type 04	138 mW 3/
Device type 05	143 mW 3/
Lead temperature (soldering, 10 seconds)	+300°C.
Junction temperature (T_J)	+175°C 4/
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases A, B, C, D, E, and F	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	2.4 V dc
Maximum low-level input voltage (V_{IL})	0.4 V dc
Normalized fanout (each output) :	
Device types 01 and 06	10 maximum 5/
Device types 02 and 03 (low level logic)	10 maximum 5/
Device types 02 and 03 (high level logic)	20 maximum 5/
Device type 04 (low level logic)	6 maximum 5/
Device type 04 (high level logic)	12 maximum 5/
Device type 05 (low level logic)	8 maximum 5/
Device type 05 (high level logic)	16 maximum 5/
Input pulse rise/fall time, device types 01 and 06:	
Schmitt input (B)	1 V/s maximum
Positive gains threshold voltage (V_{T+})	2.0 V maximum
Negative gains threshold voltage (V_{T-})	0.8 V maximum
Logic inputs (A1, A2)	1 V/μs maximum
Input data setup time (t_{SETUP}):	
Device types 01 and 06	60 ns minimum
Device types 02, 03, 04, and 05	40 ns minimum
Input data hold time (t_{HOLD}):	
Device types 01 and 06	0 ns minimum
Device types 02, 03, 04, and 05	40 ns minimum
External timing resistance:	
Device types 01 and 06	30 kΩ maximum
Device types 02, 03, 04 and 05	5 kΩ minimum to 25 kΩ maximum
Case operating temperature range (T_C)	-55°C to +125°C

3/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with MIL-PRF-38535.
5/ The device shall fanout in both high and low levels to the specified number of data inputs of the same device type as that being tested.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein the text of this document shall takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.4).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Logic diagrams and terminal connections. The logic diagram and terminal connections shall be as specified on figure 1.

3.3.2 Truth tables. The truth tables shall be as specified on figure 2.

3.3.3 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.

3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Limits		Units
				Min	Max	
High-level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -0.4 mA	01, 06	2.4		V
		V_{CC} = 4.5 V, I_{OH} = -0.8 mA	02, 03 1/	2.4		
		V_{CC} = 4.5 V, I_{OH} = -0.72 mA	04	2.4		
		V_{CC} = 4.5 V, I_{OH} = -0.96 mA	05	2.4		
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 16 mA	01, 02, 1/ 03, 06		0.4	V
		V_{CC} = 4.5 V, I_{OL} = 10 mA	04		0.4	
		V_{CC} = 4.5 V, I_{OL} = 10 mA	05		0.4	
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -12 mA, T_C = +25°C	All		-1.5	V
Low-level input current at A1 or A2	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	01, 06	-0.7	-1.6	mA
Low-level input current at B	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	01, 06	-1.4	-3.2	mA
Low level input current at data inputs	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	02, 03	-0.7	-1.6	mA
Low level input current at clear input	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	02, 03	-1.4	-3.2	mA
Low level input current at data inputs	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	04	-0.7	-1.6	mA
Low level input current at data and clear inputs	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0.4 V	05	-0.7	-1.6	mA
High level input current at A_1 or A_2	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	01, 06		40	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V			100	
High level input current at B	I_{IH3}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	01, 06		80	µA
	I_{IH4}	V_{CC} = 5.5 V, V_{IN} = 5.5 V			200	
High level input current at data input	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	02, 03		40	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V			100	
High level input current at clear input	I_{IH3}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	02, 03		80	µA
	I_{IH4}	V_{CC} = 5.5 V, V_{IN} = 5.5 V			200	
High level input current at data inputs	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	04		40	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V			100	
High level input current at data and clear inputs	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.4 V	05		40	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V			100	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Limits		Units
				Min	Max	
Short circuit output current	I_{OS}	V_{CC} = 5.5 V, V_{IN} = 0 V 1/ 2/	01, 06	-20	-55	mA
			02, 03	-10	-40	
			04	-10	-40	
			05	-10	-40	
Supply current (quiescent)	I_{CC1}	V_{CC} = 5.5 V 3/	01, 06		25	mA
			02		28	
			03		66	
			04		25	
			05		52	
Supply current (triggered)	I_{CC2}	V_{CC} = 5.5 V 4/	01, 06		40	mA
			02		28	
			03		66	
Propagation delay time to high level (B input to Q output)	t_{PLH1}	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = 80 pF ±10%, R_L = 390 Ω ±5%, figure 4 (device type 01)	01, 06	15	75	ns
Propagation delay time to low level (B input to $\overline{Q}$ output)	t_{PHL1}		01, 06	20	87	ns
Propagation delay time to high level (A_1 or A_2 inputs to Q output)	t_{PLH2}		01, 06	25	93	ns
Propagation delay time to high level (A_1 or A_2 inputs to $\overline{Q}$ output)	t_{PHL2}		01, 06	30	106	ns
Pulse width obtained with internal timing resistor	$t_{P(OUT)1}$	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = 80 pF ±10%, R_L = 390 Ω ±5%, R_X = open (figure 5), pin 9 connected to V_{CC}	01	70	150	ns
	$t_{P(OUT)1}$	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = 80 pF ±10%, R_L = 390 Ω ±5%, R_X = open (figure 5), pin 9 connected to V_{CC}	06	70	168	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Limits		Units
				Min	Max	
Pulse width obtained with internal timing resistor	$t_{P(OUT)2}$	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = 15 pF ±10%, R_L = 390 Ω ±5%, R_X = open, pin 9 connected to V_{CC}, see figure 5	01, 06	20	50	ms
Pulse width obtained with external timing resistor	$t_{P(OUT)3}$	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = 100 pF ±10%, R_X = 10 kΩ ±5%, pin 9 open, figure 5	01, 06	600	825	ns
	$t_{P(OUT)4}$	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = 1,000 pF ±10%, R_X = 10 kΩ ±5%, pin 9 open, figure 5		5.5	8	
Propagation delay time to high level (A_1 or A_2 inputs to Q output)	t_{PLH1}	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = 1,000 pF ±10%, R_X = 10 kΩ ±5%, R_L = 390 Ω ±5%, figure 6 (device type 02), figure 7 (device type 03)	02, 03	7	48	ns
Propagation delay time to high level (B_1 or B_2 inputs to Q output)	t_{PLH2}		02, 03	7	41	ns
Propagation delay time to low level (A_1 or A_2 inputs to $\overline{Q}$ output)	t_{PHL1}		02, 03	7	56	ns
Propagation delay time to low level (B_1 or B_2 inputs to $\overline{Q}$ output)	t_{PHL2}		02, 03	7	51	ns
Propagation delay time to low level (clear input to Q output)	t_{PHL3}	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = 1,000 pF ±10%, R_X = 10 kΩ ±5%, R_L = 390 Ω ±5%, figure 6 (device type 02), figure 7 (device type 03)	02,03	7	39	ns
Propagation delay time to high level (clear input to $\overline{Q}$ output)	t_{PLH3}		02,03	7	56	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Limits		Units
				Min	Max	
Minimum pulse width of Q output pulse	$t_{W(MIN)}$	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = 0, R_X = 5 kΩ ±5%, R_L = 390 Ω ±5%, figure 6 (device type 02), figure 7 (device type 03)	02,03		75	ns
		V_{CC} = 5.0 V, 5/ C_L = 50 pF ±10%, C_X = 15 pF, R_X = 5 kΩ ±5%, R_L = 390 Ω ±5%, figure 6 (device type 02), figure 7 (device type 03)	02,03		105	
Width of Q output pulse	t_W	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = 1,000 pF ±10%, R_X = 10 kΩ ±5%, R_L = 390 Ω ±5%, figure 6 (device type 02), figure 7 (device type 03)	02,03	2.60	4.15	µs
Propagation delay time to high level (A_1 or A_2 inputs to Q output)	t_{PLH1}	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = open, R_X = 5 kΩ ±5%, R_L = 390 Ω ±5%, figure 8 (device type 04)	04	7	48	ns
Propagation delay time to high level (B_1 or B_2 inputs to Q output)	t_{PLH2}		04	7	41	ns
Propagation delay time to high level (A_1 or A_2 inputs to $\overline{Q}$ output)	t_{PHL1}		04	7	56	ns
Propagation delay time to high level (B_1 or B_2 inputs to $\overline{Q}$ output)	t_{PHL2}		04	7	51	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Limits		Units
				Min	Max	
Minimum pulse width of Q output pulse	$t_{W(MIN)}$	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = 0, R_X = 5 kΩ ±5%, R_L = 390 Ω ±5%, figure 8 (device type 04)	04	25	95	ns
		V_{CC} = 5.0 V, 5/ C_L = 50 pF ±10%, C_X = 15 pF max, R_X = 5 kΩ ±5%, R_L = 390 Ω ±5%, figure 8 (device type 04)		25	125	
Width of Q output pulse	t_W	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = 1,000 pF ±10%, R_L = 390 Ω ±5%, R_X = 10 kΩ ±5%, figure 8 (device type 04)	04	2.60	4.10	µs
Propagation delay time to high level (A input to Q output)	t_{PLH1}	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = open, R_X = 10 kΩ ±5%, R_L = 390 Ω ±5%, figure 9 (device type 05)	05	7	54	ns
Propagation delay time to high level (B input to Q output)	t_{PLH2}		05	7	51	ns
Propagation delay time to low level (A input to Q output)	t_{PHL1}		05	7	61	ns
Propagation delay time to low level (B input to Q output)	t_{PHL2}		05	7	58	ns
Propagation delay time to low level (clear input to Q output)	t_{PHL3}		05	7	39	ns
Propagation delay time to high level (clear input to Q output)	t_{PLH3}		05	7	56	ns

See footnote at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Limits		Units
				Min	Max	
Minimum pulse width of Q output pulse	$t_{W(MIN)}$	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = 0, R_X = 10 kΩ ±5%, R_L = 390 Ω ±5%, figure 9 (device type 05)	05	35	108	ns
		V_{CC} = 5.0 V, 5/ C_L = 50 pF ±10%, C_X = 15 pF max, R_X = 10 kΩ ±5%, R_L = 390 Ω ±5%, figure 9 (device type 05)	05	35	140	
Width of Q output pulse	t_W	V_{CC} = 5.0 V, C_L = 50 pF ±10%, C_X = 1,000 pF ±10%, R_L = 390 Ω ±5%, R_X = 10 kΩ ±5%, figure 9 (device type 05)	05	2.60	3.91	s

1/ Ground C_X to measure V_{OH} at Q, V_{OL} at $\overline{Q}$,or I_{OS} at Q. C_X is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$. (Device types 02 and 03).

2/ Not more than one output should be shorted at a time.

3/ For device types 02 and 03: I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, C_X = 0.02 μF and R_X = 25 kΩ. R_I of device type 02 is open.

4/ For device types 02 and 03: I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C_X = 0.02 μF and R_X = 25 kΩ. R_I of device type 02 is open.

5/ 15 pF load is for automatic test equipment only, which includes probe and jig capacitance.

3.6 Electrical test requirements. Electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.8 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.9 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 3 (see MIL-PRF-38535, appendix A).

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 7, 9, 10, 11	1*, 2, 3, 7, 9
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group B electrical test parameters when using the method 5005 QCI option	1,2,3, 9,10,11	N/A
Group C end-point electrical parameters	1,2,3, 9,10,11	1, 2, 3
Group D end-point electrical parameters	1, 2, 3	1, 2, 3

*PDA applies to subgroup 1.

4. VERIFICATION.

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as function as described herein.

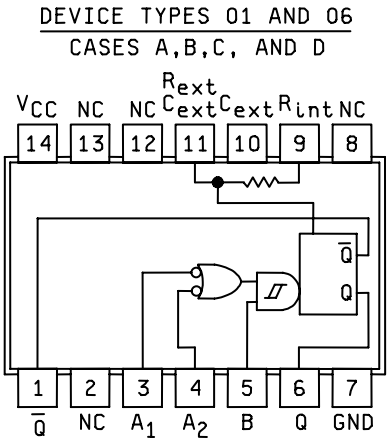
4.2 Screening. Screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

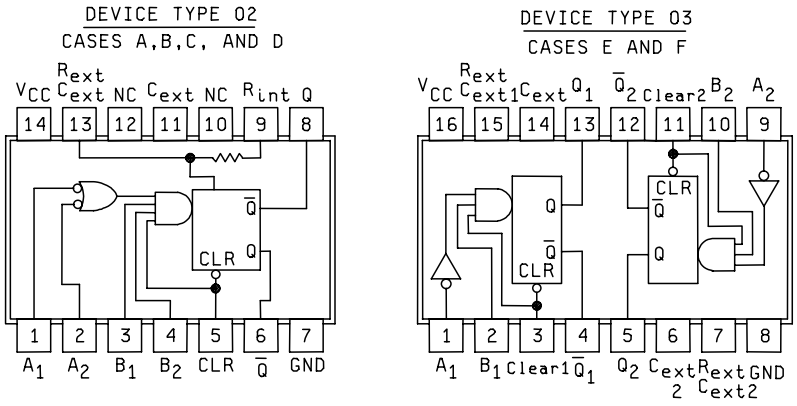
c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.



NOTES (Device types 01 and 06):

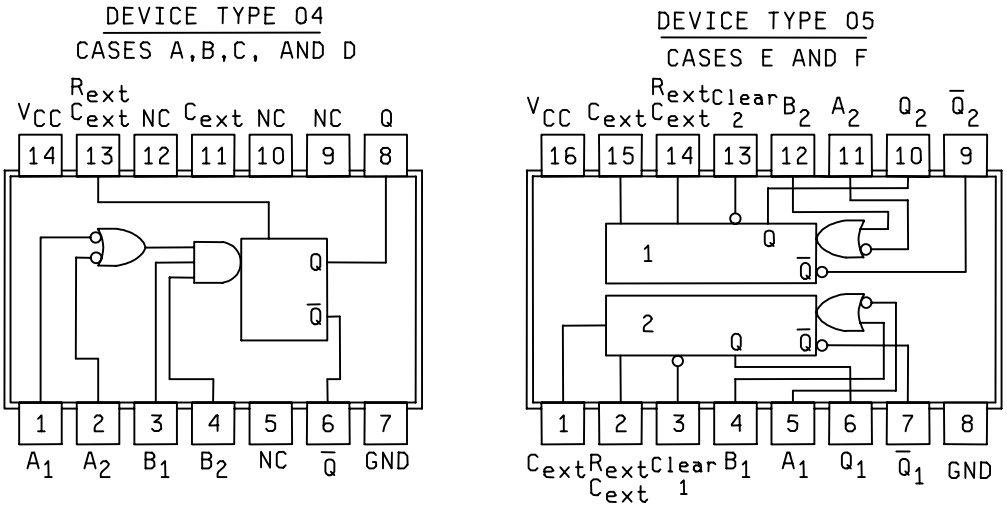
1. The use internal timing resistor (2 kΩ nominal) connect pin 9 (R_I) to pin 14 (V_{CC}).
2. To obtain a variable pulse width, connect external variable resistor between pins 9 (R_I) and 14 (V_{CC}). No external current limiting is required.
3. External timing capacitor may be connected between pins 10 (positive) (C_X) and 11 (R_X / C_X).



NOTE (device types 02 and 03):

An external timing capacitor may be connected between C_X and R_X / C_X (positive).

Figure 1. Logic diagrams and terminal connections (top view).



NOTE (device types 04 and 05):

An external timing capacitor (C_X) and an external timing resistor (R_X) are required between C_{ext} and R_{ext} / C_{ext} to determine output pulse duration and accuracy.

Figure 1. Logic diagrams and terminal connections (top views) – Continued.

DEVICE TYPES 01 and 06				
INPUTS			OUTPUTS	
A1	A2	B	Q	$\overline{Q}$
H	H	X	L	H
X	L	↓	L	H
L	X	↓	L	H
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
X	↑	L	L	H
↑	X	L	L	H
H	↑	H	L	H
↑	H	H	L	H
↑	↑	H	L	H

DEVICE TYPE 02						
INPUTS					OUTPUTS	
Clear	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	H	H	L	H
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎

DEVICE TYPE 03				
INPUTS			OUTPUTS	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↑	H	⎍	⎎
↑	L	H	⎍	⎎

NOTE:
H = High level (steady state), L = low level (steady state), ↑ = transition from low to high level,
↓ = transition from high to low level, ⎍ = one high level pulse, ⎎ = one low level pulse,
X = irrelevant (any input, including transitions).

FIGURE 2. Truth tables.

DEVICE TYPE 04					
INPUTS				OUTPUTS	
A_1	A_2	B_1	B_2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⊓	⊔
L	X	H	↑	⊓	⊔
X	L	H	H	L	H
X	L	↑	H	⊓	⊔
X	L	H	↑	⊓	⊔
H	↓	H	H	⊓	⊔
↓	↓	H	H	⊓	⊔
↓	H	H	H	⊓	⊔

DEVICE TYPE 05				
INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
H	H	↑	⊓	⊔
H	↑	L	⊓	⊔

NOTE:
H = High level (steady state), L = low level (steady state), ↑ = transition from low to high level,
↓ = transition from high to low level, ⊓ = one high level pulse, ⊔ = one low level pulse,
X = irrelevant (any input, including transitions).

FIGURE 2. Truth tables – Continued.

Description of device types 01, 02, and 06

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. Device types 01, 02 and 06 have an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired. Applications requiring more precise pulse widths and not requiring the clear feature can best be satisfied with device types 01 and 06.

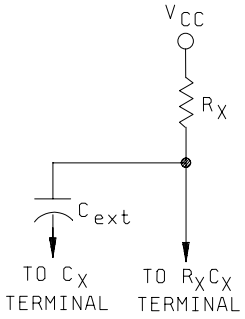
The output pulse is primarily a function of the external capacitor and resistor.
For $C_X > 1{,}000$ pF, the output pulse width (t_W) is defined as:

t_W (device type 01) = $R_X C_X$ Ln2

t_W (device type 02) = $0.32 R_X C_X (1 + (0.7/R_X))$

where R_X is in kΩ (either internal or external timing resistor)
C_X is in pF
t_W is in ns

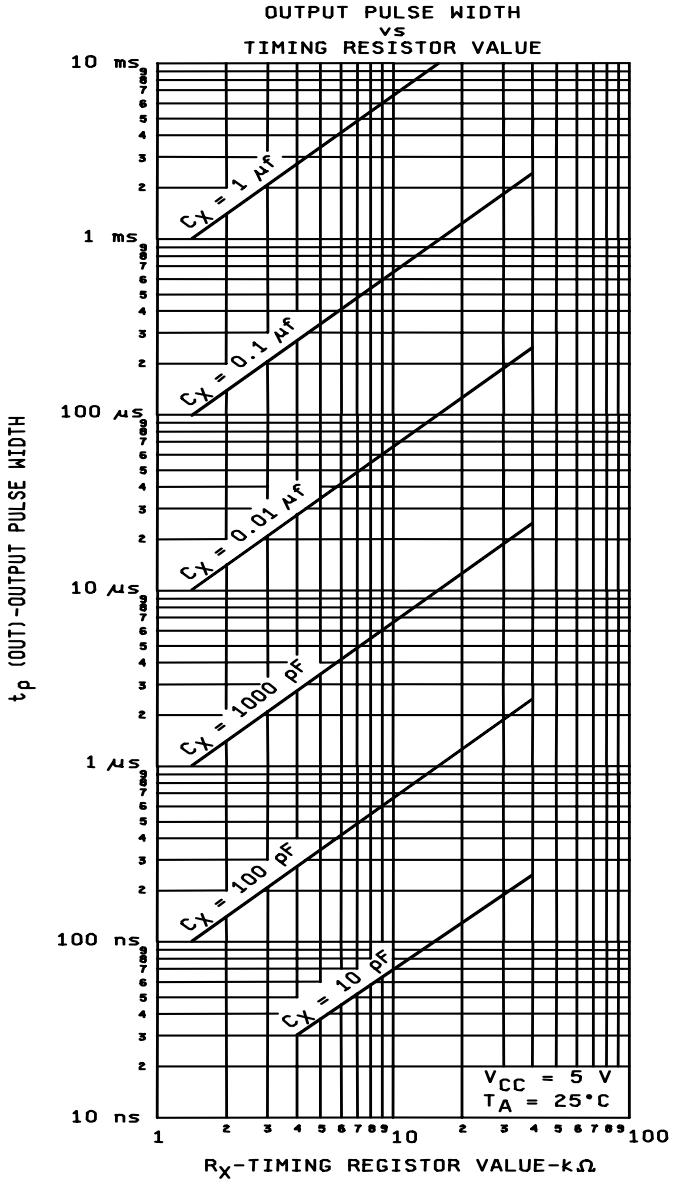
For pulse widths when $CX \leq 1{,}000$ pF, the following circuit for timing component connections is recommended.



These circuits are fully compatible with most TTL or DTL families. Inputs are diode-clamped to minimize reflections due to transmission-line effects, which simplifies design. Typical power dissipation per one shot is 115 milliwatts; typical average propagation delay time to the Q output is 21 nanoseconds.

FIGURE 3. Device descriptions.

Description of device types 01 and 06 –Continued.



NOTE: See 1.4 for maximum external timing resistance values.

FIGURE 3. Device descriptions – Continued.

B. Description of device types 01 and 06 –Continued.

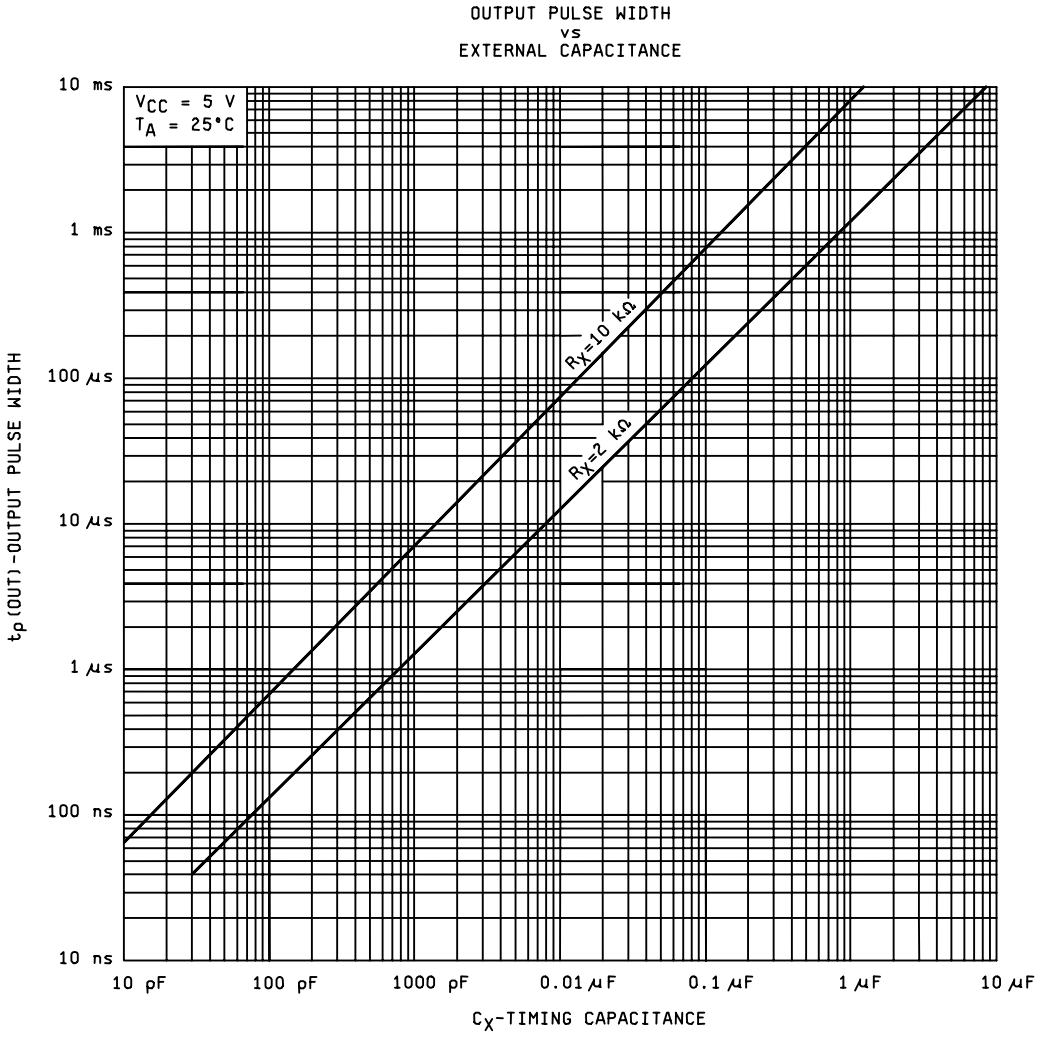
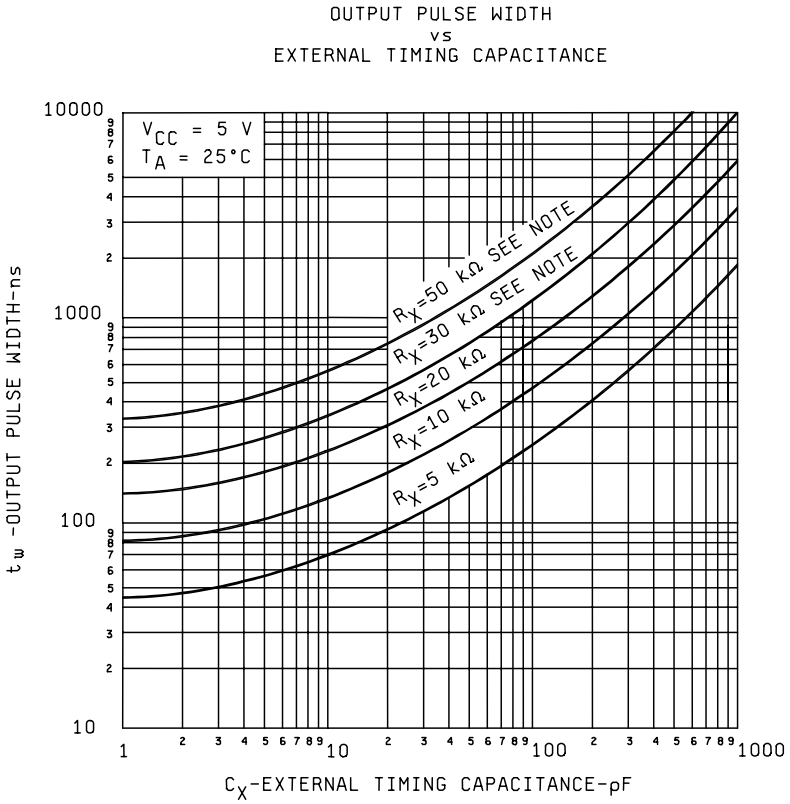


FIGURE 3. Device descriptions – Continued.

Description of device types 02 and 03

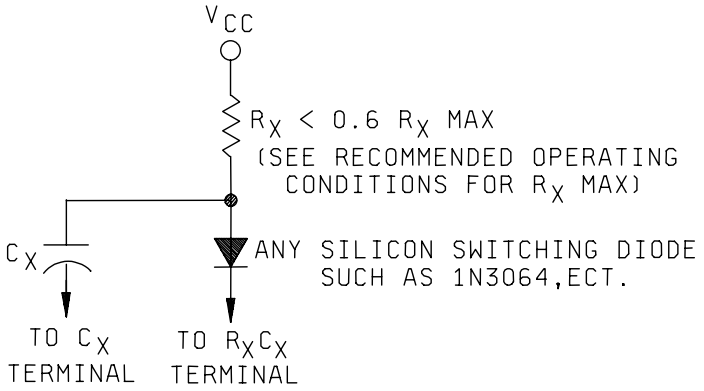


These values of resistance exceed the maximums recommended for use over the full temperature range.

FIGURE 3. Device descriptions – Continued.

Description of device types 02 and 03

To prevent reverse voltage across C_X, it is recommended that the following circuit be employed when using electrolytic capacitors and in applications utilizing the clear functions.
This circuit is also recommended for $C_X > 1{,}000$ pF.



In all applications using the diode, the pulse width is:

$$t_W = 0.28\ R_X\ C_X\ (1 + (0.7/R_X))$$

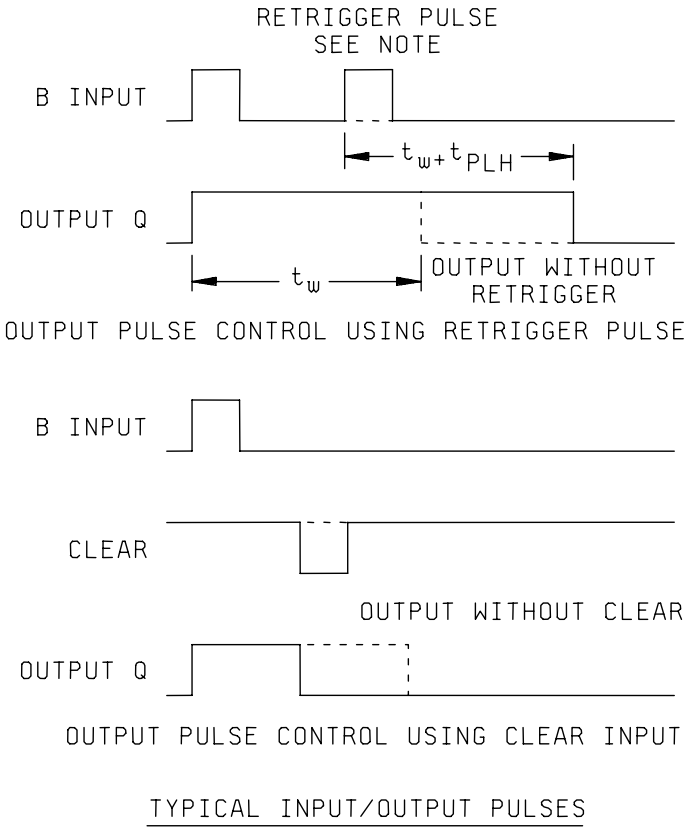
where R_X is in kΩ
C_X is in pF
t_W is in ns

FIGURE 3. Device descriptions – Continued.

Description of device types 02 and 03

These monolithic TTL retriggerable monostable multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. The retrigger capability simplies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

Waveforms below illustrates triggering the one-shot with the high-level-active (B) inputs.



TYPICAL INPUT/OUTPUT PULSES

NOTE: Retrigger pulse must not start before 0.22 C_X (in picofarads) nanoseconds after previous trigger pulse.

FIGURE 3. Device descriptions – Continued.

Description of device type 04

These retriggerable monostables multivibrator provides an output pulse whose duration and accuracy is a function of external timing components. It is designed to allow a choice of triggering either the leading or trailing edge of the pulse, thus providing the system designer with complete flexibility in controlling the pulse width.

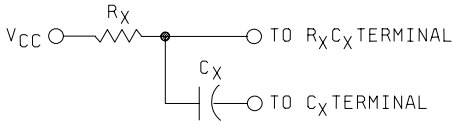
The output pulse width is primarily a function of the external capacitor and external resistor.
For $C_X \geq 1{,}000$ pF, the output pulse width (t_W) is defined as:

$$t_W = 0.32\ R_X\ C_X\ (1 + (0.7/R_X))$$

where R_X is in kΩ (see note 3)
C_X is in pF (see note 2)
t_W is in ns

For pulse widths when $C_X < 1{,}000$ pF, the following circuit for timing component connections is recommended.

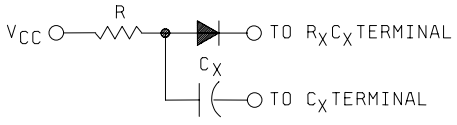
Circuit A. This circuit is for use with low leakage electrolytic capacitors. This configuration can be used predictability only if the forward capacitor leakage at 5.0 volts is less than 3 μA, and the reverse capacitor leakage at 1.0 volt is less than 5 μA over the operational temperature range, and note 1 below is satisfied.



Circuit B. This circuit is for use with high reverse leakage current electrolytic capacitors. The diode in this configuration prevents high reverse leakage currents through the capacitor by preventing a reverse voltage across the capacitor.

$$t_W \approx 0.3\ R_X$$

Any silicon switching diode such as 1N3064, etc.



$R < 0.6\ R_X$ (maximum) (see recommended operating conditions for R_X maximum).

FIGURE 3. Device descriptions – Continued.

Description of device type 04 - Continued

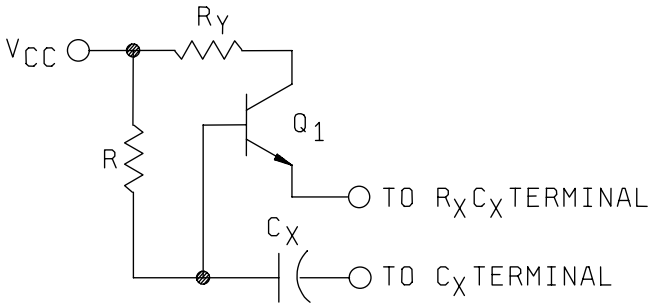
Circuit C. This circuit is used to obtain extended pulse width. This configuration obtains extended pulse widths, because of the larger timing resistor allowed by Beta multiplication.
Electrolytics with high ($> 5\ \mu A$) reverse leakage currents can be used.

$R < R_X\ (0.7)\ (h_{FE}Q1)$ or $< 2.5\ M\Omega$ whichever is lesser.

R_X (minimum) $< RY <$ (maximum) ($5 \leq R_Y \leq 10\ k\Omega$ is recommended).

Q1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962.

$t_W \approx 0.3\ RC_X$.



NOTES:

1. C_X may vary from 0 to any necessary value available. If however, the capacitor has leakage approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse with obtained.
2. Configuration B and C are not recommended with retriggerable operation.
3. R_X may vary from 5.0 to 25 $k\Omega$

FIGURE 3. Device descriptions – Continued.

Description of device type 04

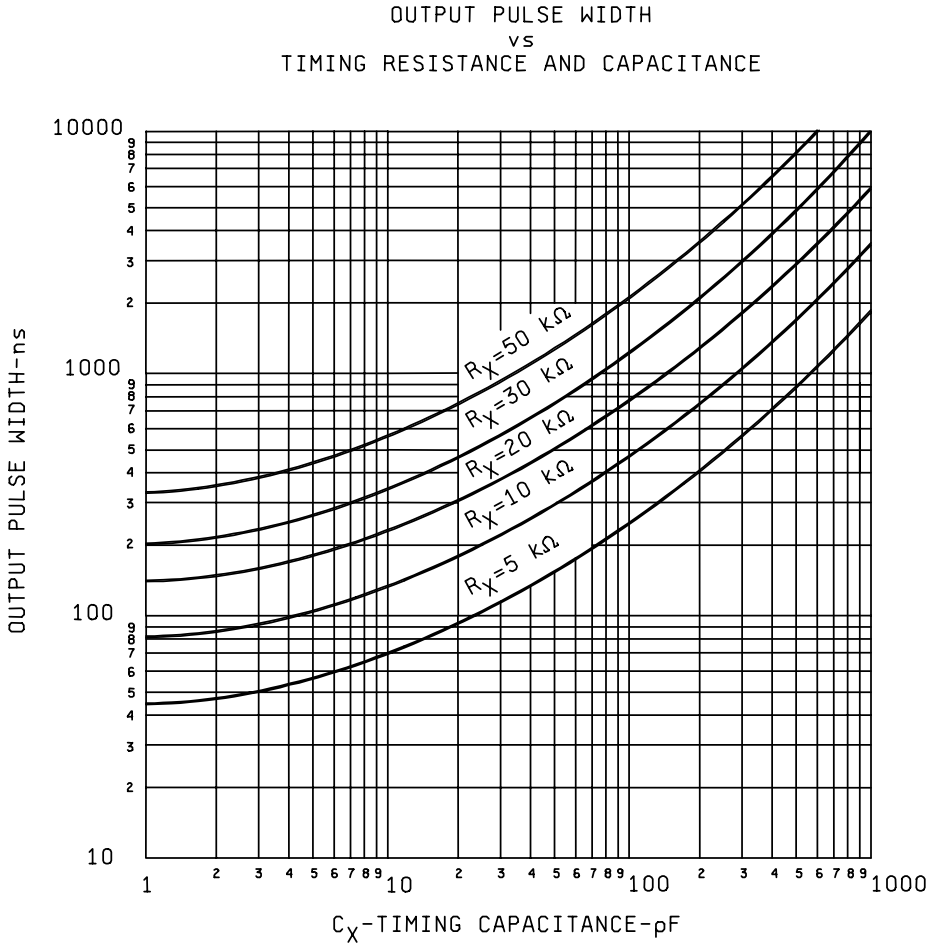
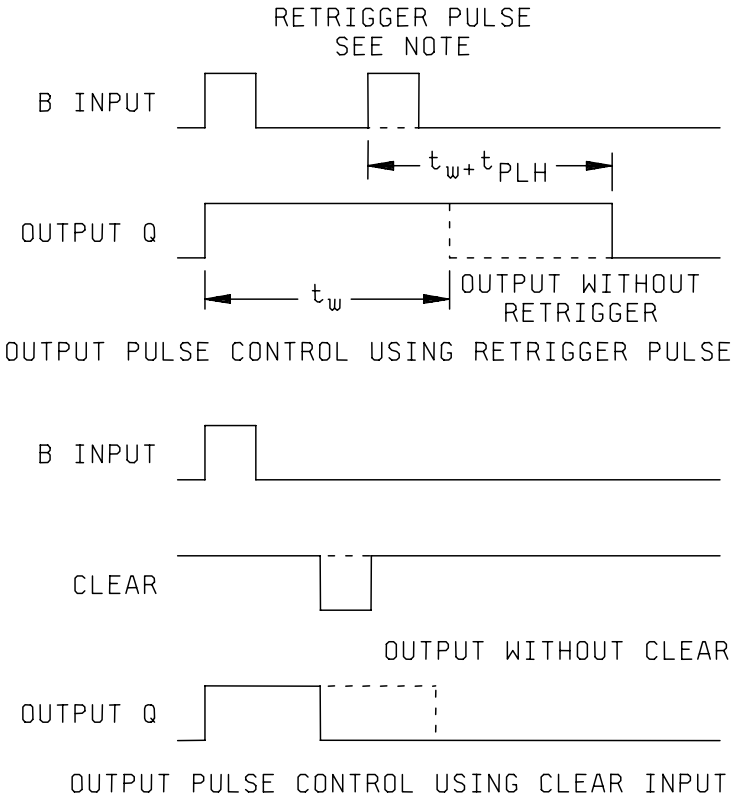


FIGURE 3. Device descriptions – Continued.

Description of device types 04 and 05

These monolithic TTL retriggerable monostable multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. The retrigger capability simplies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. For device type 05, the overriding clear permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

Waveforms below illustrates triggering the one-shot with the high-level-active (B) inputs.



TYPICAL INPUT / OUTPUT PULSES

NOTE: Retrigger pulse must not start before 0.3 C_X nanoseconds after previous trigger pulse.

FIGURE 3. Device descriptions – Continued.

Description of device type 05

This dual retriggerable, resettlable monostables multivibrator provides an output pulse whose duration and accuracy is a function of external timing components. It is designed to allow a choice of triggering either the leading or trailing edge of the pulse, thus providing the system designer with complete flexibility in controlling the pulse width.

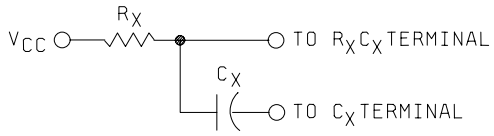
The output pulse width is primarily a function of the external capacitor and external resistor.
For $C_X \geq 1{,}000$ pF, the output pulse width (t_W) is defined as:

$$t_W = 0.31\ R_X\ C_X\ (1 + (1/R_X))$$

where R_X is in kΩ (see note 3)
C_X is in pF (see note 2)
t_W is in ns

For pulse widths when $C_X < 1{,}000$ pF, the following circuit for timing component connections is recommended.

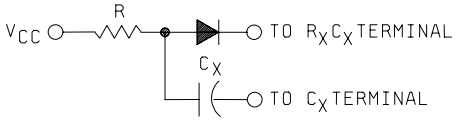
Circuit A. This circuit is for use with low leakage electrolytic capacitors. This configuration can be used predictability only if the forward capacitor leakage at 5.0 volts is less than 3 μA, and the reverse capacitor leakage at 1.0 volt is less than 5 μA over the operational temperature range, and note 1 below is satisfied.



Circuit B. This circuit is for use with high reverse leakage current electrolytic capacitors. The diode in this configuration prevents high reverse leakage currents through the capacitor by preventing a reverse voltage across the capacitor.

$$t_W = 0.3\ R_X$$

Any silicon switching diode such as 1N3064, etc.



$R < 0.6\ R_X$ (maximum) (see recommended operating conditions for R_X maximum).

FIGURE 3. Device descriptions – Continued.

Description of device type 05 - Continued

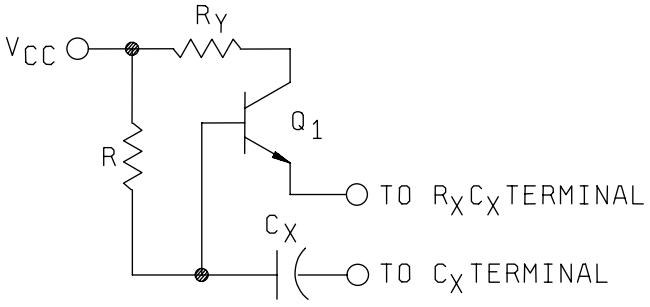
Circuit C. This circuit is used to obtain extended pulse widths. This configuration obtains extended pulse widths, because of the larger timing resistor allowed by Beta multiplication.
Electrolytics with high inverse leakage currents can be used.

$R < R_X$ (0.7) ($h_{FE}Q1$) or < 2.5 MΩ whichever is lesser.

R_X (minimum) < R_Y < (maximum) ($5 \leq R_Y \leq 10$ kΩ is recommended).

Q1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962.

$t_W \approx 0.3\ RC_X$.



NOTES:

1. C_X may vary from 0 to any necessary value available. If however, the capacitor has leakage approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
2. Configuration B and C are not recommended with retriggerable operation.
3. R_X may vary from 5.0 to 25 kΩ

FIGURE 3. Device descriptions – Continued.

Description of device type 05

OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE

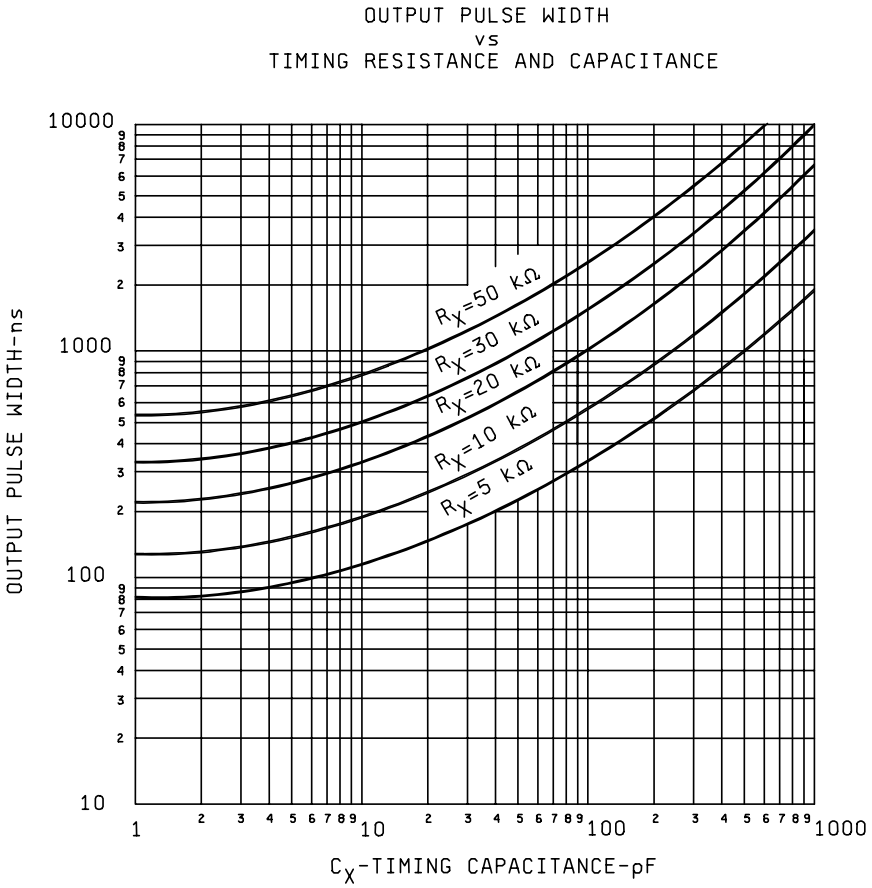
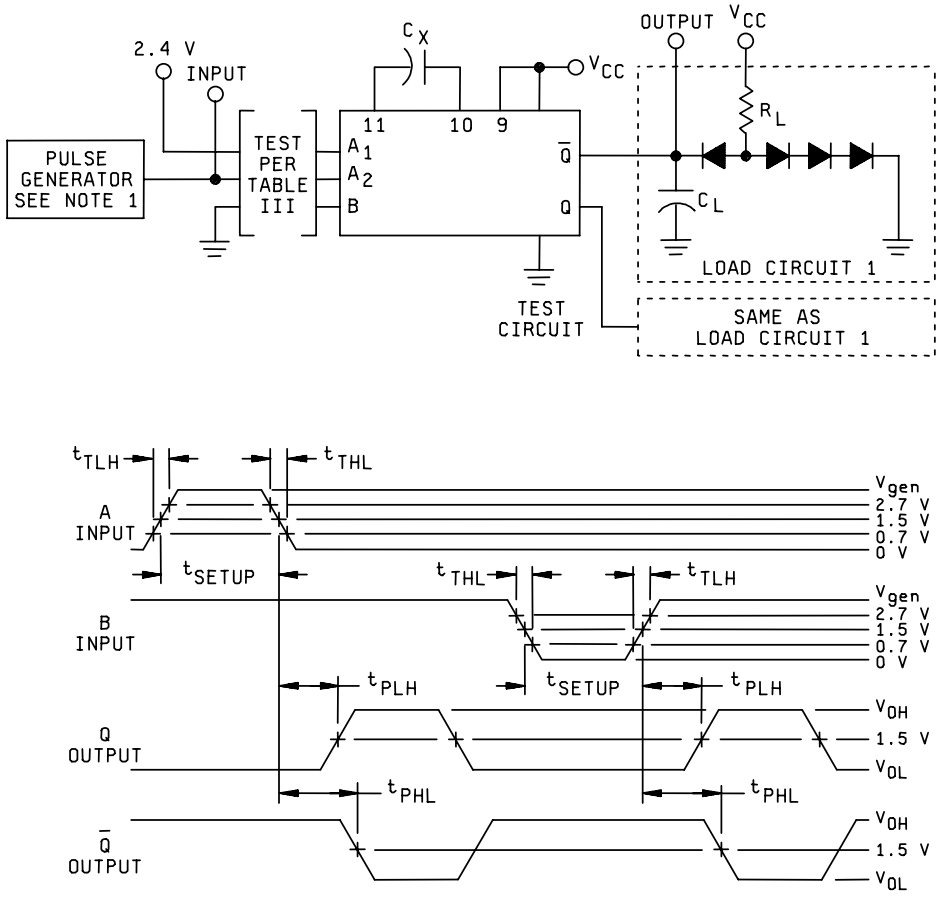


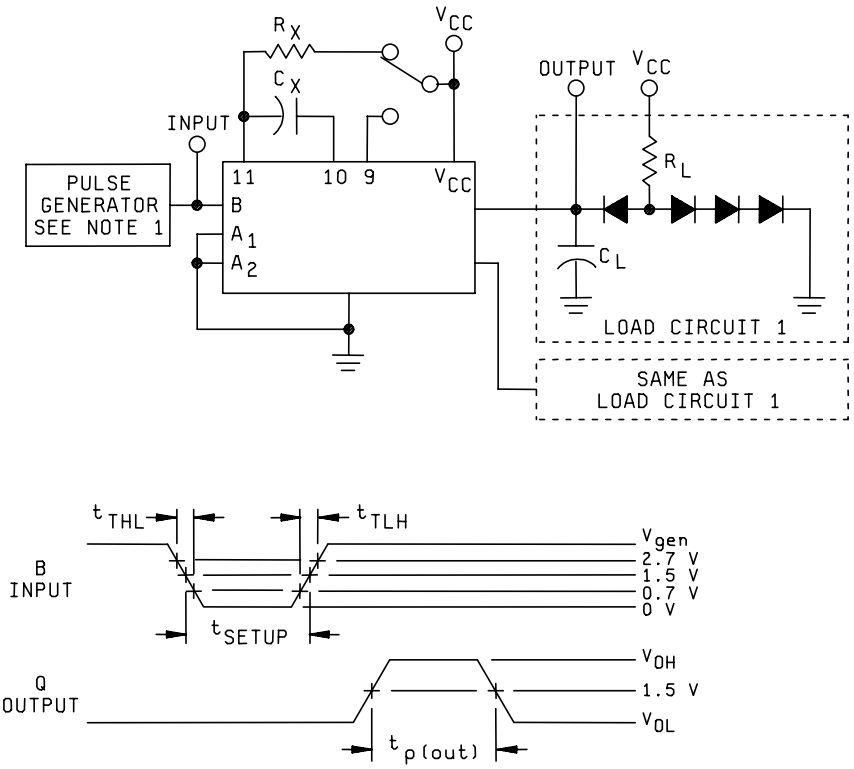
FIGURE 3. Device descriptions – Continued.



NOTES:

1. The pulse generator has the following characteristics: V_{gen} = 3.0 V, $t_{THL} \leq 10$ ns, $t_{TLH} < 10$ ns, t_{SETUP} = 60 ns, PRR ≤ 1 MHz, and $Z_{OUT} \approx 50\ \Omega$.
2. All diodes are 1N3064 or equivalent.
3. C_L = 50 pF minimum including probe and jig capacitance.
4. $R_L = 390\ \Omega \pm 5\ \%$.
5. V_{CC} = 5.0 V minimum.
6. See table III for R_X and C_X values.

FIGURE 4. Switching test circuit for t_{PHL} and t_{PLH} of device types 01 and 06.



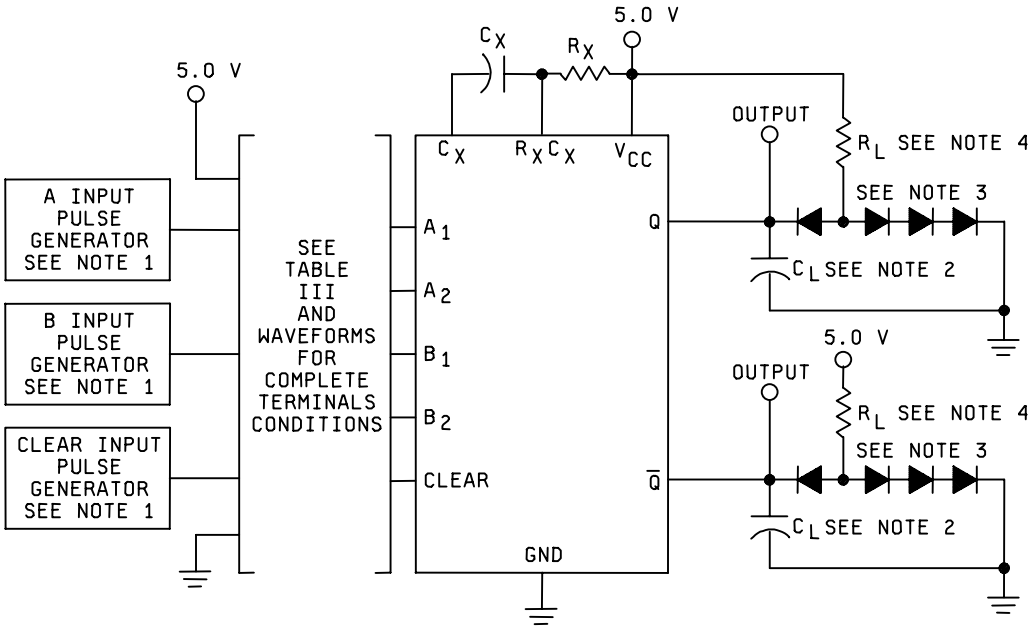
NOTES:

1. The pulse generator has the following characteristics: V_{gen} = 3.0 V, $t_{THL} \leq 10$ ns, $t_{TLH} < 10$ ns, t_{SETUP} = 60 ns, $Z_{OUT} \approx 50\ \Omega$, and PRR is as follows:

TEST	PRR
t_P(out) 1 and t_P(out) 2	1 MHz
t_P(out) 3	500 kHz
t_P(out) 4	20 kHz

2. V_{CC} = 5.0 V minimum, R_L = 390 Ω ±5 %, C_L = 50 pF minimum including probe and jig capacitance.
3. See table III for R_X and C_X values.
4. All diodes are 1N3064 or equivalent.

FIGURE 5. Switching test circuit for t_{SETUP} and $t_{P(out)}$ of device types 01 and 06.

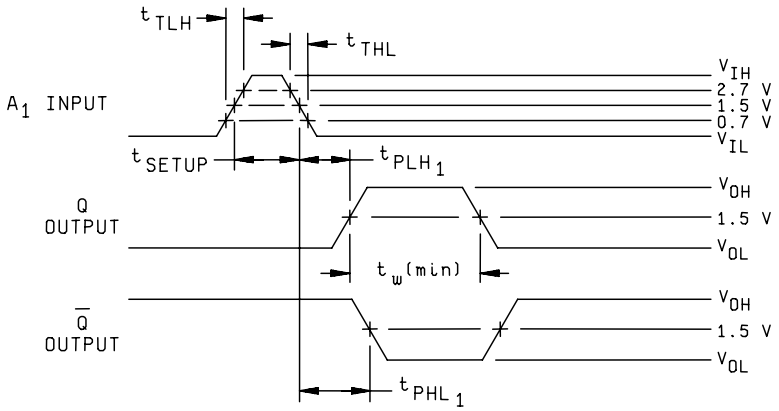


NOTES:

1. Unless otherwise specified in the notes with individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} < 10$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$ V and $Z_{OUT} \approx 50\ \Omega$.
2. $C_L = 50$ pF minimum including probe and jig capacitance.
3. All diodes are 1N3064 or equivalent.
4. $R_L = 390\ \Omega \pm 5$ %.
5. See table III for R_X and C_X values.

FIGURE 6. Switching test circuit and waveforms for device type 02.

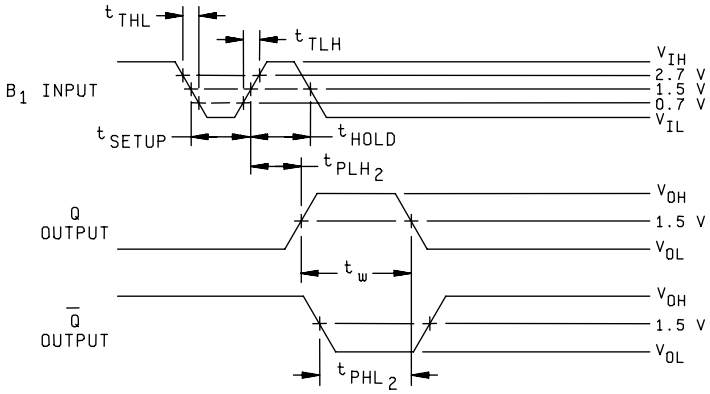
A1 INPUT to Q and $\overline{Q}$ OUTPUTS (t_{PLH1}, t_{PHL1}) (t_W min)



NOTES:

1. A_1 input characteristics: PRR ≤ 1 MHz, t_{SETUP} = 40 ns.
2. A_2, B_1, B_2, and clear = 5.0 V.

B_1 INPUT to Q and $\overline{Q}$ OUTPUTS (t_{PLH2}, t_{PHL2}) (t_W)

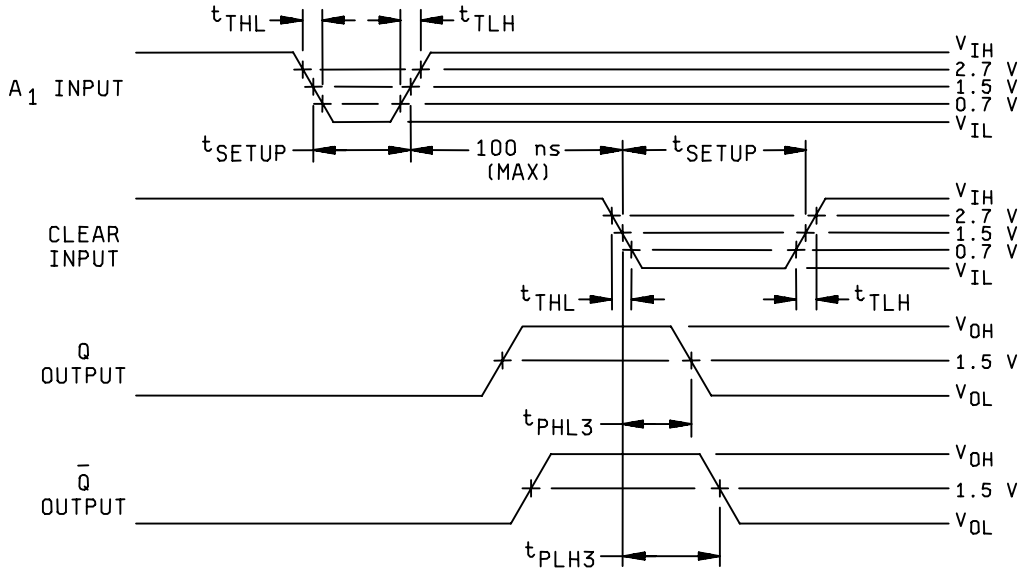


NOTES:

1. B_1 input characteristics: PRR ≤ 1 MHz, t_{SETUP} = 40 ns, t_{HOLD} = 40 ns.
2. A_1, A_2 = GND, B_2, clear = 5.0 V.

FIGURE 6. Switching test circuit and waveforms for device type 02 – Continued.

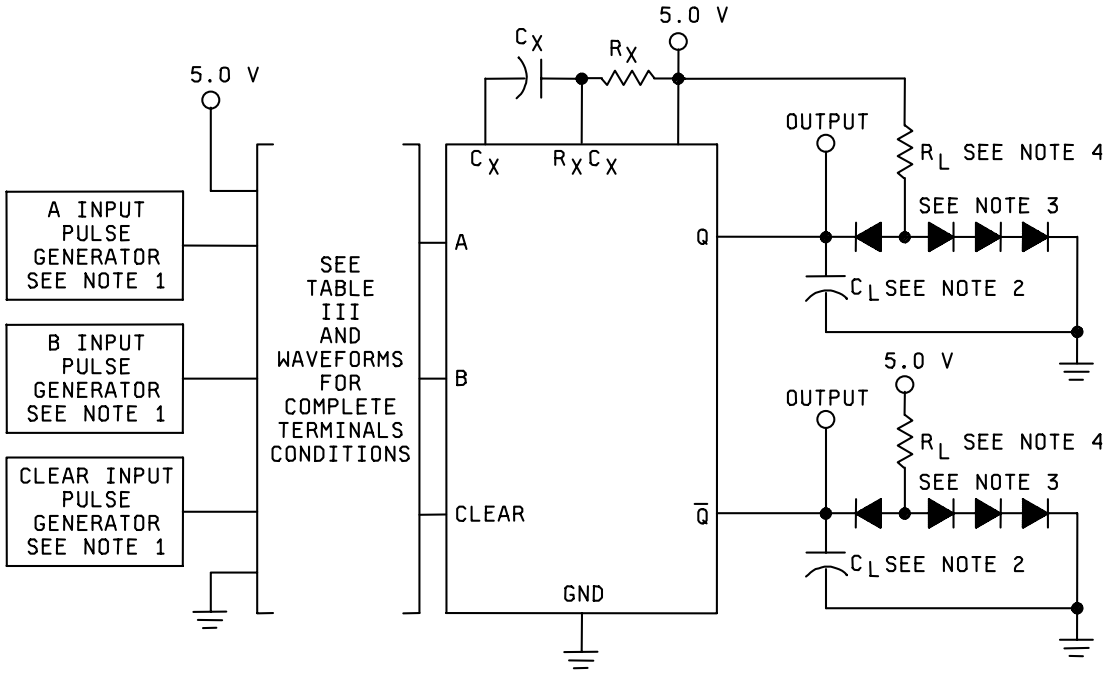
CLEAR to Q and $\overline{Q}$ OUTPUTS (t_{PLH3} and t_{PHL3})



NOTES:

1. A_1 input characteristics: PRR ≤ 1 MHz, t_{SETUP} = 40 ns.
2. Clear input characteristics: PRR ≤ 1 MHz, t_{SETUP} = 100 ns.
3. A_2, B_1, B_2 = 5.0 V.

FIGURE 6. Switching test circuit and waveforms for device type 02 – Continued.

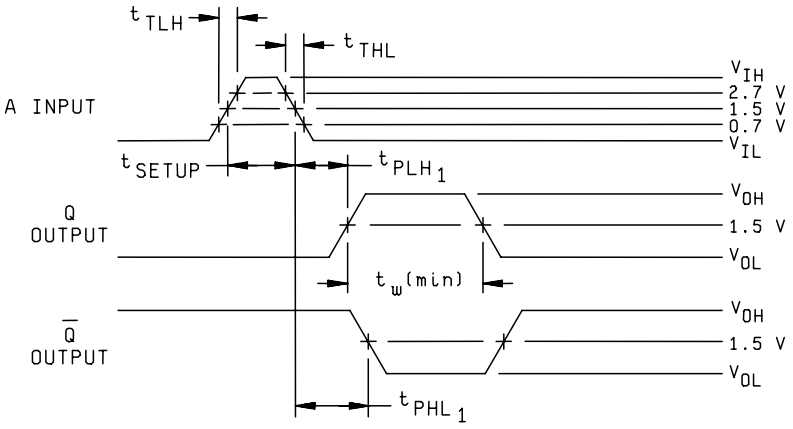


NOTES:

1. Unless otherwise specified in the notes with individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} \leq 10$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$ V and $Z_{OUT} \approx 50\ \Omega$.
2. $C_L = 50$ pF minimum including probe and jig capacitance.
3. All diodes are 1N3064 or equivalent.
4. $R_L = 390\ \Omega \pm 5$ %.
5. See table III for R_X and C_X values.

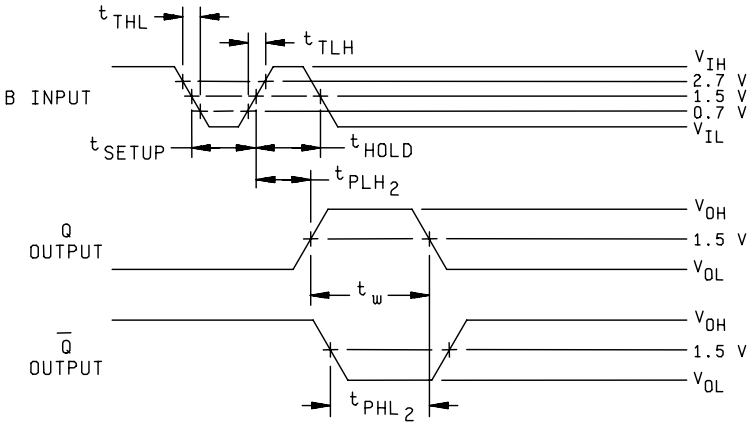
FIGURE 7. Switching test circuit and waveforms for device type 03.

A INPUT to Q and $\overline{Q}$ OUTPUTS (t_{PLH1}, t_{PHL1}) (t_W min)



NOTES:
1. A input characteristics: PRR ≤ 1 MHz, t_{SETUP} = 40 ns.
2. B and clear = 5.0 V.

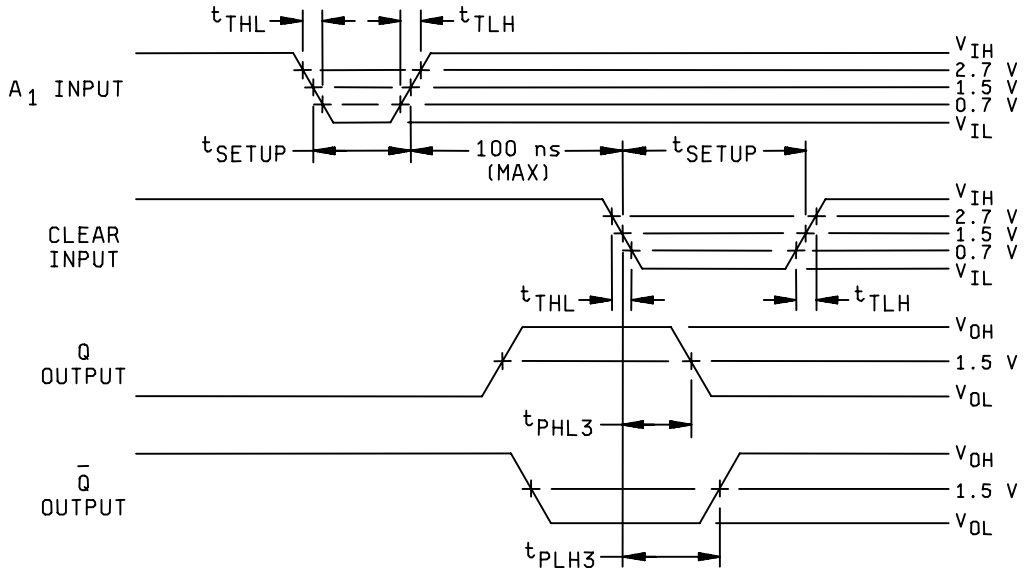
B INPUT to Q and $\overline{Q}$ OUTPUTS (t_{PLH2}, t_{PHL2}) (t_W)



NOTES:
1. B input characteristics: PRR ≤ 285 kHz, t_{SETUP} = 40 ns, t_{HOLD} = 40 ns.
2. A = GND, clear = 5.0 V.

FIGURE 7. Switching test circuit and waveforms for device type 03 – Continued.

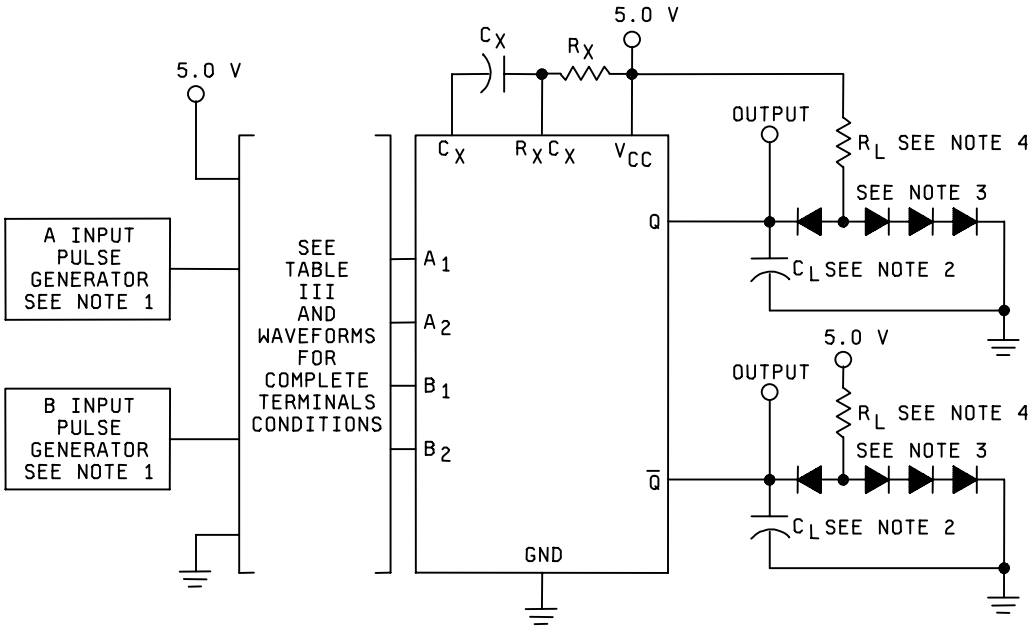
CLEAR to Q and $\overline{Q}$ OUTPUTS (t_{PLH3} and t_{PHL3})



NOTES:

1. A_1 input characteristics: PRR ≤ 285 kHz, t_{SETUP} = 40 ns.
2. Clear input characteristics: PRR ≤ 285 kHz, t_{SETUP} = 100 ns.
3. B = 5.0 V.

FIGURE 7. Switching test circuit and waveforms for device type 03 – Continued.

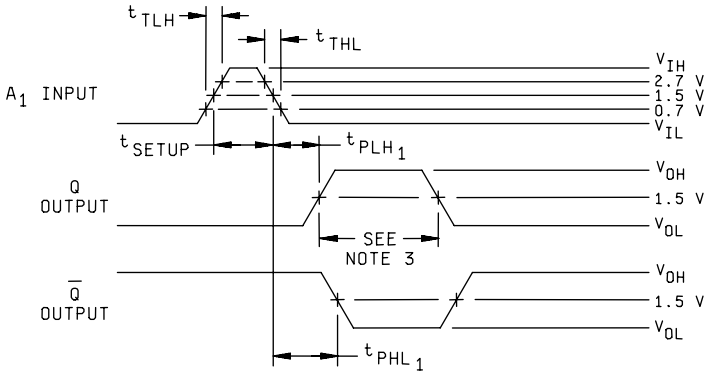


NOTES:

1. Unless otherwise specified in the notes with individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} < 10$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$ V and $Z_{OUT} \approx 50\ \Omega$.
2. $C_L = 50$ pF minimum including probe and jig capacitance.
3. All diodes are 1N3064 or equivalent.
4. $R_L = 390\ \Omega \pm 5$ %.
5. See table III for R_X and C_X values.

FIGURE 8. Switching test circuit and waveforms for device type 04.

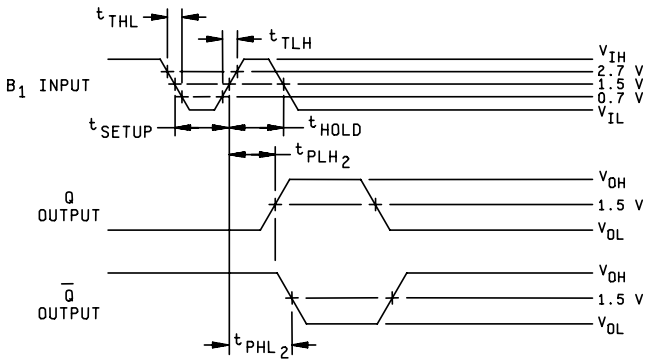
A1 INPUT to Q and $\overline{Q}$ OUTPUTS (t_{PLH1}, t_{PHL1}) (t_W) (t_W min)



NOTES:

1. A_1 input characteristics: PRR ≤ 1 MHz, t_{SETUP} = 40 ns.
2. A_2, B_1, and B_2 = 5.0 V.
3. t_W and t_W (min)

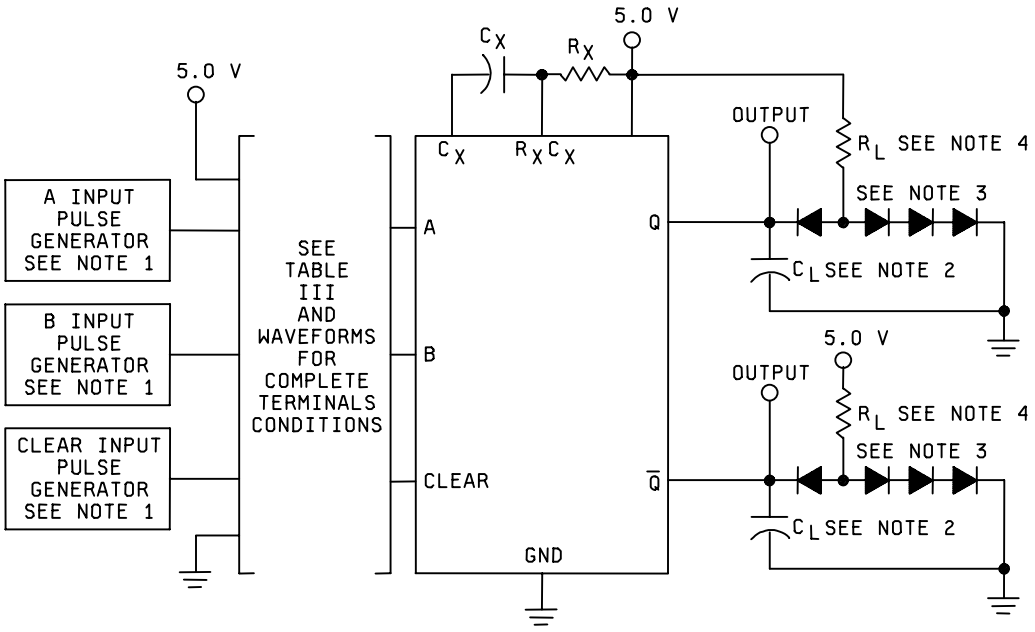
B_1 INPUT to Q and $\overline{Q}$ OUTPUTS (t_{PLH2}, t_{PHL2})



NOTES:

1. B_1 input characteristics: PRR ≤ 1 MHz, t_{SETUP} = 40 ns, t_{HOLD} = 40 ns.
2. A_1, A_2 = GND, B_2 = 5.0 V.

FIGURE 8. Switching test circuit and waveforms for device type 04 – Continued.

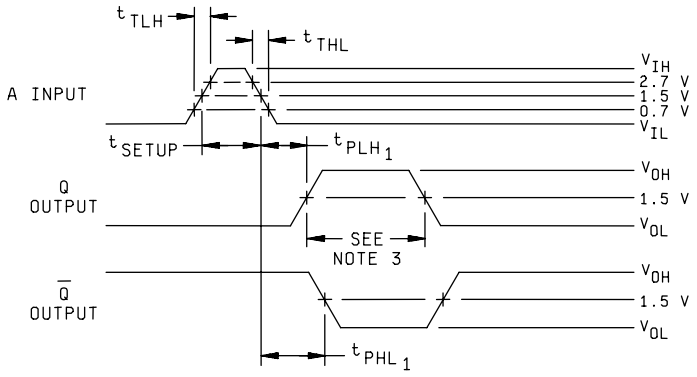


NOTES:

1. Unless otherwise specified in the notes with individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} < 10$ ns, $V_{IH} = 3.0$ V minimum, $V_{IL} = 0$ V and $Z_{OUT} \approx 50\ \Omega$.
2. $C_L = 50$ pF minimum including probe and jig capacitance.
3. All diodes are 1N3064 or equivalent.
4. $R_L = 390\ \Omega \pm 5$ %.
5. See table III for R_X and C_X values.

FIGURE 9. Switching test circuit and waveforms for device type 05.

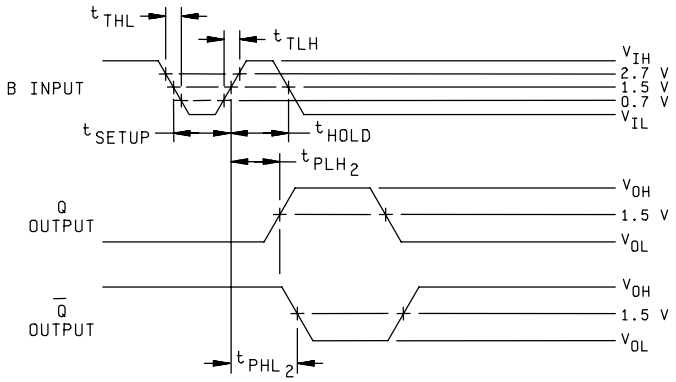
A INPUT to Q and $\overline{Q}$ OUTPUTS (t_{PLH1}, t_{PHL1}) (t_W) (t_W min)



NOTES:

1. A input characteristics: PRR ≤ 1 MHz, t_{SETUP} = 40 ns.
2. B = GND, and clear = 5.0 V.
3. t_W and t_W (min)

B INPUT to Q and $\overline{Q}$ OUTPUTS (t_{PLH2}, t_{PHL2})

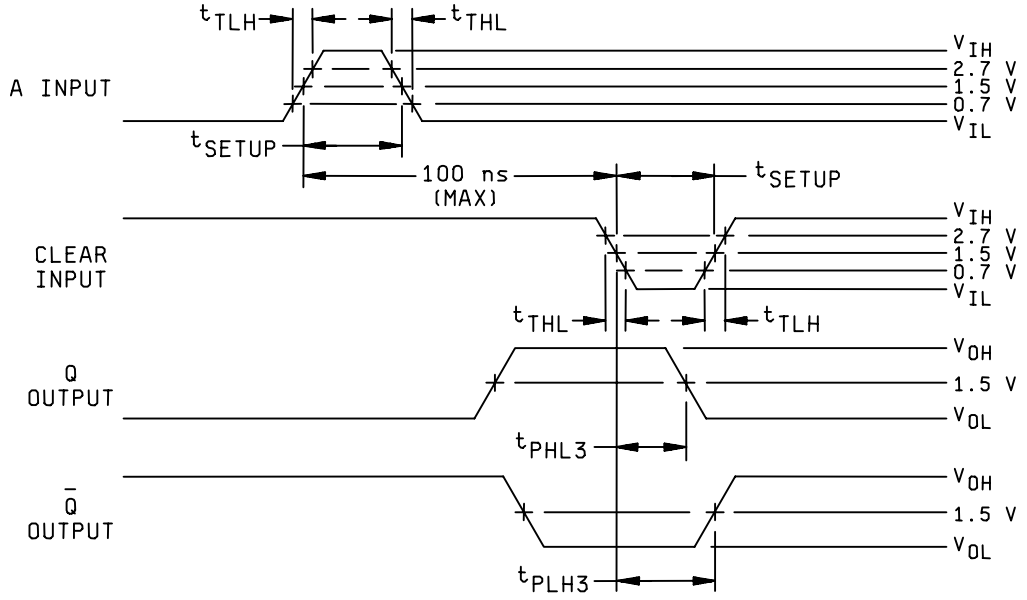


NOTES:

1. B input characteristics: PRR ≤ 1 MHz, t_{SETUP} = 40 ns, t_{HOLD} = 40 ns.
2. A and clear = 5.0 V.

FIGURE 9. Switching test circuit and waveforms for device type 05 – Continued.

CLEAR to Q and $\overline{Q}$ OUTPUTS (t_{PLH3} and t_{PHL3})



NOTES:

1. A input characteristics: PRR ≤ 1 MHz, t_{SETUP} = 40 ns.
2. Clear input characteristics: PRR ≤ 1 MHz, t_{SETUP} = 40 ns.
3. B = GND

FIGURE 9. Switching test circuit and waveforms for device type 05 – Continued.

TABLE III. Group A inspection for device types 01 and 06.
Terminal conditions (pins not designated may be high ≥ 2.4 V, low ≤ 0.4 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
				$\overline{Q}$	NC	A_1	A_2	B	Q	GND	NC	R_I	C_X	R_XC_X	NC	NC	V_{CC}
1 Tc =+25°C	V_{OL}	3007 1/	1			0.8 V	0.8 V	0.8 V	16 mA	GND		4.5 V					4.5 V
		3007	2	16 mA		"	2.0 V	"		"		GND	GND				"
	V_{OH}	3006 1/	3	-.4 mA		"	0.8 V	"		"		4.5 V					"
		"	4			"	2.0 V	"	-.4 mA	"		GND	GND				"
	V_{IC}		5			-12 mA				"							"
			6				-12 mA			"							"
			7					-12 mA		"							"
	I_{IL1}	3009	8			0.4 V	5.5 V			"							5.5 V
		3009	9			5.5 V	0.4 V			"							"
	I_{IL2}	3009	10			GND	GND	0.4 V		"		4.5 V					5.5 V
	I_{IH1}	3010	11			2.4 V	GND			"							"
		"	12			GND	2.4 V			"							"
	I_{IH2}	"	13			5.5 V	GND			"							"
		"	14			GND	5.5 V			"							"
	I_{IH3}	"	15			5.5 V	5.5 V	2.4 V		"		4.5 V					"
	I_{IH4}	"	16			5.5 V	5.5 V	5.5 V		"		4.5 V					"
	I_{OS}	3011	17			GND	GND		GND	"		GND	GND	GND			"
	"	"	18	GND		"	"	GND		"		5.5 V					"
	I_{CC1}	3005	19			"	"	"		"		5.5 V					"
	I_{CC2}	"	20			"	"	"		"		GND	GND				"
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = 125° C, and $V_{I\,C}$ tests are omitted.																
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55° C, and $V_{I\,C}$ tests are omitted.																
7 Tc =+25°C	Truth table test 14/	3014	21	H		A	A	2/	L	GND		3/	4/	4/			5.0 V
		"	22	"		"	A	5/	"	"		"	"	"			"
		"	23	"		"	B	5/	"	"		"	"	"			"
		"	24	"		B	A	5/	"	"		"	"	"			"
		"	25	"		B	2/	B	"	"		"	"	"			"
		"	26	"		2/	B	"	"	"		"	"	"			"
		"	27	"		A	2/	"	"	"		"	"	"			"
		"	28	"		2/	A	"	"	"		"	"	"			"
		"	29	"		2/	2/	"	"	"		"	"	"			"
		"	30	"		A	2/	A	"	"		"	"	"			"
		"	31	"		2/	A	"	"	"		"	"	"			"
		"	32	"		2/	2/	"	"	"		"	"	"			"
		"	33	7/		B	A	2/	8/	"		"	"	"			"
		"	34	"		A	B	2/	"	"		"	"	"			"
		"	35	"		A	5/	A	"	"		"	"	"			"
		"	36	"		5/	A	"	"	"		"	"	"			"
		"	37	"		5/	5/	"	"	"		"	"	"			"
8	Repeat subgroup 7 at T_C = +125°C and T_C = -55°C. 14/																

See footnotes at end of device type 01

TABLE III. Group A inspection for device types 01 and 06 – Continued.
Terminal conditions (pins not designated may be high ≥ 2.4 V, low ≤ 0.4 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14
			Test no.	$\overline{Q}$	NC	A_1	A_2	B	Q	GND	NC	R_1	C_X	R_XC_X	NC	NC	V_{CC}
9	t_{PLH1}	3003	38			GND		IN	OUT	GND		3/	9/	9/			5.0 V
Tc = +25°C	t_{PHL1}	(Fig. 4)	39	OUT		GND		IN		"		"	"	"			"
	t_{PLH2}	"	40			5.0 V	IN	5.0 V	OUT	"		"	"	"			"
	t_{PHL2}	"	41	OUT		5.0 V	IN	5.0 V		"		"	"	"			"
	$t_{P(OUT)1}$	3003	42			GND	GND	IN	OUT	"		"	"	"			"
	$t_{P(OUT)2}$	(Fig. 5)	43			"	"	"	"	"		"	10/	10/			"
	$t_{P(OUT)3}$	"	44			"	"	"	"	"			11/	11/ 13/			"
	$t_{P(OUT)4}$	"	45			"	"	"	"	"			12/	12/ 13/			"
10	t_{PLH1}	3003	46			"		"	"	"		3/	9/	9/			"
Tc = +125°C	t_{PHL1}	(Fig. 4)	47	OUT		"		"		"		"	"	"			"
	t_{PLH2}	"	48			5.0 V	IN	5.0 V	OUT	"		"	"	"			"
	t_{PHL2}	"	49	OUT		5.0 V	IN	5.0 V		"		"	"	"			"
	$t_{P(OUT)1}$	3003	50			GND	GND	IN	OUT	"		"	"	"			"
	$t_{P(OUT)2}$	(Fig. 5)	51			"	"	"	"	"		"	10/	10/			"
	$t_{P(OUT)3}$	"	52			"	"	"	"	"			11/	11/ 13/			"
	$t_{P(OUT)4}$	"	53			"	"	"	"	"			12/	12/ 13/			"
11	Same tests, terminal conditions and limits as for subgroup 10, except T_C = -55°C.																

1/ For circuit D, test numbers 2 and 4, terminal A_2 shall be 0.8 V shall be 2.0 V.

2/ In transition from low level to high level.

3/ R1 connected to V_{CC}.

4/ R_XC_X and C_X are open.

5/ In transition from high level to low level.

6/ Output voltages fro subgroups 7 and 8: H ≥ 1.5 V, L ≤ 1.5 V.

7/ One low logic level pulse.

8/ One high logic level pulse.

9/ C_X connected to R_XC_X through an 80 pF capacitor.

10/ C_X connected to R_XC_X through an 25 pF capacitor which includes stray, probe, and jig capacitor.

11/ C_X connected to R_XC_X through an 100 pF capacitor.

12/ C_X connected to R_XC_X through an 1,000 pF capacitor.

13/ R_XC_X connected to V_{CC} through a 10 kΩ resistor.

14/ A = 2.0 V and B = 0.8 V for subgroup 7. A = 2.4 V and B = 0.4 V for subgroup 8.

15/ For device type 06 only, $t_{P(OUT)1}$ maximum test limit under TABLE I and TABLE III is 168 ns at -55°C and +125°C.

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated may be high ≥ 2.4 V, low ≤ 0.4 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D Test no.	1 A_1	2 A_2	3 B_1	4 B_2	5 Clear	6 $\overline{Q}$	7 GND	8 Q	9 R_I	10 NC	11 C_X	12 NC	13 R_XC_X	14 V_{CC}
1 Tc =+25°C	V_{OL}	3007	1				0.8 V	2.0 V		GND	16 mA	4.5 V					4.5 V
		"	2	0.8 V		2.0 V	"	"	16 mA	"		GND		GND			"
	V_{OH}	3006	3	0.8 V		2.0 V	"	"		"	-.8 mA	GND		GND			"
		"	4				"	"	-.8 mA	"		4.5 V					"
	V_{IC}		5	-12 mA						"							"
			6		-12 mA					"							"
			7			-12 mA				"							"
			8				-12 mA			"							"
			9					-12 mA		"							"
	I_{IL1}	3009	10	0.4 V	5.5 V					"							5.5 V
			11	5.5 V	0.4 V					"							"
			12		GND	0.4 V	5.5 V	5.5 V		"							"
			13		"	5.5 V	0.4 V	5.5 V		"							"
	I_{IL2}	3009	14		"	5.5 V	5.5 V	0.4 V		"							5.5 V
	I_{IH1}	3010	15	2.4 V	"					"							"
			16	GND	2.4 V					"							"
			17	5.5 V	5.5 V	2.4 V	GND	GND		"							"
			18	"	5.5 V	GND	2.4 V	GND		"							"
	I_{IH2}	"	19	"	GND					"							"
		"	20	GND	5.5 V					"							"
		"	21	5.5 V	"	5.5 V	GND	GND		"							"
		"	22	"	"	GND	5.5 V	GND		"							"
	I_{IH3}	"	23	"	"	GND	GND	2.4 V		"							"
	I_{IH4}	"	24	"	"	GND	"	5.5 V		"							"
	I_{OS}	3011	25	GND		5.5 V	GND	"		"	GND	GND		GND			"
	"	"	26				"	"	GND	"		5.5 V					"
	I_{CC1}	3005	27	5.5 V	5.5 V	GND	"	"		"		5.5 V					"
	I_{CC2}	"	28	GND	GND	5.5 V	5.5 V	"		"		GND		0.8 V			"
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = 125° C, and $V_{I\,C}$ tests are omitted.																
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55° C, and $V_{I\,C}$ tests are omitted.																
7 Tc =+25°C	Truth table test	3014	29					GND	H	GND	L					1/	5.0 V
		"	30	5.0 V	5.0 V	2/	2/	5.0 V	"	"	"					"	"
		"	31	"	"	5.0 V	2/	"	"	"	"					"	"
		"	32	"	"	2/	5.0 V	"	"	"	"					"	"
		"	33	GND	3/	5.0 V	"	"	"	"	"					"	"
		"	34	3/	GND	5.0 V	"	"	"	"	"					"	"
		"	35	GND		2/	"	"	4/	"	5/					"	"
		"	36	GND		5.0 V	2/	"	"	"	"					"	"
		"	37		GND	2/	5.0 V	"	"	"	"					"	"
		"	38		GND	5.0 V	2/	"	"	"	"					"	"
		"	39	5.0 V	3/	"	5.0 V	"	"	"	"					"	"
		"	40	3/	5.0 V	"	"	"	"	"	"					"	"
		"	41	3/	3/	"	"	"	"	"	"					"	"
8	Repeat subgroup 7 at T_C = +125°C and T_C = -55°C.																

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 – Continued.
Terminal conditions (pins not designated may be high ≥ 2.4 V, low ≤ 0.4 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D Test no.	1 A_1	2 A_2	3 B_1	4 B_2	5 Clear	6 $\overline{Q}$	7 GND	8 Q	9 R_I	10 NC	11 C_X	12 NC	13 R_XC_X	14 V_{CC}
9	t_{PLH1}	3003	42	IN	5.0 V	5.0 V	5.0 V	5.0 V		GND	OUT			7/		7/ 8/	5.0 V
Tc = +25°C	t_{PLH2}	(Fig. 6)	43	OUT	GND	IN	"	5.0 V		"	OUT			"		"	"
	t_{PLH3}	"	44	9/	5.0 V	5.0 V	"	IN	OUT	"				"		"	"
	t_{PHL1}	"	45	IN	5.0 V	5.0 V	"	5.0 V	OUT	"				"		"	"
	t_{PHL2}	"	46	OUT	GND	IN	"	5.0 V	OUT	"				"		"	"
	t_{PHL3}	"	47	9/	5.0 V	5.0 V	"	IN		"	OUT			"		"	"
	$t_{W(MIN)}$ 11/	"	48	IN	"	"	"	5.0 V		"	"					1/	"
	$t_{W(MIN)}$ 12/	"	49	IN	"	"	"	"		"	"			10/		10/ 1/	"
	t_W	"	50	GND	GND	IN	"	"		"	"			7/		7/ 8/	"
10	t_{PLH1}	3003	51	IN	5.0 V	5.0 V	5.0 V	"		GND	"			7/		7/ 8/	5.0 V
Tc = +125°C	t_{PLH2}	(Fig. 6)	52	GND	GND	IN	"	"		"	"			"		"	"
	t_{PLH3}	"	53	9/	5.0 V	5.0 V	"	IN	OUT	"	"			"		"	"
	t_{PHL1}	"	54	IN	5.0 V	5.0 V	"	5.0 V	OUT	"				"		"	"
	t_{PHL2}	"	55	GND	GND	IN	"	5.0 V	OUT	"				"		"	"
	t_{PHL3}	"	56	9/	5.0 V	5.0 V	"	IN		"	OUT			"		"	"
	$t_{W(MIN)}$ 11/	"	57	IN	"	"	"	5.0 V		"	"					1/	"
	$t_{W(MIN)}$ 12/	"	58	IN	"	"	"	"		"	"			10/		10/ 1/	"
	t_W	"	59	GND	GND	IN	"	"		"	"			7/		7/ 8/	"
11	Same tests, terminal conditions and limits as for subgroup 10, except T_C = -55°C.																

1/ R_XC_X connected to V_{CC} through a 5 kΩ resistor.

2/ In transition from low level to high level.

3/ In transition from high level to low level

4/ One low logic level pulse.

5/ One high logic level pulse

6/ Output voltages fro subgroups 7 and 8: H > 1.5 V, L < 1.5 V.

7/ C_X connected to R_XC_X through an 1,000 pF capacitor.

8/ R_XC_X connected to V_{CC} through a 10 kΩ resistor.

9/ Device must be triggered before t_{PHL3} can be measured (see figure 6).

10/ C_X connected to R_XC_X through an 15 pF capacitor which includes stray, probe, and jig capacitor.

11/ This test shall be performed for bench setup only. For class B devices only, this test does not have to be performed at final electricals for subgroup 9. For Group A, subgroup sample size for these tests shall be 15 devices.

12/ This test shall be performed with automatic test equipment only or bench setup. For class B devices only, this test does not have to be performed at final electricals for subgro Group C, subgroups 10 and 11, sample size for these tests shall be 15 devices.

TABLE III. Group A inspection for device type 03.

Terminal conditions (pins not designated may be high ≥ 2.4 V, low ≤ 0.4 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test no.	1 A_1	2 B_1	3 Clear 1	4 $\overline{Q}_1$	5 Q_2	6 C_X2	7 R_XC_X2	8 GND	9 A_2	10 B_2	11 Clear 2	12 $\overline{Q}_2$	13 Q_1	14 C_X1	15 R_XC_X1	V
1	V_{OL}	3007	1	2.0 V	0.8 V	GND					GND					16 mA		1/	4
		"	2	0.8 V	2.0 V	2.0 V	16 mA				"						2/		
Tc =		"	3					16 mA		1/	"	2.0 V	0.8 V	GND					
+25°C		"	4						2/		"	0.8 V	2.0 V	2.0 V	16 mA				
	V_{OH}	3006	5	2.0 V	0.8 V	GND	-.8 mA				GND							1/	4
		"	6	0.8 V	2.0 V	2.0 V					"					-.8 mA	2/		
		"	7							1/	"	2.0 V	0.8 V	GND	-.8 mA				
		"	8					-.8 mA	2/		"	0.8 V	2.0 V	2.0 V					
	V_{IC}		9	-12 mA							"								
			10		-12 mA						"								
			11			-12 mA					"								
			12								"	-12 mA							
			13								"		-12 mA						
			14								"			-12 mA					
	I_{IL1}	3009	15	0.4 V							"								5
		"	16	GND	0.4 V	5.5 V					"								
		"	17								"	0.4 V							
		"	18								"	GND	0.4 V	5.5 V					
	I_{IL2}	"	19	GND	5.5 V	0.4 V					"								
		"	20								"	GND	5.5 V	0.4 V					
	I_{IH1}	3010	21	2.4 V							"								
		"	22	5.5 V	2.4 V	GND					"								
		"	23								"	2.4 V							
		"	24								"	5.5 V	2.4 V	GND					
	I_{IH2}	"	25	5.5 V							"								
		"	26	5.5 V	5.5 V	GND					"								
		"	27								"	5.5 V							
		"	28								"	5.5 V	5.5 V	GND					
	I_{IH3}	"	29	5.5 V	GND	2.4 V					"								
		"	30								"	5.5 V	GND	2.4 V					
	I_{IH4}	"	31	5.5 V	GND	5.5 V					"								
		"	32								"	5.5 V	GND	5.5 V					
	I_{OS}	3011	33	GND	4/	5.5 V					"					GND	2/		
		"	34	GND	GND	GND	GND				"							1/	
		"	35					GND	2/		"	GND	4/	5.5 V					
		"	36							1/	"	GND	GND	GND	GND				
	I_{CC1}	3005	37	2.4 V	GND	2.4 V				1/	"	2.4 V	GND	2.4 V				1/	
	I_{CC2}	3005	38	2.4 V	GND	2.4 V			2/		"	2.4 V	GND	2.4 V			2/		
2	Same	Same tests, terminal conditions and limits as for subgroup 1, except 1, except T_C = +125°C and V_{IC} tests are omitted.																	
3	Same	Same tests, terminal conditions and limits as for subgroup 1, except 1, except T_C = -55°C and V_{IC} tests are omitted.																	
7	Truth	3014	39			GND	H	L		1/	GND			GND	H	L		1/	5
	table	"	40	5.0 v	4/	5.0 V	H	L		"	"	5.0 V	4/	5.0 V	H	L		"	
Tc =	test	"	41	5/	GND	"	H	L		"	"	5/	GND	"	H	L		"	
+25°C		"	42	GND	4/	"	6/	8/		"	"	GND	4/	"	6/	8/		"	
		"	43	5/	5.0 V	"	6/	8/		"	"	5/	5.0	"	6/	8/		"	

See footnotes at end of table.

TABLE III. Group A inspection for device type 03 – Continued.

Terminal conditions (pins not designated may be high ≥ 2.4 V, low ≤ 0.4 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test no.	1 A_1	2 B_1	3 Clear 1	4 $\overline{Q}_1$	5 Q_2	6 C_X2	7 R_XC_X2	8 GND	9 A_2	10 B_2	11 Clear 2	12 $\overline{Q}_2$	13 Q_1	14 C_X1	15 R_XC_X1	V
8	Repeat subgroup 7 at T_C = +125°C and T_C = -55°C.																		
9	t_{PLH1}	3003 (Fig. 7)	44	IN	5.0 V	5.0 V					GND					OUT	9/	9/ 10/	5
Tc = +25°C	"	"	45					OUT	9/	9/ 10/	"	IN	5.0 V	5.0 V					
	t_{PLH2}	"	46	GND	IN	5.0 V					"					OUT	9/	9/ 10/	
	"	"	47					OUT	9/	9/ 10/	"	GND	IN	5.0 V					
	t_{PLH3}	"	48	11/	5.0 V	IN	OUT				"						9/	9/ 10/	
	"	"	49						9/	9/ 10/	"	11/	5.0 V	IN	OUT				
	t_{PHL1}	"	50	IN	5.0 V	5.0 V	OUT				"						9/	9/ 10/	
	"	"	51						9/	9/ 10/	"	IN	5.0 V	5.0 V	OUT				
	t_{PHL2}	"	52	GND	IN	5.0 V	OUT				"						9/	9/ 10/	
	"	"	53						9/	9/ 10/	"	GND	IN	5.0 V	OUT				
	t_{PHL3}	"	54	11/	5.0 V	IN					"					OUT	9/	9/ 10/	
	"	"	55					OUT	9/	9/ 10/	"	11/	5.0 V	IN					
	$t_{W(MIN)}$ 13/	"	56	IN	5.0 V	5.0 V					"					OUT		1/	
	"		57					OUT		1/	"	IN	5.0 V	5.0 V					
	$t_{W(MIN)}$ 14/	"	58	IN	5.0 V	5.0 V					"					OUT	12/	1/	
	"		59					OUT	12/	1/	"	IN	5.0 V	5.0 V					
	t_W	"	60	GND	IN	5.0 V					"					OUT	9/	9/ 10/	
	"	"	61					OUT	9/	9/ 10/	"	GND	IN	5.0 V					
10	t_{PLH1}	"	62	IN	5.0 V	5.0 V					"					OUT	9/	9/ 10/	5
	"	"	63					OUT	9/	9/ 10/	"	IN	5.0 V	5.0 V					
Tc = +125°C	t_{PLH2}	"	64	GND	IN	5.0 V					"					OUT	9/	9/ 10/	
	"	"	65					OUT	9/	9/ 10/	"	GND	IN	5.0 V					
	t_{PLH3}	"	66	11/	5.0 V	IN	OUT				"						9/	9/ 10/	
	"	"	67						9/	9/ 10/	"	11/	5.0 V	IN	OUT				
	t_{PHL1}	"	68	IN	5.0 V	5.0 V	OUT				"						9/	9/ 10/	
	"	"	69						9/	9/ 10/	"	IN	5.0 V	5.0 V	OUT				
	t_{PHL2}	"	70	GND	IN	5.0 V	OUT				"						9/	9/ 10/	
	"	"	71						9/	9/ 10/	"	GND	IN	5.0 V	OUT				
	t_{PHL3}	"	72	11/	5.0 V	IN					"					OUT	9/	9/ 10/	
	"	"	73					OUT	9/	9/ 10/	"	11/	5.0 V	IN					

See footnotes at end of table.

TABLE III. Group A inspection for device type 03 – Continued.
Terminal conditions (pins not designated may be high ≥ 2.4 V, low ≤ 0.4 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
			Test no.	A_1	B_1	Clear 1	$\overline{Q}_1$	Q_2	C_X2	R_XC_X2	GND	A_2	B_2	Clear 2	$\overline{Q}_2$	Q_1	C_X1	R_XC_X1	V
10	$t_{W(MIN)}$ 13/	3003 (Fig. 7)	74	IN	5.0 V	5.0 V					GND					OUT		1/	5
Tc =	$t_{W(MIN)}$ 13/	"	75					OUT		1/	"	IN	5.0 V	5.0 V					
+125°C	$t_{W(MIN)}$ 14/	"	76	IN	5.0 V	5.0 V					"					OUT	11/	1/	
	$t_{W(MIN)}$ 14/	"	77					OUT	11/	1/	"	IN	5.0 V	5.0 V					
	t_W	"	78	GND	IN	5.0 V					"					OUT	9/	9/ 10/	
	"	"	79					OUT	9/	9/ 10/	"	GND	IN	5.0 V					
11	Same tests, terminal conditions and limits as subgroup 10, except T_C = -55°C.																		

1/ R_XC_X connected to V_{CC} through a 5 kΩ resistor.
2/ C_X connected to GND or 0.8 V.
3/ For schematic circuits A, B, and C, the minimum and maximum limits shall be –1.4 mA and –0.2 mA, respectively. For schematic circuit D, the minimum and maximum limits shall be
4/ In transition from low level to high level.
5/ In transition from high level to low level.
6/ One low logic level pulse. At manufacturer's option, this may be verified in subgroups 9, 10, 11.
7/ Output voltages for subgroups 7 and 8: H > 1.5 V, L > 1.5 V.
8/ One high logic level pulse. At manufacturer's option, this may be verified in subgroups 9, 10, 11.
9/ C_X connected to R_XC_X through a 1,000 pF capacitor.
10/ R_XC_X connected to V_{CC} through a 10 kΩ resistor.
11/ Device must be triggered before t_{PLH3} and t_{PHL3} can be measured (see figure 7).
12/ C_X connected to R_XC_X through a 15 pF capacitor which includes stray, probe, and jig capacitance.
13/ This test shall be performed for bench setup only.
14/ This test shall be performed for automatic test equipment only.

TABLE III. Group A inspection for device type 04.
Terminal conditions (pins not designated may be high ≥ 2.4 V, low ≤ 0.4 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D Test no.	1 A_1	2 A_2	3 B_1	4 B_2	5 NC	6 $\overline{Q}$	7 GND	8 Q	9 NC	10 NC	11 C_X	12 NC	13 R_XC_X	14 V_{CC}
1	V_{OL}	3007	1				0.8 V			GND	10 mA					1/	4.5 V
Tc =+25°C		"	2		0.8 V	2.0 V	2.0 V		10 mA	"				GND		1/	"
	V_{OH}	3006	3		0.8 V	2.0 V	2.0 V			"	-.72 mA			GND		1/	"
		"	4				0.8 V		-.72 mA	"						1/	"
	V_{IC}		5	-12 mA						"							"
			6		-12 mA					"							"
			7			-12 mA				"							"
			8				-12 mA			"							"
	I_{IL1}	3009	9	0.4 V	5.5 V					"							5.5 V
		"	10	5.5 V	0.4 V					"							"
		"	11		GND	0.4 V	5.5 V			"							"
		"	12		GND	5.5 V	0.4 V			"							"
	I_{IH1}	3010	13	2.4 V	"					"							"
		"	14	GND	2.4 V					"							"
		"	15	5.5 V	5.5 V	2.4 V	GND			"							"
		"	16	"	5.5 V	GND	2.4 V			"							"
	I_{IH2}	"	17	5.5 V	GND					"							"
		"	18	GND	5.5 V					"							"
		"	19	5.5 V	"	5.5 V	GND			"							"
		"	20	"	"	GND	5.5 V			"							"
	I_{OS}	3011	21		GND	5.5 V	5.5 V		GND	"						1/	"
	"	"	22			"	GND			"	GND			GND		1/	"
	I_{CC}	3005	23	GND	GND	5.5 V	5.5 V			"						1/	"
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = 125° C, and $V_{I\,C}$ tests are omitted.																
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55° C, and $V_{I\,C}$ tests are omitted.																
7	Truth	3014	24	5.0 V	5.0 V				H	GND	L					2/	5.0 V
Tc =+25°C	table	"	25			GND			"	"	"					"	"
	test	"	26				GND		"	"	"					"	"
		"	27	GND		5.0 V	5.0 V		"	"	"					"	"
		"	28		GND	5.0 V	5.0 V		"	"	"					"	"
		"	29	GND		3/	5.0 V		4/	"	5/					"	"
		"	30	GND		5.0 V	3/		"	"	"					"	"
		"	31		GND	3/	5.0 V		"	"	"					"	"
		"	32		GND	5.0 V	3/		"	"	"					"	"
		"	33	5.0 V	7/		5.0 V		"	"	"					"	"
		"	34	7/	5.0 V		5.0 V		"	"	"					"	"
		"	35	7/	7/		5.0 V		"	"	"					"	"
8	Repeat subgroup 7 at T_C = +125°C and T_C = -55°C.																
9	t_{PLH1}	3003	36	IN	5.0 V	5.0 V	5.0 V			GND	OUT					2/	5.0 V
Tc =+25°C	t_{PLH2}	(Fig. 8)	37	GND	GND	IN	"			"	OUT					"	"
	t_{PHL1}	"	38	IN	5.0 V	5.0 V	"		OUT	"						"	"
	t_{PHL2}	"	39	GND	GND	IN	"		OUT	"						"	"

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04 – Continued.
Terminal conditions (pins not designated may be high ≥ 2.4 V, low ≤ 0.4 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D Test no.	1 A_1	2 A_2	3 B_1	4 B_2	5 NC	6 $\overline{Q}$	7 GND	8 Q	9 NC	10 NC	11 C_X	12 NC	13 R_XC_X	14 V_{CC}
9 Tc =+25°C	$t_{W(MIN)}$ 8/	3003 (Fig. 8)	40	IN	5.0 V	5.0 V	5.0 V			GND	OUT					2/	5.0 V
	$t_{W(MIN)}$ 9/	"	41	IN	"	"	"			"	"			10/		2/	"
	t_W	"	42	7/	"	"	"			"	"			11/		1/ 11/	"
10 Tc = +125°C	t_{PLH1}	"	43	IN	5.0 V	5.0 V	"			"	"					2/	"
	t_{PLH2}	"	44	GND	GND	IN	"			"	"					"	"
	t_{PHL1}	"	45	IN	GND	IN	"		OUT	"						"	"
	t_{PHL2}	"	46	GND	GND	IN	"		OUT	"						"	"
	$t_{W(MIN)}$ 8/	"	47	IN	5.0 V	5.0 V	"			"	OUT					"	"
	$t_{W(MIN)}$ 9/	"	48	IN	"	"	"			"	"			10/		"	"
	t_W	"	49	7/	"	"	"			"	"			11/		11/ 1/	"
11	Same tests, terminal conditions and limits as for subgroup 10, except T_C = -55°C.																

1/ R_XC_X connected to V_{CC} through a 10 kΩ resistor.

2/ R_XC_X connected to V_{CC} through a 5 kΩ resistor.

3/ In transition from low level to high level.

4/ One low logic level pulse.

5/ One high logic level pulse

6/ Output voltages for subgroups 7 and 8: H > 1.5 V, L < 1.5 V.

7/ In transition from high level to low level.

8/ This test shall be performed for bench setup only.

9/ This test shall be performed for automatic test equipment only.

10/ C_X connected to R_XC_X through an 15 pF capacitor which includes stray, probe, and jig capacitor.

11/ C_X connected to R_XC_X through an 1,000 pF capacitor.

TABLE III. Group A inspection for device type 05.

Terminal conditions (pins not designated may be high ≥ 2.4 V, low ≤ 0.4 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test no.	1 C_X1	2 R_XC_X1	3 Clear 1	4 B_1	5 A_1	6 Q_1	7 $\overline{Q}_1$	8 GND	9 $\overline{Q}_2$	10 Q_2	11 A_2	12 B_2	13 Clear 2	14 R_XC_X2	15 C_X2	16
1	V_{OL}	3007	1			0.8 V			10 mA		GND								4.
		"	2		0.9 V	2.0 V	GND	1/		10 mA	"								
Tc =		"	3								"		10 mA	1/		0.8 V			
+25°C		"	4								"	10 mA			GND	2.0 V	0.9 V		
	V_{OH}	3006	5		0.9 V	2.0 V	GND	1/	-.96 mA		"								
		"	6			0.8 V				-.96 mA	"								
		"	7								"		-.96 mA	1/	GND	2.0 V	0.9 V		
		"	8								"	-.96 mA				0.8 V			
	V_{IC}		9			-12 mA					"								
			10				-12 mA				"								
			11					-12 mA			"								
			12								"				-12 mA				
			13								"					-12 mA			
			14								"			-12 mA					
	I_{IL}	3009	15			0.4 V					"								5.
		"	16				0.4 V				"								
		"	17					0.4 V			"								
		"	18								"					0.4 V			
		"	19								"				0.4 V				
		"	20								"			0.4 V					
	I_{IH1}	3010	21			2.4 V					"								
		"	22				2.4 V				"								
		"	23					2.4 V			"								
		"	24								"				2.4 V				
		"	25								"			2.4 V		2.4 V			
		"	26								"								
	I_{IH2}	"	27			5.5 V					"								
		"	28				5.5 V				"								
		"	29					5.5 V			"								
		"	30								"				5.5 V				
		"	31								"			5.5 V					
		"	32								"								
	I_{OS}	3011	33		0.9 V	2.0 V	GND	1/	0.5 V		"								6.
		"	34			0.8 V				0.5 V	"								
		"	35								"		0.5 V	1/	GND	2.0 V	0.9 V		
		"	36								"	0.5 V				0.8 V			
	I_{CC}	3005	37	GND	GND		GND	GND			"			GND	GND		GND	GND	5.
	I_{CC}	3005	38								"								5.
2	Same tests, terminal conditions and limits as for subgroup 1, except T_C = +125° C, and V_{IC} tests are omitted.																		
3	Same tests, terminal conditions and limits as for subgroup 1, except T_C = -55° C, and V_{IC} tests are omitted.																		
7	Truth	3014	39		2/	GND			L	H	GND	H	L			GND	2/		5.
	table	"	40		"	5.0 V	3/	GND	L	H	"	H	L	GND	3/	5.0 V	"		
Tc =	test	"	41		"	"	5.0 V	1/	L	H	"	H	L	5.0 V	5.0 V	"	"		
+25°C		"	42		"	"	3/	5.0 V	4/	5/	"	5/	4/	1/	3/	"	"		
		"	43		"	"	GND	1/	4/	5/	"	5/	4/	1/	GND	"	"		

See footnotes at end of table.

TABLE III. Group A inspection for device type 05 – Continued.

Terminal conditions (pins not designated may be high ≥ 2.4 V, low ≤ 0.4 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test no.	1 C_X1	2 R_XC_X1	3 Clear 1	4 B_1	5 A_1	6 Q_1	7 $\overline{Q}_1$	8 GND	9 $\overline{Q}_2$	10 Q_2	11 A_2	12 B_2	13 Clear 2	14 R_XC_X2	15 C_X2	
8	Repeat subgroup 7 at T_C = +125°C and T_C = -55°C.																		
9	t_{PLH1}	3003 (Fig. 7)	44		2/	5.0 V	GND	IN	OUT		GND								5
	"	"	45								"		OUT	IN	GND	5.0 V	2/		
Tc = +25°C	t_{PLH2}	"	46		2/	5.0 V	IN	5.0 V	OUT		"								
	"	"	47								"		OUT	5.0 V	IN	5.0 V	2/		
	t_{PLH3}	"	48		2/	IN	GND	7/		OUT	"								
	"	"	49								"	OUT		7/	GND	IN	2/		
	t_{PHL1}	"	50		2/	5.0 V	GND	IN		OUT	"								
	"	"	51								"	OUT		IN	GND	5.0 V	2/		
	t_{PHL2}	"	52		2/	5.0 V	IN	5.0 V		OUT	"								
	"	"	53								"	OUT		5.0 V	IN	5.0 V	2/		
	t_{PHL3}	"	54		2/	IN	GND	7/	OUT		"								
	"	"	55								"		OUT	7/	GND	IN	2/		
	$t_{W(MIN)}$ 8/	"	56		2/	5.0 V	GND	IN	OUT		"								
	"		57								"		OUT	IN	GND	5.0 V	2/		
	$t_{W(MIN)}$ 9/	"	58	10/	2/	5.0 V	GND	IN	OUT		"								
	"		59								"		OUT	IN	GND	5.0 V	2/	10/	
	t_W	"	60	11/	11/ 12/	5.0 V	GND	1/	OUT		"								
	"	"	61								"		OUT	1/	GND	5.0 V	11/ 12/	11/	
10	t_{PLH1}	"	62		2/	5.0 V	GND	IN	OUT		"								
	"	"	63								"		OUT	IN	GND	5.0 V	2/		
Tc = +125°C	t_{PLH2}	"	64		2/	5.0 V	IN	5.0 V	OUT		"								
	"	"	65								"		OUT	5.0 V	IN	5.0 V	2/		
	t_{PLH3}	"	66		2/	IN	GND	7/		OUT	"								
	"	"	67								"	OUT		7/	GND	IN	2/		
	t_{PHL1}	"	68		2/	5.0 V	GND	IN		OUT	"								
	"	"	69								"	OUT		IN	GND	5.0 V	2/		
	t_{PHL2}	"	70		2/	5.0 V	IN	5.0 V		OUT	"								
	"	"	71								"	OUT		5.0 V	IN	5.0 V	2/		
	t_{PHL3}	"	72		2/	IN	GND	1/	OUT		"								
	"	"	73								"		OUT	1/	GND	IN	2/		
	"																		

See footnotes at end of table.

TABLE III. Group A inspection for device type 05 – Continued.

Terminal conditions (pins not designated may be high ≥ 2.4 V, low ≤ 0.4 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E, F Test no.	1 C_X1	2 R_XC_X1	3 Clear 1	4 B_1	5 A_1	6 Q_1	7 $\overline{Q}_1$	8 GND	9 $\overline{Q}_2$	10 Q_2	11 A_2	12 B_2	13 Clear 2	14 R_XC_X2	15 C_X2	
10	$t_{W(MIN)}$ 8/	3003 (Fig. 7)	74		2/	5.0 V	GND	IN	OUT		GND								5
Tc =	$t_{W(MIN)}$ 8/	"	75								"		OUT	IN	GND	5.0 V	9/		
+125°C	$t_{W(MIN)}$ 9/	"	76	10/	2/	5.0 V	GND	IN	OUT		"								
	$t_{W(MIN)}$ 9/	"	77								"		OUT	IN	GND	5.0 V	2/	10/	
	t_W	"	78	11/	11/ 12/	5.0 V	GND	1/	OUT		"								
	"	"	79								"		OUT	1/	GND	5.0 V	11/ 12/	11/	
11	Same tests, terminal conditions and limits as subgroup 10, except T_C = -55°C, and t_W max limit = 4.10 μs.																		

1/ In transition from high level to low level.
2/ R_XC_X connected to V_{CC} through a 5 kΩ resistor.
3/ In transition from low level to high level.
4/ One high logic level pulse.
5/ One low logic level pulse.
6/ Output voltages for subgroups 7 and 8: H > 1.5 V, L > 1.5 V.
7/ Device must be triggered before t_{PLH3} and t_{PHL3} can be measured (see figure 9).
8/ This test shall be performed for bench setup only.
9/ This test shall be performed for automatic test equipment only.
10/ C_X connected to R_XC_X through a 15 pF capacitor which includes stray, probe, and jig capacitance.
11/ C_X connected to R_XC_X through a 1,000 pF capacitor.
12/ R_XC_X connected to V_{CC} through a 10 kΩ resistor.

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End point electrical parameters shall be as specified in table II herein.

b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows.

4.5.1 Voltage and current. All voltage values given are referenced to the microcircuit ground terminals. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service, or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. PIN and compliance identifier, if applicable (see 1.2).

c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

d. Requirements for certificate of compliance, if applicable.

e. Requirements for notification of change of product or process to acquiring activity in addition to notification of the qualifying activity, if applicable.

f. Requirements for failure analysis (including required test condition of MIL-STD-883, method 5003), corrective action and reporting of results, if applicable.

g. Requirements for product assurance options.

h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

i. Requirements for "JAN" marking.

j. Packaging requirements (see 5.1).

6.3 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43218-3990.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-STD-1331, and as follows:

GND -------- Ground zero voltage potential.
I_{IN} ---------- Current flowing into an input terminal
V_{IN} --------- Voltage level at an input terminal
V_{IC} --------- Input clamp voltage

6.6 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry type
01	54121
02	54122
03	54123
04	9601
05	9602
06	54121 1/

1/ For device type 06, the $t_{P(OUT)1}$ maximum test limit under TABLE I and TABLE III is 168 ns at -55°C and +125°C.

6.8 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
Army – CR
Navy - EC
Air Force - 11
DLA – CC

Preparing activity:
DLA - CC

Project 5962-2092

Review activities:
Army - MI, SM
Navy - AS, CG, SH, TD
Air Force – 03, 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.

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