INCH-POUND
MIL-M-38510/208F
21 August 2013
SUPERSEDING
MIL-M-38510/208E
12 October 2010

MILITARY SPECIFICATION

MICROCIRCUIT, DIGITAL, 4096-BIT SCHOTTKY, BIPOLAR, PROGRAMMABLE READ-ONLY MEMORY (PROM), MONOLITHIC SILICON

Inactive for new design after 24 July 1995

This specification is approved for use by all Departmentsand Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, programmable read-only memory (PROM) microcircuits which employ thin film nichrome (NiCr) resistors, titanium-tungsten (TiW), or zapped vertical emitter (ZVE) as the fusible link or programming element. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are as follows:

Device type	Circuit
01	512 word/8 bits per word PROM with uncommitted collector
02	512 word/8 bits per word PROM with active pull-up and a choice third high-impedance state output
03	512 word/8 bits per word PROM with active pull-up and a third high-impedance state output
04	512 word/8 bits per word PROM with uncommitted collector
05	512 word/8 bits per word PROM with active pull-up and a third high-impedance state output

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
X	See figure 1	24	Flat pack
Y	See figure 2	20	Dual-in-line
Z	CQCC1-N24	24	Square leadless chip carrier

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DLA LAND AND MARITIME-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to Memory@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil

AMSC N/A FSC 5962

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -10 mA to +5.5 V dc
Storage temperature range	-65° to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction to case (θ_{JC}) 1/:	
Cases J, K, and Y	30°C/W
Case X and Z	36° C/W
Output voltage applied	-0.5 V dc dc to +V_{CC}
Output sink current	100 mA
Maximum power dissipation (P_D) 2/	1.02 W
Maximum, junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high-level input voltage	2.0 V dc
Maximum low-level input voltage	0.8 V dc
Normalized fanout (each output)	8 mA 3/
Case operating temperature range (T_C)	-55 °C to +125 °C

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and Standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outline

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Heat sinking is recommended to reduce the junction temperature.
2/ Must withstand the added P_D due to short circuit test (e.g. I_{OS}).
3/ 16 mA for circuit F devices.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figures 3.

3.3.2 Truth table

3.3.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 4. When required in groups A, B, or C (see 4.4), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.3.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3.3.3 Logic diagram. The logic diagram shall be as specified on figure 5.

3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table II, and where applicable, the altered item drawing. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.8 Processing options. Since the PROM is an unprogrammed memory capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.8.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.3.2.1, table II, and table III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.8.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.9 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see Appendix A MIL-PRF-38535.)

TABLE I. Electrical performance characteristics.

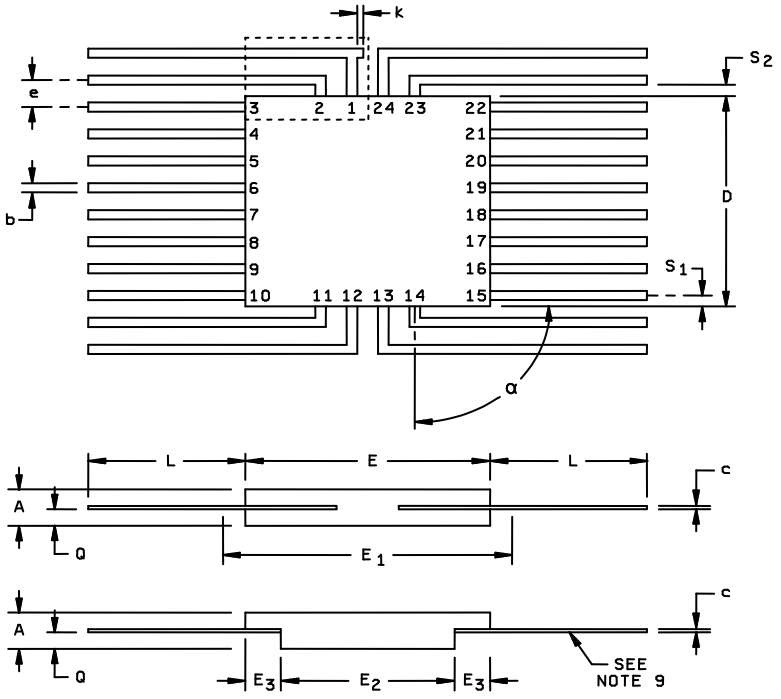
Test	Symbol	Conditions 1/ 2/	Device type	Limits		Unit
				Min	Max	
High-level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2 mA	02,03,05	2.4	---	V
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA 3/	All	---	0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -10 mA, T_C = 25°C	All	---	-1.5	V
Maximum collector cut-off current	I_{CEX}	V_{CC} = 5.5 V, V_O = 5.2 V	01,04	---	100	µA
High-impedance (off-state) output high current	I_{OHZ}	V_{CC} = 5.5 V V_O = 5.2 V	02,03,05	---	100	µA
High-impedance (off-state) output low current	I_{OLZ}	V_{CC} = 5.5 V, V_O = 0.5 V	02,03,05		-100	µA
High-level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	All	---	50	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 4.5 V, special program-ming pin	All	---	100	µA
Low-level input current	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.5 V	All	-1.0	-250	µA
	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 0.5 V, for CE_3 and CE_4	01,02	-1.0	-1000	µA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V, V_O = 0.0 V 4/	02,03,05	-10	-100	mA
Supply current	I_{CC}	V_{CC} = 5.5 V, V_{IN} = 0, out-puts = open	01,02,03	---	185	mA
			04,05	---	155	mA
Propagation delay time, high-to-low level logic, address to output	t_{PHL1}	V_{CC} = 4.5 V and 5.5 V, C_L = 30 pF (see figure 6)	01,02,03	---	90	ns
			04,05	---	80	ns
Propagation delay time, low-to-high level logic, address to output	t_{PLH1}		01,02,03	---	90	ns
			04,05	---	80	ns
Propagation delay time, high-to-low level logic, enable to output	t_{PHL2}	V_{CC} = 4.5 V and 5.5 V, C_L = 30 pF (see figure 6)	01,02,03	---	50	ns
			04,05	---	40	ns
Propagation delay time, low-to-high level logic, enable to output	t_{PLH2}		01,02,03	---	50	ns
			04,05		40	ns

1/ Complete terminal conditions shall be as specified on table III.

2/ For device type 03, the fusing pins FE_1 and FE_2 may be grounded or floating during operation.

3/ I_{OL} = 16 mA for circuit F devices.

4/ Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.



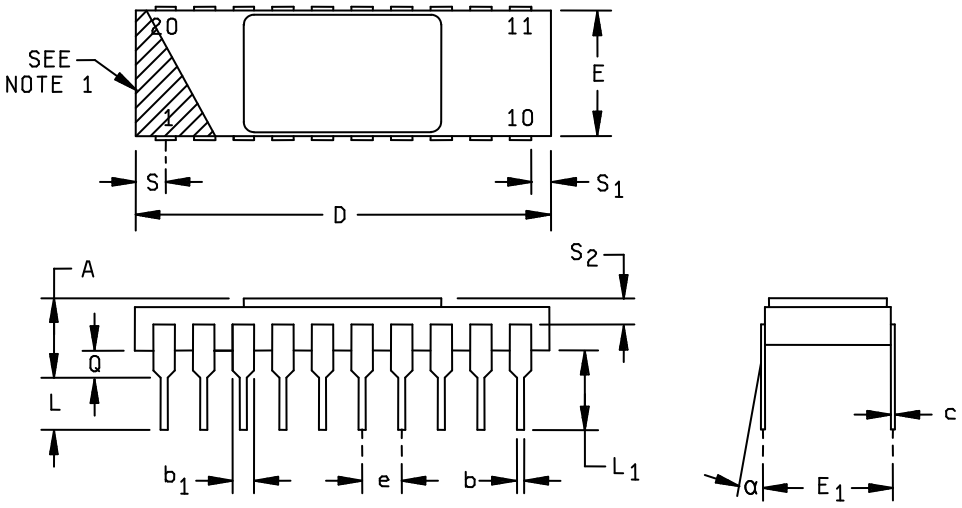
Symbol	Dimension				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	.045	.090	1.14	2.29	
b	.015	.019	.38	.48	5
c	.003	.006	.08	.15	5
D	----	.400	----	10.16	3
E	.340	.385	8.64	9.78	
E_1	----	.400	----	10.16	3
E_2	.125	----	3.18	----	
E_3	.030	----	.76	----	14
e	.050 BSC		1.27 BSC		4, 6
k	.008	.015	.20	.38	10
L	.250	.370	6.35	9.40	
Q	.010	.040	.25	1.02	2
S_1	.005	----	.13	----	7, 8
S_2	.005	---	.13	----	11
α	30°	90°	30°	90°	12, 13

FIGURE 1. Case outline X.

NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic pin spacing is .050 (1.25 mm) between centerlines. Each pin centerline shall be located within ±.005 (0.13 mm) of its exact longitudinal position relative to pins relative to pins 1 and 24.
5. All leads – increase maximum limit by .003 (0.08mm) measured at the center of the flat, when lead finish A is applied.
6. Twenty-two spaces.
7. Applies to all four corners (leads number 3, 10, 15, and 22).
8. Dimension S_1 may be .000 (0.00 mm) if leads number 3, 10, 15, and 22 bend toward the cavity of the package within one lead width from the point of entry of the lead, into the body or if the leads are brazed to the metallized ceramic body (see MIL-STD-1835) .
9. Optional configuration: if this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
10. Optional, see note 1. If a pin one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.
11. Applies to leads number 2, 11, 14, and 23.
12. Lead configuration is optional within dimension E except dimensions b and c apply (see MIL-STD-1835).
13. Applies to lead numbers 1, 2, 11, 12, 13, 14, 23, and 24.
14. Applies to all edges.

FIGURE 1. Case outline X – Continued.



Dimension					
Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	----	.175	----	4.44	
b	.016	.020	.41	.51	11, 8
b_1	.040	.060	1.02	1.52	8, 2
C	.008	.012	.20	.30	11, 8
D	.970	1.010	24.64	25.65	4
E	.280	.300	7.11	7.62	4
E_1	.290	.320	7.37	8.13	7
e	.090	.110	2.29	2.79	5, 9
L	.125	.180	3.18	4.58	
L_1	.150	----	3.81	----	
Q	.020	.060	.51	1.52	3
S	----	.098	----	2.49	6
S_1	.005	----	.13	----	6
S_2	.005	----	.13	----	8
α	0°	15°	0°	15°	

FIGURE 2. Case outline Y.

NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be .020 (.51 mm) for leads number 1, 10, 11, and 20 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (.25 mm) of its exact longitudinal position relative to pins 1 and 20.
6. Applies to all four corners (leads number 1, 10, 11, and 20) (see MIL-STD-1835).
7. Lead center when α is 0°. E_1 shall be measured at the centerline of leads (see MIL-STD-1835).
8. All leads – Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
9. Eighteen spaces.
10. No organic or polymeric materials shall be molded to the bottom of the package.
11. Applies to all leads.

FIGURE 2. Case outline Y – Continued.

Device type	01 and 02	03	04 and 05
Case outline	J, K, X, and Z	J, K, and X	Y
Terminal number	Terminal symbol		
1	A7	A3	A0
2	A6	A4	A1
3	A5	A5	A2
4	A4	A6	A3
5	A3	A7	A4
6	A2	A8	O1
7	A1	O1	O2
8	A0	O2	O3
9	O1	O3	O4
10	O2	O4	GND
11	O3	FE_2	O5
12	GND	GND	O6
13	O4	FE_1	O7
14	O5	O5	O8
15	O6	O6	$\overline{CE}_1$
16	O7	O7	A5
17	O8	O8	A6
18	CE_4	STROBE	A7
19	CE_3	CE_2	A8
20	$\overline{CE}_2$	$\overline{CE}_1$	V_{CC}
21	$\overline{CE}_1$	A0	----
22	NC	A1	----
23	A8	A2	----
24	V_{CC}	V_{CC}	----

NOTE: Case Z: option A with active terminals on plane 1.

FIGURE 3. Terminal connections.

Device types 01 and 02

WORD NO.	ENABLE				ADDRESS									DATA							
	$\overline{CE}_1$	$\overline{CE}_2$	CE_3	CE_4	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8
NA	L	L	L	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	L	L	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	H	L	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	H	L	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	L	H	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	L	H	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	H	H	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	H	H	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	L	L	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	L	L	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	H	L	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	H	L	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	L	H	H	X	X	X	X	X	X	X	X	X	4/	4/	4/	4/	4/	4/	4/	4/
NA	H	L	H	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	H	H	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	H	H	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC

Device type 03

WORD NO.				ADDRESS									DATA							
	$\overline{CE}_1$	CE_2	STROBE	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8
NA	L	L	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	L	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	H	H	X	X	X	X	X	X	X	X	X	4/	4/	4/	4/	4/	4/	4/	4/
NA	H	H	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	H	L	X	X	X	X	X	X	X	X	X		Last data is latched						

Device types 04 and 05

WORD NO.	ENABLE	ADDRESS									DATA							
	$\overline{CE}_1$	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8
NA	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	X	X	X	X	X	X	X	X	X	4/	4/	4/	4/	4/	4/	4/	4/

NOTES:
1. NA = Not applicable.
2. X = Input may be high level, low level, or open circuit.
3. OC = Open circuit (high resistance output).
4. The outputs for an unprogrammed device shall be high for circuits A, B, D, and F, and low for circuit C, G and H.

FIGURE 4. Truth table (unprogrammed).

LOGIC CIRCUIT A
(Device types 01 and 02)

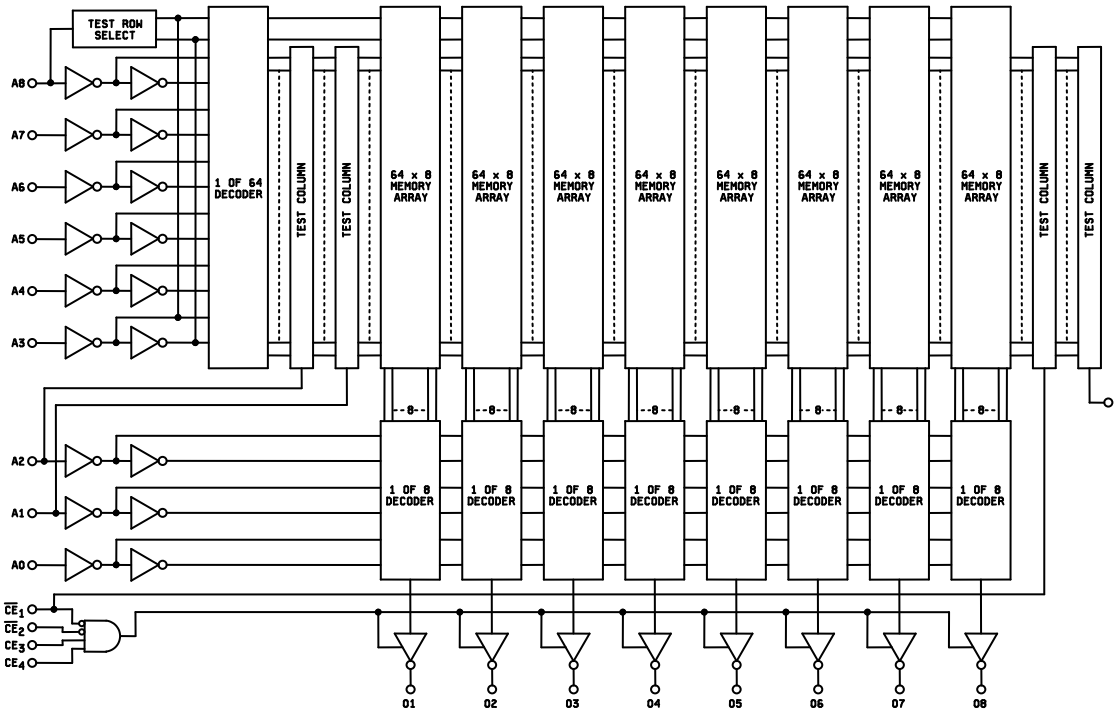


FIGURE 5. Logic diagrams.

LOGIC CIRCUIT B
(Device types 01, 02, 04, & 05) and
LOGIC CIRCUIT F
(Device type 05)

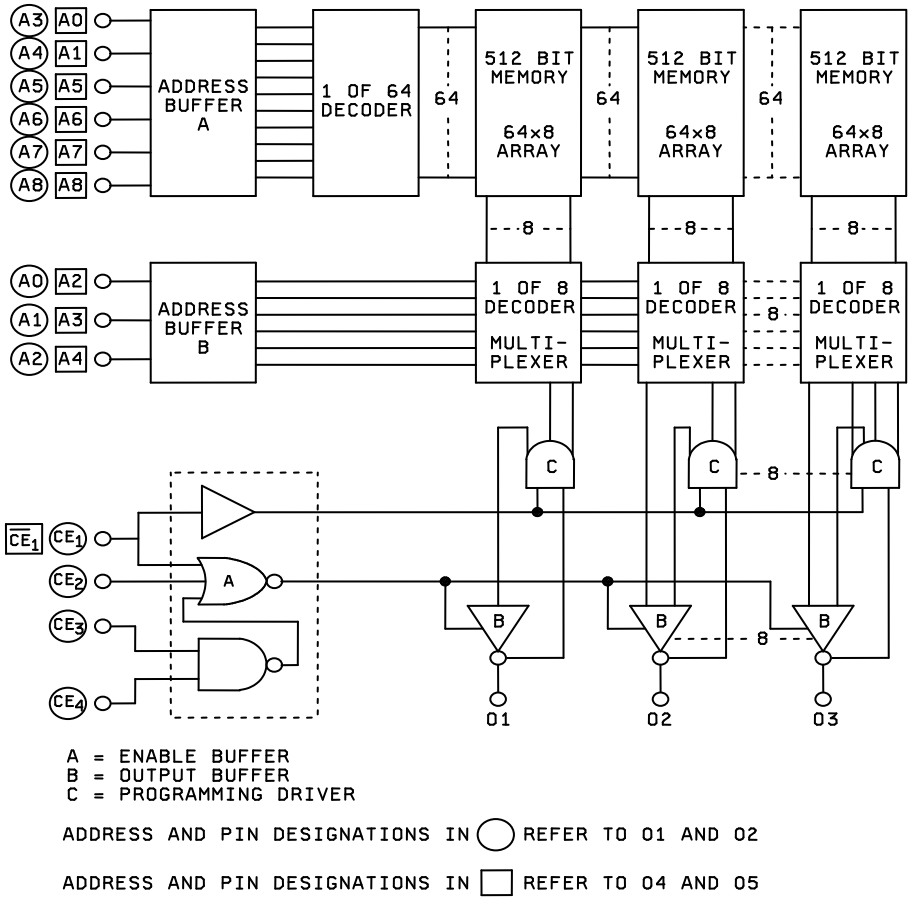


FIGURE 5. Logic diagrams – Continued.

LOGIC CIRCUIT C
(Device types 01 and 02) and
LOGIC CIRCUIT H
(Device type 02)

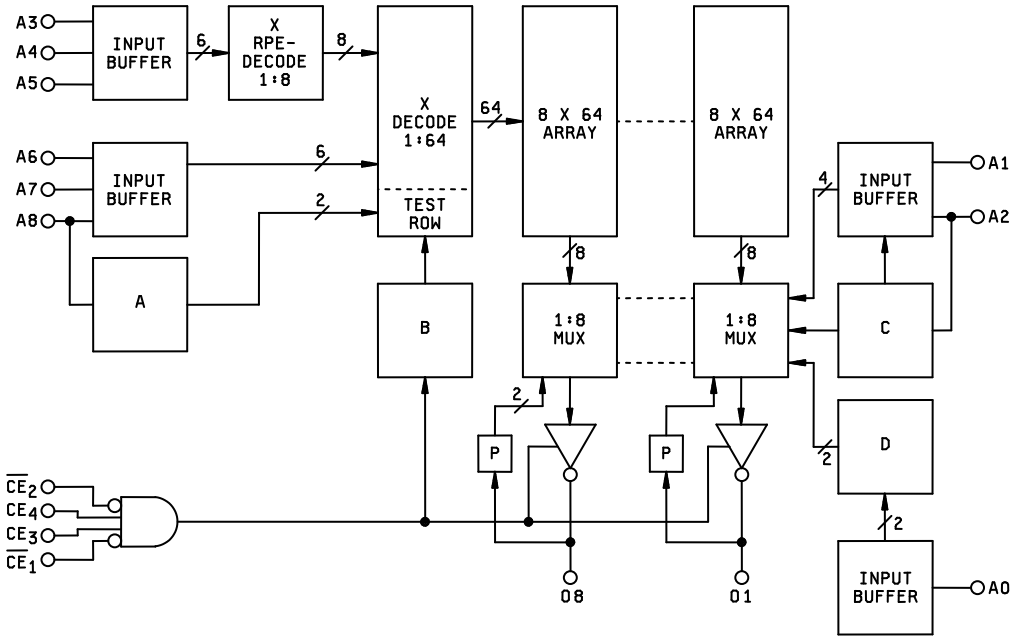


FIGURE 5. Logic diagrams – Continued.

LOGIC CIRCUIT C
(Device type 03)

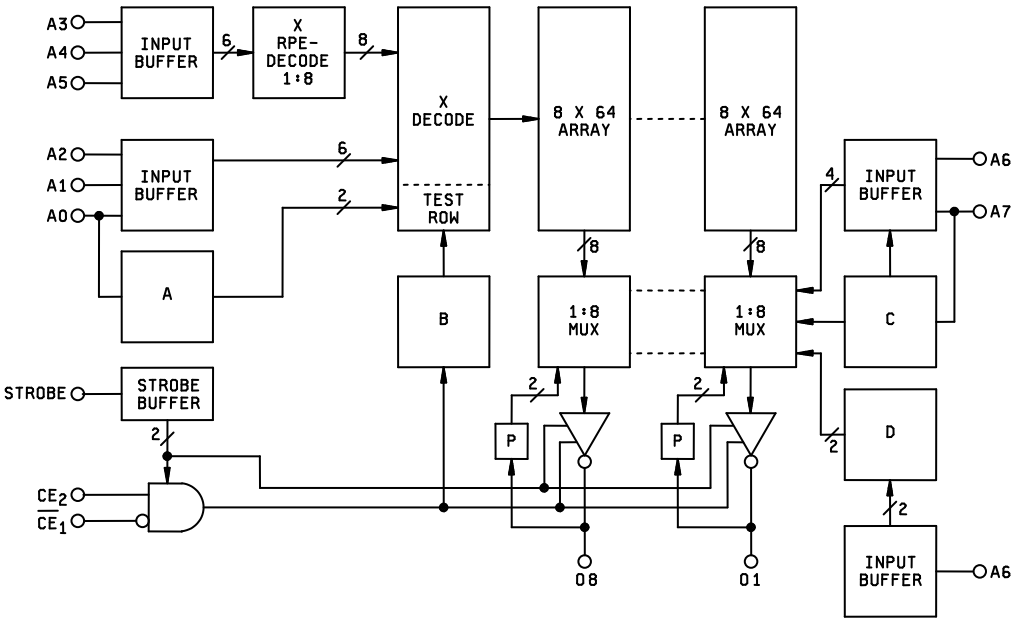


FIGURE 5. Logic diagrams – Continued.

LOGIC CIRCUIT D
(Device types 01 and 02)

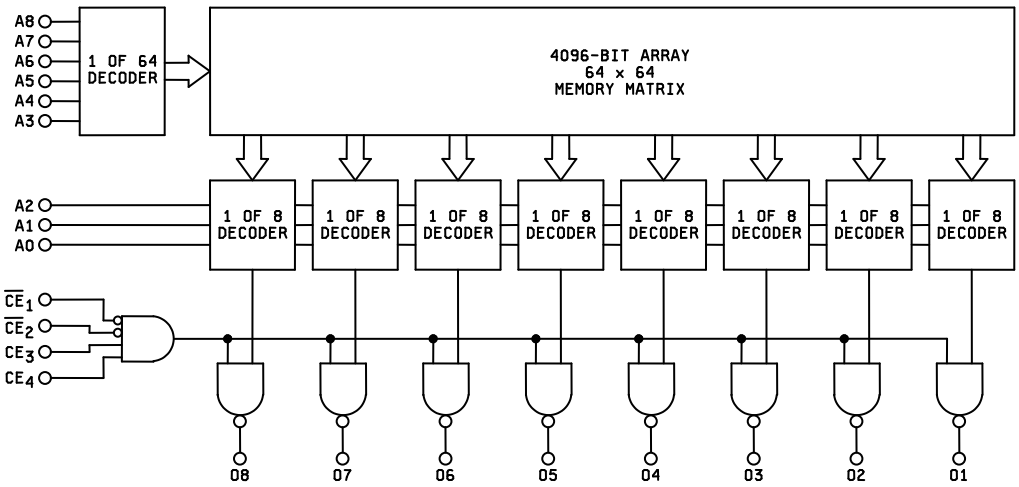


FIGURE 5. Logic diagrams - Continued

LOGIC CIRCUIT G
(Device type 01)

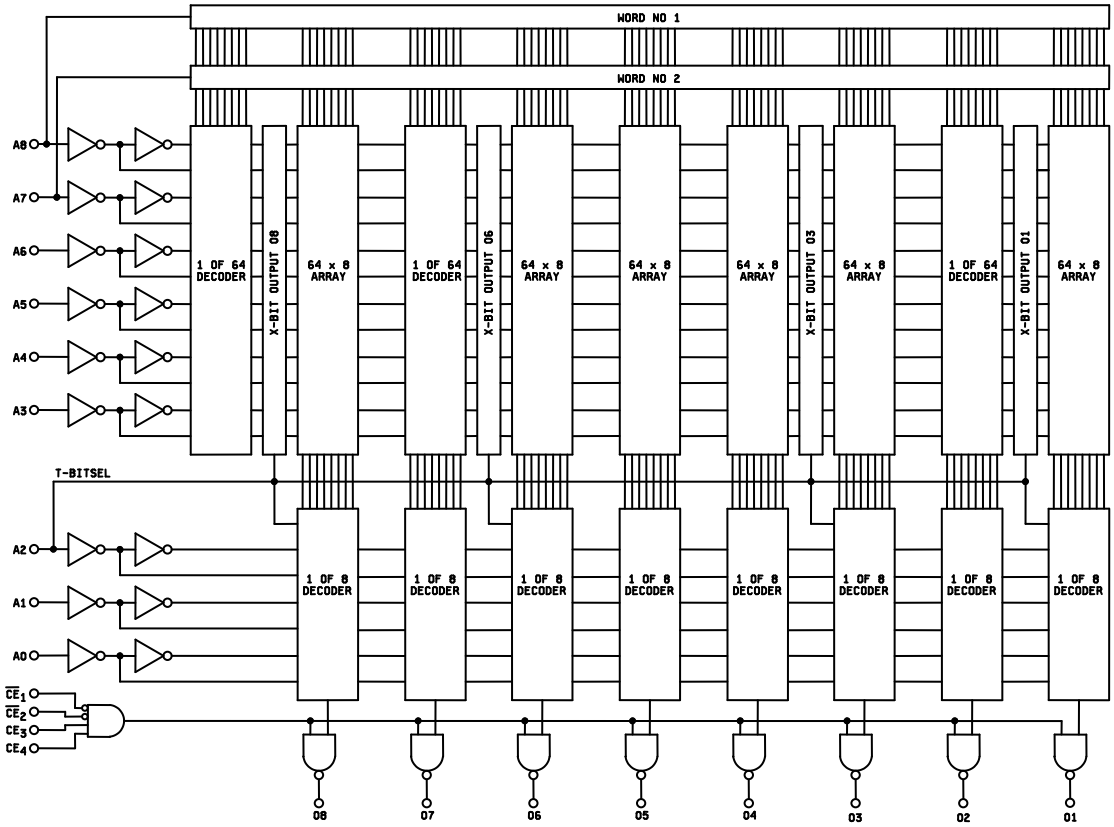


FIGURE 5. Logic diagrams – Continued.

LOGIC CIRCUIT G
(Device type 02)

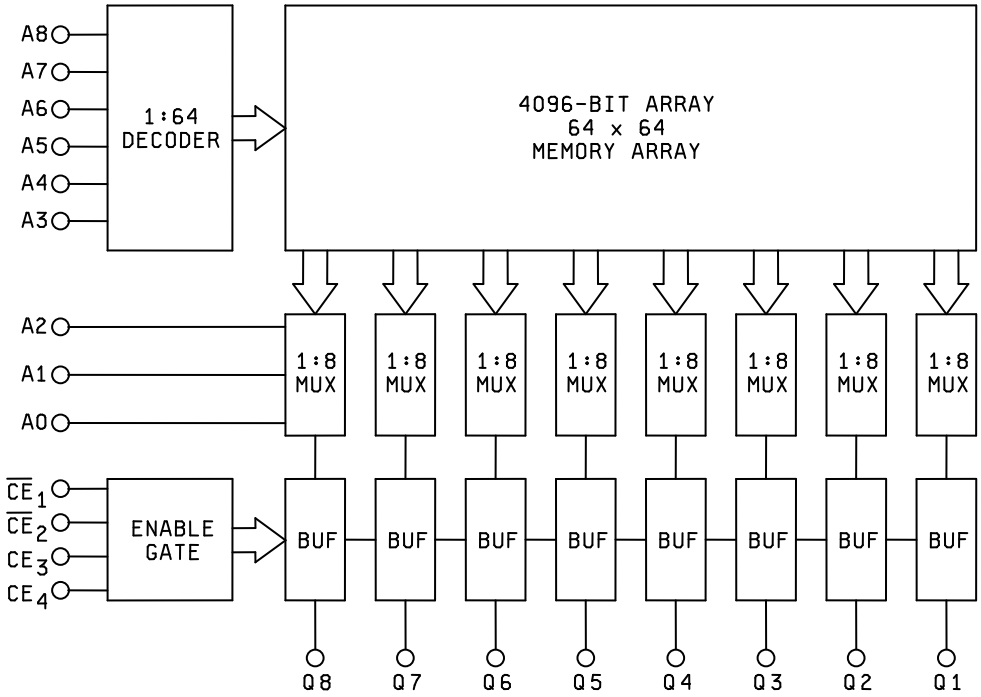


FIGURE 5. Logic diagrams – Continued.

LOGIC CIRCUIT G
(Device types 04 and 05)

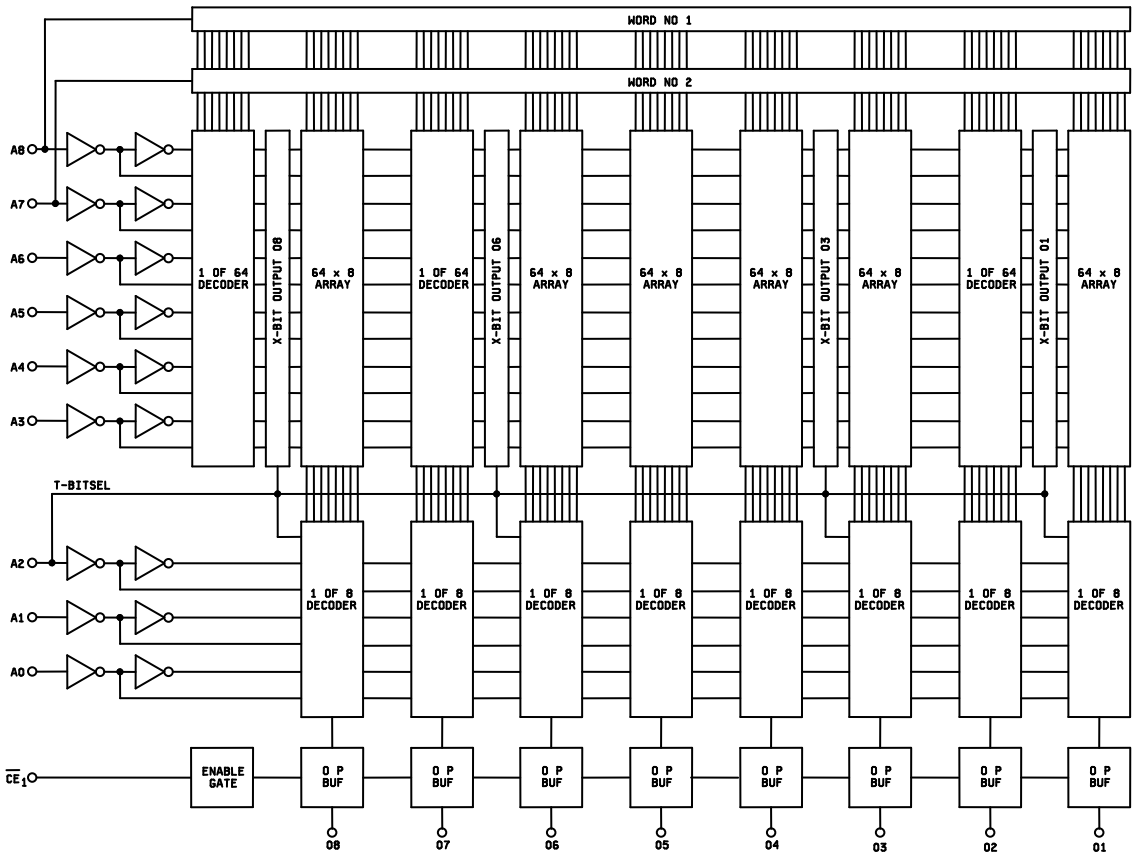
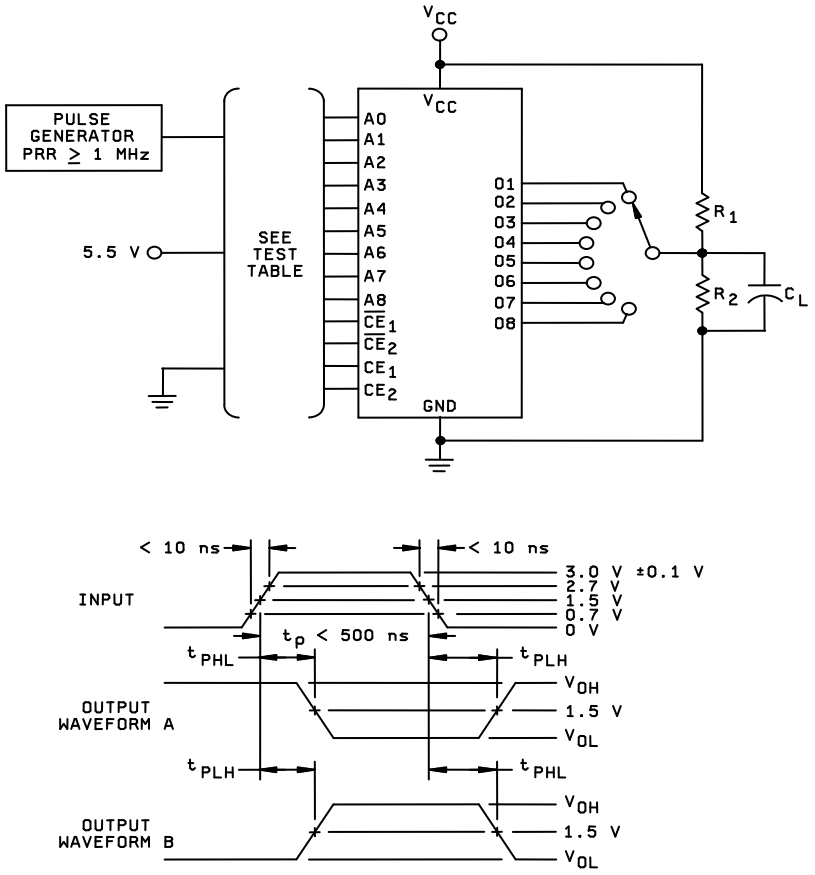


FIGURE 5. Logic diagrams – Continued.

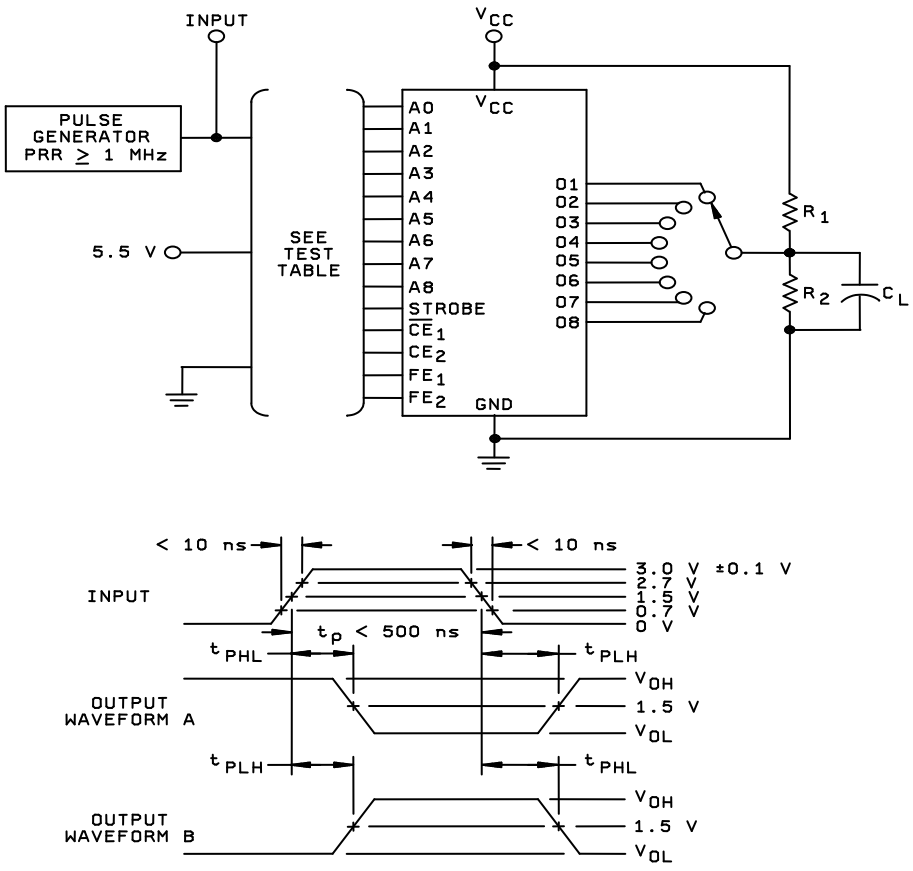
Device types 01 and 02



NOTES:
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory
2. C_L = 30 pF minimum, including jig and probe capacitance, R_1 =330 Ω ±25%, and R_2 = 680 Ω ±20%.
3. Outputs may be under load simultaneously.

FIGURE 6. Switching time test circuit.

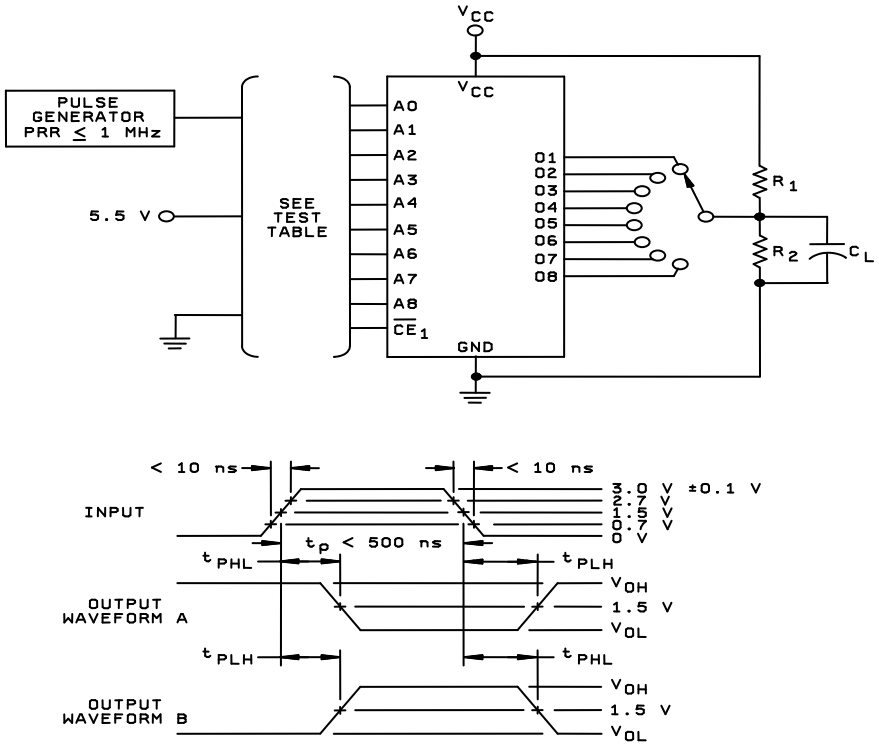
Device type 03



NOTES:
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory
2. C_L = 30 pF minimum, including jig and probe capacitance, R_1 =330 Ω ±25%, and R_2 = 680 Ω ±20%.
3. Outputs may be under load simultaneously.

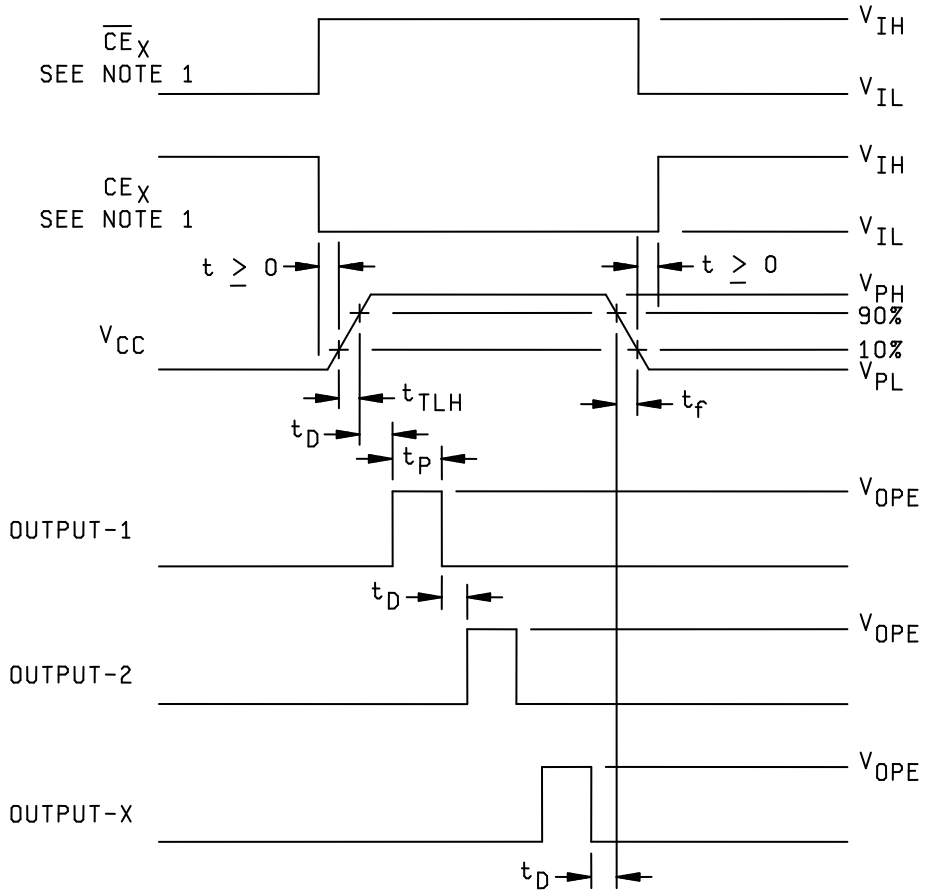
FIGURE 6. Switching time test circuit – Continued.

Device types 04 and 05



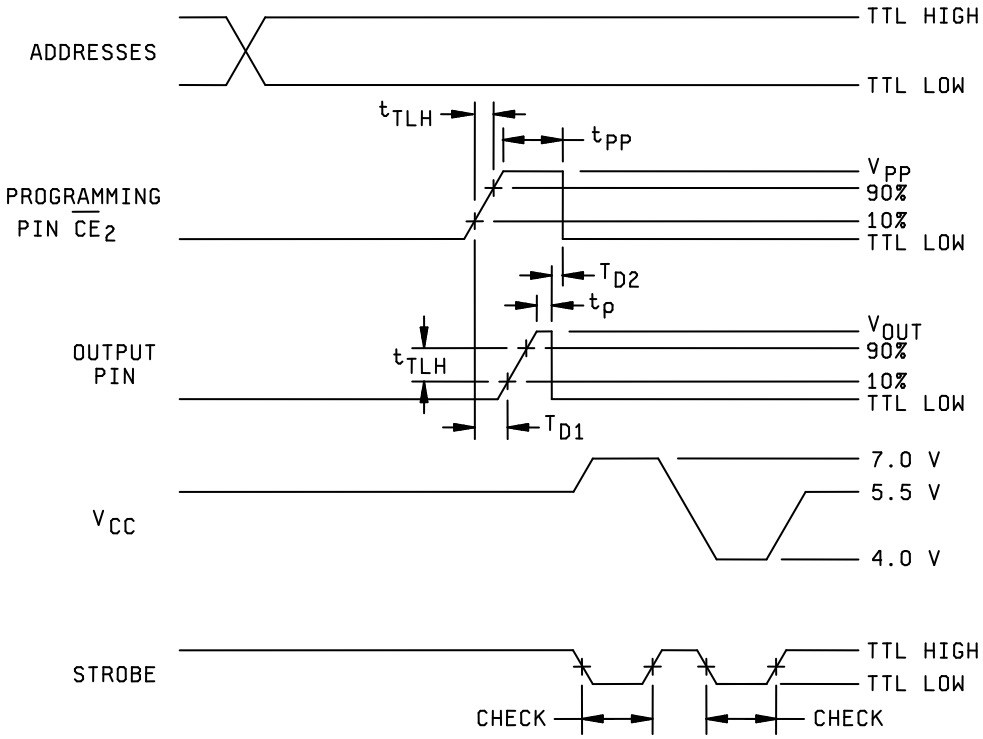
NOTES:
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory
2. C_L = 30 pF minimum, including jig and probe capacitance, R_1 =330 Ω ±25%, and R_2 = 680 Ω ±20%.
3. Outputs may be under load simultaneously.

FIGURE 6. Switching time test circuit – Continued.



NOTES:
1. Disregard for devices with no chip enable inputs.
2. All other waveforms characteristics shall be as specified in table IVA.

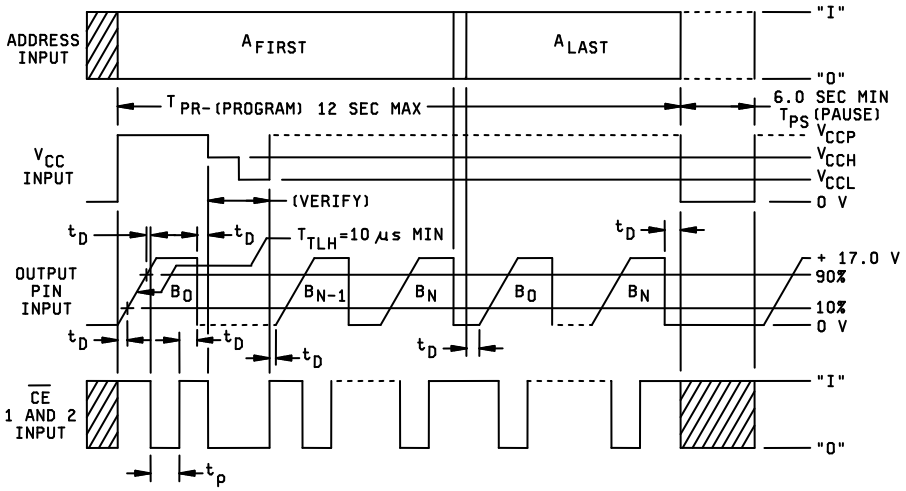
FIGURE 7a. Programming voltage waveforms during programming for circuit A.



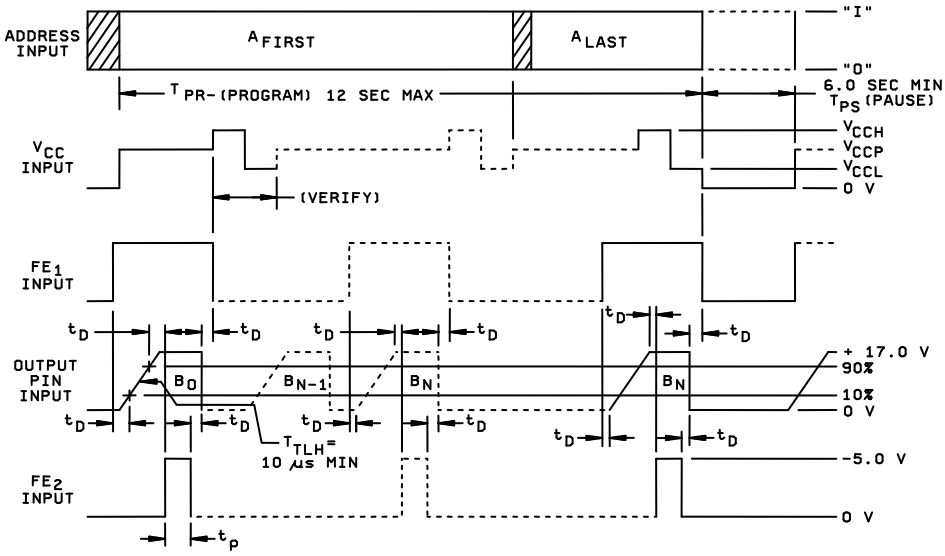
NOTES:
1. Output load is 0.2 mA and 12 mA during 7.0 V and 4.0 V check, respectively.
2. All other waveform characteristics shall be as specified in table IVB.
3. $\overline{CE}_1$ is the programming pin for device types 04 and 05.

FIGURE 7b. Programming voltage waveforms during programming for circuit B.

Device types 01 and 02

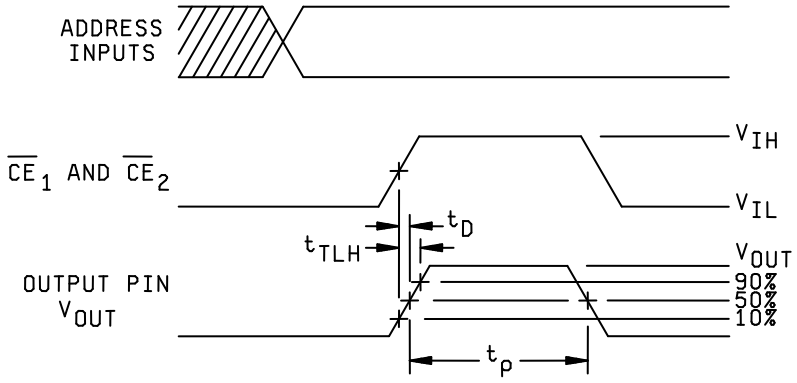


Device type 03



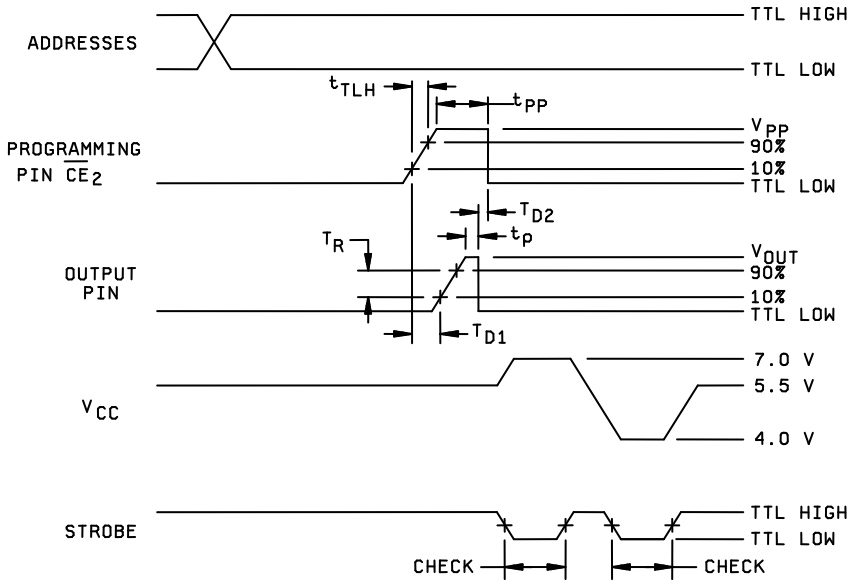
NOTE: All other waveform characteristics shall be as specified in table IVC.

FIGURE 7c. Programming voltage waveforms during programming for circuits C and H.



NOTE: All other waveform characteristics shall be as specified in table IVD.

FIGURE 7d Programming voltage waveforms during programming for circuit D.



NOTES:
1. Output load is 0.2 mA and 12 mA during 7.0 V and 4.0 V check, respectively.
2. All other waveform characteristics shall be as specified in table IVF.

FIGURE 7f. Programming voltage waveforms during programming for circuit F.

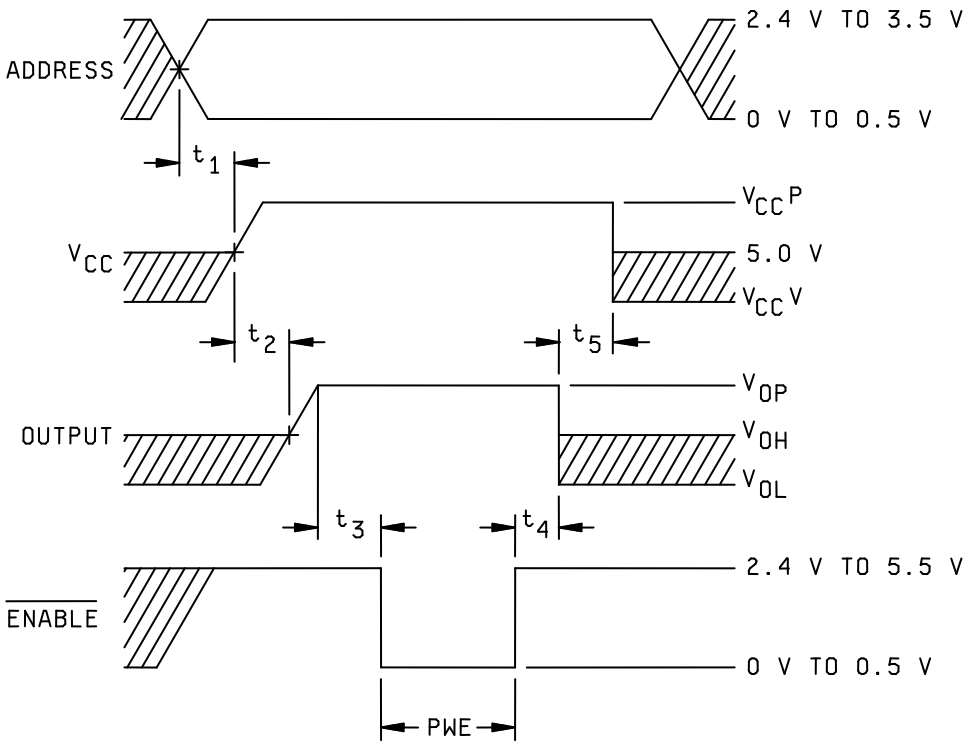


FIGURE 7g. Programming voltage waveforms during programming for circuit G.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. Additional screening for space level product shall be as specified in MIL-PRF-38535, appendix B.

d. Class B devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein. Class S devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III) 1/, 2/, 3/	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters for unprogrammed devices	1*, 2, 3, 7*, 8	1*, 2, 3, 7*, 8
Final electrical test parameters for programmed devices	1*, 2, 3, 7* 8, 9, 10, 11	1*, 2, 3, 7*, 8, 9,
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8 9, 10, 11
Group B end-point electrical parameters when using the method 5005 QCI option	1, 2, 3, 7, 8, 9, 10, 11	N/A
Group C end-point electrical parameters	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8
Group D test requirements	1, 2, 3, 7, 8	1, 2, 3, 7, 8

1/ * indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 shall consist of verifying the pattern specified.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and as specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Electrical test requirements shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 shall be omitted.

c. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.3.2.1). If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowed.

d. For unprogrammed devices, 10 devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two total devices fail in all three subgroups, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more that 4 total device failures allowed.

TABLE III. Group A inspection for device type 01.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; input not designated are high ≥ 2.0 V, lo

Subgroup	Symbol	MIL-STD-883 method	Cases J,K, X,Z	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE_4	CE_3	$\overline{CE}_2$	$\overline{CE}_1$	NC	A8
1 T_C=25°C	V_{IC}		1	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA				GND						-10mA	-10mA	-10mA	-10mA		-10m
	V_{OL}	3007	14	1/ 2/	1/ 3/	1/	1/	1/	1/	1/	1/ 2/	8 mA	8 mA	8 mA	"	8 mA	8 mA	8 mA	8 mA	8 mA	2.4V	2.4V	0.5V	0.5V		1/2/4
	I_{IL1}	3009	22	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V				"								0.5V	0.5V		0.5V
	I_{IL2}	"	33												"						0.5V	0.5V				
	I_{IH1}	3010	35	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V				"						5.5V	5.5V		5.5V		5.5V
	I_{IH2}	"	47												"								4.5V			

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 – Continued.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; input not designated are high ≥ 2.0 V, lo

Subgroup	Symbol	MIL-STD-883 method	Cases J,K, X,Z	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE_4	CE_3	$\overline{CE}_2$	$\overline{CE}_1$	NC	A8	V
1 T_C=+25°C	I_{CEX}		48	15/	15/	15/	15/	15/	15/	15/	15/	5.2V	5.2V	5.2V	GND	5.2V	5.2V	5.2V	5.2V	5.2V						15/	5
			49	1/	1/	1/	1/	1/	1/	1/	1/				"											1/	
			50	"	"	"	"	"	"	"	"				"												"	
			51	"	"	"	"	"	"	"	"				"												"	
			52	"	"	"	"	"	"	"	"				"												"	
			53	"	"	"	"	"	"	"	"				"												"	
			54	"	"	"	"	"	"	"	"				"												"	
			55	"	"	"	"	"	"	"	"				"												"	
	I_{CC}	3005	56	GND	GND	GND	GND	GND	GND	GND	GND				"						5/	5/	GND	GND		GND	
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = 125°C and V_{IC} tests are omitted.																										
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																										
7 T_C=25°C	Func-tional test	3014	57	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	6/	6/	6/	6/		6/	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = 125°C.																										
9 T_C=25°C	t_{PLH1}	GALPAT Fig. 6	58	7/	7/	7/	7/	7/	7/	7/	7/	9/	9/	9/	GND	9/	9/	9/	9/	9/	5.5V	5.5V	GND	GND		7/	
	t_{PHL1}	GALPAT Fig. 6	59	7/	7/	7/	7/	7/	7/	7/	7/	"	"	"	"	"	"	"	"	"	5.5V	5.5V	GND	GND		7/	
	t_{PLH2}	Sequen-tial Fig. 6	60	8/	8/	8/	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/		8/	
	t_{PHL2}	Sequen-tial Fig. 6	61	8/	8/	8/	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/		8/	
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = 125°C.																										
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.																										

See footnotes at end of table.

TABLE III. Group A inspection for device type 02.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; input not designated are high ≥ 2.0 V, lo

Subgroup	Symbol	MIL-STD-883 method	Cases J,K, X,Z	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE_4	CE_3	$\overline{CE}_2$	$\overline{CE}_1$	NC	A8
1 T_C=25°C	V_{IC}		1	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA				GND						-10mA	-10mA	-10mA	-10mA		-10m
			2	"	"	"	"	"	"	"	"				"												
			3	"	"	"	"	"	"	"	"				"												
			4	"	"	"	"	"	"	"	"				"												
			5	"	"	"	"	"	"	"	"				"												
			6	"	"	"	"	"	"	"	"				"												
			7	"	"	"	"	"	"	"	"				"												
			8	"	"	"	"	"	"	"	"				"												
			9	"	"	"	"	"	"	"	"				"												
			10	"	"	"	"	"	"	"	"				"												
			11	"	"	"	"	"	"	"	"				"												
			12	"	"	"	"	"	"	"	"				"												
			13	"	"	"	"	"	"	"	"				"												
	V_{OL}	3007	14	1/ 2/	1/ 3/	1/	1/	1/	1/	1/	1/ 2/	8 mA	8 mA	8 mA	"	8 mA	8 mA	8 mA	8 mA	8 mA	2.4V	2.4V	0.5V	0.5V		1/ 4/
		"	15	"	"	"	"	"	"	"	"				"						"	"	"	"		"
		"	16	"	"	"	"	"	"	"	"				"						"	"	"	"		"
		"	17	"	"	"	"	"	"	"	"				"						"	"	"	"		"
		"	18	16/	16/	16/	16/	16/	16/	16/	16/				"						"	"	"	"		16/
		"	19	"	"	"	"	"	"	"	"				"						"	"	"	"		"
		"	20	"	"	"	"	"	"	"	"				"						"	"	"	"		"
		"	21	13/	13/	13/	13/	13/	13/	13/	13/				"						"	"	"	"		13/
	V_{OH}	3006	22	"	1/ 10/	1/	1/ 25/	1/	1/	1/	1/	-2mA	-2mA	-2mA	"	-2mA	-2mA	-2mA	-2mA	-2mA	"	"	"	"		1/ 10
		"	23	"	"	"	"	"	"	"	"				"						"	"	"	"		"
		"	24	"	"	"	"	"	"	"	"				"						"	"	"	"		"
		"	25	"	"	"	"	"	"	"	"				"						"	"	"	"		"
		"	26	"	"	"	"	"	"	"	"				"						"	"	"	"		"
		"	27	"	"	"	"	"	"	"	"				"						"	"	"	"		"
		"	28	"	"	"	"	"	"	"	"				"						"	"	"	"		"
		"	29	17/	17/	17/	17/	17/	17/	17/	17/				"						"	"	"	"		17/
	I_{IL1}	3009	30	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V				"								0.5V	0.5V		0.5V
		"	31												"											
		"	32												"											
		"	33												"											
		"	34												"											
		"	35												"											
		"	36												"											
		"	37												"											
		"	38												"											
		"	39												"											
		"	40												"											
	I_{IL2} 24/	"	41												"						0.5V					
		"	42												"							0.5V				
	I_{IH1}	3010	43	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V				"											
		"	44												"											
		"	45												"											
		"	46												"											
		"	47												"											
		"	48												"											
		"	49												"											
		"	50												"											
		"	51												"											
		"	52												"											
		"	53												"											
		"	54												"						5.5V	5.5V		5.5V		5.5V
	I_{IH2} 23/	"	55												"								4.5V			

See footnotes at end of table.

TABLE III. Group A inspection for device type 02 – Continued.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; input not designated are high ≥ 2.0 V, lo

Subgroup	Symbol	MIL-STD-883 method	Cases J,K, X,Z	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
			Test no.	A7	A6	A5	A4	A3	A2	A1	A0	O1	O2	O3	GND	O4	O5	O6	O7	O8	CE_4	CE_3	$\overline{CE}_2$	$\overline{CE}_1$	NC	A8
1 T_C=25°C	I_{OHZ}		56									5.2V	5.2V	5.2V	GND						GND	GND	5.5V	5.5V		
			57												"						"	"	"	"		
			58												"						"	"	"	"		
			59												"	5.2V					"	"	"	"		
			60												"		5.2V				"	"	"	"		
			61												"			5.2V			"	"	"	"		
			62												"				5.2V		"	"	"	"		
			63												"					5.2V	"	"	"	"		
	I_{OLZ}		64									0.5V	0.5V	0.5V	"						"	"	"	"		
			65												"						"	"	"	"		
			66												"						"	"	"	"		
			67												"	0.5V					"	"	"	"		
			68												"		0.5V				"	"	"	"		
			69												"			0.5V			"	"	"	"		
			70												"				0.5V		"	"	"	"		
			71												"					0.5V	"	"	"	"		
	I_{CC}	3005	72	GND	GND	GND	GND	GND	GND	GND	GND				"						5/	5/	GND	GND		GND
	I_{OS}	3011	73	1/	1/ 10/	1/	1/	1/	1/	1/	1/	GND	GND	GND	"						5.5V	5.5V	"	"		1/ 10
		"	74	"	"	"	"	"	"	"	"				"						"	"	"	"		"
		"	75	"	"	"	"	"	"	"	"				"						"	"	"	"		"
		"	76	"	"	"	"	"	"	"	"				"	GND					"	"	"	"		"
		"	77	"	"	"	"	"	"	"	"				"		GND				"	"	"	"		"
		"	78	"	"	"	"	"	"	"	"				"			GND			"	"	"	"		"
		"	79	"	"	"	"	"	"	"	"				"				GND		"	"	"	"		"
		"	80	18/	18/	18/	18/	18/	18/	18/	18/				"					GND	"	"	"	"		18/
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = 125°C and V_{IC} tests are omitted.																									
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																									
7 T_C=25°C	Func-tional test	3014	81	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	6/	6/	6/	6/		6/
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = 125°C and T_C = -55°C.																									
9 T_C=25°C	t_{PLH1}	GALPAT Fig. 6	82	7/	7/	7/	7/	7/	7/	7/	7/	9/	9/	9/	GND	9/	9/	9/	9/	9/	5.5V	5.5V	GND	GND		7/
	t_{PHL1}	GALPAT Fig. 6	83	7/	7/	7/	7/	7/	7/	7/	7/	"	"	"	"	"	"	"	"	"	5.5V	5.5V	GND	GND		7/
	t_{PLH2}	Sequen-tial Fig. 6	84	8/	8/	8/	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/		8/
	t_{PHL2}	Sequen-tial Fig. 6	85	8/	8/	8/	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	9/		8/
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = 125°C.																									
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.																									

See footnotes at end of table.

TABLE III. Group A inspection for device type 03.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high ≥ 2.0 V, l

Subgroup	Symbol	MIL-STD-883 method	Cases J,K,X Test no.	1 A3	2 A4	3 A5	4 A6	5 A7	6 A8	7 O1	8 O2	9 O3	10 O4	11 FE2	12 GND	13 FE1	14 O5	15 O6	16 O7	17 O8	18 Strobe	19 $\overline{CE}_2$	20 $\overline{CE}_1$	21 A0	22 A1	23 A2	V
1 T_C=25°C	V_{IC}		1	-10mA	-10mA	-10mA	-10mA	-10mA	-10mA					-10mA	GND	-10mA					-10mA	-10mA	-10mA	-10mA	-10mA	-10mA	4
			2	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
			3	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
			4	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
			5	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
			6	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
			7	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
			8	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
			9	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
			10	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
			11	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
			12	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
			13	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
			14	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
	V_{OL}	3007	15	1/	1/	1/	1/	1/	1/	8mA	8mA	8mA	8mA	GND	"	GND	8mA	8mA	8mA	8mA	2.4V	2.4V	0.5V	1/	1/	1/	
		"	16	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
		"	17	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
		"	18	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
		"	19	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
		"	20	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
		"	21	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
		"	22	"	"	"	"	"	"					"	"	"					"	"	"	"	"	"	
	V_{OH}	3006	23	"	"	"	"	"	1/ 10/	-2mA	-2mA	-2mA	-2mA	"	"	"	-2mA	-2mA	-2mA	-2mA	"	"	"	"	"	"	
		"	24	"	"	"	"	"	"					"	"	"					"	"	"	"		"	
		"	25	"	"	"	"	"	"					"	"	"					"	"	"	"		"	
		"	26	"	"	"	"	"	"					"	"	"					"	"	"	"		"	
		"	27	"	"	"	"	"	"					"	"	"					"	"	"	"		"	
		"	28	"	"	"	"	"	"					"	"	"					"	"	"	"		"	
		"	29	"	"	"	"	"	"					"	"	"					"	"	"	"		"	
		"	30	"	"	"	"	"	"					"	"	"					"	"	"	"		"	
	I_{IL1}	3009	31	0.5V	0.5V	0.5V	0.5V	0.5V	0.5V					0.5V	"	0.5V					0.5V	0.5V	0.5V	0.5V	0.5V	0.5V	5
		"	32												"											
		"	33												"											
		"	34												"											
		"	35												"											
		"	36												"											
		"	37												"											
		"	38												"											
		"	39												"											
		"	40												"											
		"	41												"											
		"	42												"											
		"	43												"											
		"	44												"											
	I_{IH1}	3010	45	5.5V	5.5V	5.5V	5.5V	5.5V	5.5V						"						5.5V	5.5V	5.5V	5.5V	5.5V	5.5V	
		"	46												"											
		"	47												"											
		"	48												"											
		"	49												"											
		"	50												"											
		"	51												"											
		"	52												"											
		"	53												"											
		"	54												"											
		"	55												"											
		"	56												"											

See footnotes at end of table.

TABLE III. Group A inspection for device type 03 – Continued.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; input not designated are high ≥ 2.0 V, lo

Subgroup	Symbol	MIL-STD-883 method	Cases J,K,X Test no.	1 A3	2 A4	3 A5	4 A6	5 A7	6 A8	7 O1	8 O2	9 O3	10 O4	11 FE_2	12 GND	13 FE_1	14 O5	15 O6	16 O7	17 O8	18 Strobe	19 $\overline{CE}_2$	20 $\overline{CE}_1$	21 A0	22 A1	23 A2
1 T_C=25°C	I_{OHZ}		57 58 59 60 61 62 63 64							5.2V	5.2V	5.2V	5.2V		GND " " " " " " "		5.2V	5.2V	5.2V	5.2V	0.5V " " " " " " "	2.4V " " " " " " "	0.5V " " " " " " "			
	I_{OLZ}		65 66 67 68 69 70 71 72							0.5V	0.5V	0.5V	0.5V		" " " " " " " "		0.5V	0.5V	0.5V	0.5V	" " " " " " " "	" " " " " " " "	" " " " " " " "			
	I_{CC}	3005	73	GND	GND	GND	GND	GND	GND					GND	"	GND					GND	GND	GND			
	I_{OS}	3011	74 75 76 77 78 79 80 81	1/ " " " " " " "	1/ " " " " " " "	1/ " " " " " " "	1/ 25/ " " " " " " "	1/ " " " " " " "	1/ 10/ " " " " " " "	GND	GND	GND	GND		"		GND	GND	GND	GND	"	5.5V " " " " " " "	" " " " " " " "	1/ " " " " " " "	1/ 10/ " " " " " " "	1/ " " " " " " "
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = 125°C and V_{IC} tests are omitted.																									
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																									
7 T_C=25°C	Func-tional test	3014	82	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	6/	6/	6/	6/		6/
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = 125°C and T_C = -55°C.																									
9 T_C=25°C	t_{PLH1}	GALPAT Fig. 6	83	7/	7/	7/	7/	7/	7/	9/	9/	9/	9/	GND	GND	GND	9/	9/	9/	9/	GND	5.5V	GND	7/	7/	7/
	t_{PHL1}	GALPAT Fig. 6	84	7/	7/	7/	7/	7/	7/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	7/	7/	7/
	t_{PLH2}	Sequen-tial Fig. 6	85	8/	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	8/	8/	8/
	t_{PHL2}	Sequen-tial Fig. 6	86	8/	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	8/	8/	8/
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = 125°C.																									
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.																									

See footnotes at end of table.

TABLE III. Group A inspection for device type 04.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; input not designated are high ≥ 2.0 V, lo

Subgroup	Symbol	MIL-STD-883 method	Case Y Test no.	1 A0	2 A1	3 A2	4 A3	5 A4	6 O1	7 O2	8 O3	9 O4	10 GND	11 O5	12 O6	13 O7	14 O8	15 $\overline{CE}_1$	16 A5	17 A6	18 A7	19 A8	20 V_{CC}
1 T_C=25°C	V_{IC}		1	-10mA	-10mA	-10mA	-10mA	-10mA					GND					-10mA	-10mA	-10mA	-10mA	-10mA	4.5V
			2										"										"
			3										"										"
			4										"										"
			5										"										"
			6										"										"
			7										"										"
			8										"										"
			9										"										"
			10										"										"
	V_{OL}	3007	11	2.4V	1/ 3/	1/	1/	1/	8mA	8mA	8mA	8mA	"	8mA	8mA	8mA	8mA	0.5V	1/	1/	1/	1/	"
		"	12	"	"	"	"	"					"					"	"	"	"	"	"
		"	13	"	"	"	"	"					"					"	"	"	"	"	"
		"	14	"	"	"	"	"					"					"	"	"	"	"	"
		"	15	"	"	"	"	"					"					"	"	"	"	"	"
		"	16	"	"	"	"	"					"					"	"	"	"	"	"
		"	17	"	"	"	"	"					"					"	"	"	"	"	"
		"	18	" 19/	19/	19/	19/	19/					"					19/	19/	19/	19/	19/	19/
	I_{IL}	3009	19	0.5V	0.5V	0.5V	0.5V	0.5V					"					0.5V	0.5V	0.5V	0.5V	0.5V	5.5V
		"	20										"										"
		"	21										"										"
		"	22										"										"
		"	23										"										"
		"	24										"										"
		"	25										"										"
		"	26										"										"
		"	27										"										"
		"	28										"										"
	I_{IH1}	3010	29	5.5V	5.5V	5.5V	5.5V	5.5V					"						5.5V	5.5V	5.5V	5.5V	"
		"	30										"										"
		"	31										"										"
		"	32										"										"
		"	33										"										"
		"	34										"										"
		"	35										"										"
		"	36										"										"
		"	37										"										"
	I_{IH2}	"	38										"					4.5V					"
	I_{CEX}		39						5.2V	5.2V	5.2V	5.2V	"	5.2V	5.2V	5.2V	5.2V	5.5V					"
			40										"					"					"
			41										"					"					"
			42										"					"					"
			43										"					"					"
			44										"					"					"
			45										"					"					"
			46										"					"					"
	I_{CC}	3005	47	GND	GND	GND	GND	GND					"					GND	GND	GND	GND	GND	"

See footnotes at end of table.

TABLE III. Group A inspection for device type 04 – Continued.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; input not designated are high ≥ 2.0 V, lo

Subgroup	Symbol	MIL-STD-883 method	Case Y Test no.	1 A0	2 A1	3 A2	4 A3	5 A4	6 O1	7 O2	8 O3	9 O4	10 GND	11 O5	12 O6	13 O7	14 O8	15 $\overline{CE}_1$	16 A5	17 A6	18 A7	19 A8	20 V_{CC}
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = 125°C and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																						
7 T_C=25°C	Func-tional test	3014	48	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = 125°C and T_C = -55°C.																						
9 T_C=25°C	t_{PLH1}	GALPAT Fig. 6	49	7/	7/	7/	7/	7/	9/	9/	9/	9/	GND	9/	9/	9/	9/	GND	7/	7/	7/	7/	7/
	t_{PHL1}	GALPAT Fig. 6	50	7/	7/	7/	7/	7/	"	"	"	"	"	"	"	"	"	GND	7/	7/	7/	7/	7/
	t_{PLH2}	Sequential Fig. 6	51	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/	8/	8/
	t_{PHL2}	Sequential Fig. 6	52	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/	8/	8/
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = 125°C.																						
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.																						

See footnotes at end of table.

TABLE III. Group A inspection for device type 05.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; input not designated are high ≥ 2.0 V, lo

Subgroup	Symbol	MIL-STD-883 method	Case Y Test no.	1 A0	2 A1	3 A2	4 A3	5 A4	6 O1	7 O2	8 O3	9 O4	10 GND	11 O5	12 O6	13 O7	14 O8	15 $\overline{CE}_1$	16 A5	17 A6	18 A7	19 A8	20 V_{CC}
1 T_C=25°C	V_{IC}		1	-10mA	-10mA	-10mA	-10mA	-10mA					GND					-10mA	-10mA	-10mA	-10mA	-10mA	4.5V
			2	"	"	"	"	"					"										"
			3	"	"	"	"	"					"										"
			4	"	"	"	"	"					"										"
			5	"	"	"	"	"					"										"
			6	"	"	"	"	"					"										"
			7	"	"	"	"	"					"										"
			8	"	"	"	"	"					"										"
			9	"	"	"	"	"					"										"
			10	"	"	"	"	"					"										"
	V_{OL}	3007	11	2.4V	1/ 3/	1/ 11/	1/ 11/	1/ 11/	12/	12/	12/	12/	"	12/	12/	12/	12/	0.5V	1/	1/	1/	1/	"
		"	12	"	"	"	"	"					"					"	"	"	"	"	"
		"	13	"	"	"	"	"					"					"	"	"	"	"	"
		"	14	"	"	"	"	"					"					"	"	"	"	"	"
		"	15	"	"	"	"	"					"					"	"	"	"	"	"
		"	16	"	"	"	"	"					"					"	"	"	"	"	"
		"	17	"	"	"	"	"					"					"	"	"	"	"	"
		"	18	20/	20/	20/	20/	20/					"					"	20/	20/	20/	20/	"
	V_{OH}	3006	19	1/	1/	1/	1/	1/	-2mA	-2mA	-2mA	-2mA	"	-2mA	-2mA	-2mA	-2mA	"	1/	1/	1/	1/	"
		"	20	"	"	"	"	"					"					"	"	"	"	"	"
		"	21	"	"	"	"	"					"					"	"	"	"	"	"
		"	22	"	"	"	"	"					"					"	"	"	"	"	"
		"	23	"	"	"	"	"					"					"	"	"	"	"	"
		"	24	"	"	"	"	"					"					"	"	"	"	"	"
		"	25	"	"	"	"	"					"					"	"	"	"	"	"
		"	26	21/	21/	21/	21/	21/					"					"	21/	21/	21/	21/	"
	I_{IL}	3009	27	0.5V	0.5V	0.5V	0.5V	0.5V					"					0.5V	0.5V	0.5V	0.5V	0.5V	5.5V
		"	28										"										"
		"	29										"										"
		"	30										"										"
		"	31										"										"
		"	32										"										"
		"	33										"										"
		"	34										"										"
		"	35										"										"
		"	36										"										"
	I_{IH1}	3010	37	5.5V	5.5V	5.5V	5.5V	5.5V					"						5.5V	5.5V	5.5V	5.5V	"
		"	38										"										"
		"	39										"										"
		"	40										"										"
		"	41										"										"
		"	42										"										"
		"	43										"										"
		"	44										"										"
		"	45										"										"
	I_{IH2}	"	46										"					4.5V					"

See footnotes at end of table.

TABLE III. Group A inspection for device type 05 – Continued.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; input not designated are high ≥ 2.0 V, lo

Subgroup	Symbol	MIL-STD-883 method	Case Y Test no.	1 A0	2 A1	3 A2	4 A3	5 A4	6 O1	7 O2	8 O3	9 O4	10 GND	11 O5	12 O6	13 O7	14 O8	15 $\overline{CE}_1$	16 A5	17 A6	18 A7	19 A8	20 V_{CC}
1 T_C=25°C	I_{OHZ}		47						5.2V	5.2V	5.2V	5.2V	GND	5.2V	5.2V	5.2V	5.2V	5.5V					5.5V
			48						"	"	"	"	"	"	"	"	"	"					"
			49						"	"	"	"	"	"	"	"	"	"					"
			50						"	"	"	"	"	"	"	"	"	"					"
			51						"	"	"	"	"	"	"	"	"	"					"
			52						"	"	"	"	"	"	"	"	"	"					"
			53						"	"	"	"	"	"	"	"	"	"					"
			54						"	"	"	"	"	"	"	"	"	"					"
	I_{OLZ}		55						0.5V	0.5V	0.5V	0.5V	"	0.5V	0.5V	0.5V	0.5V	"					"
			56						"	"	"	"	"	"	"	"	"	"					"
			57						"	"	"	"	"	"	"	"	"	"					"
			58						"	"	"	"	"	"	"	"	"	"					"
			59						"	"	"	"	"	"	"	"	"	"					"
			60						"	"	"	"	"	"	"	"	"	"					"
			61						"	"	"	"	"	"	"	"	"	"					"
			62						"	"	"	"	"	"	"	"	"	"					"
	I_{CC}	3005	63	GND	GND	GND	GND	GND					"					GND	GND	GND	GND	GND	"
	I_{OS}	3011	64	1/	1/	1/	1/	1/	GND	GND	GND	GND	"	GND	GND	GND	GND	0.5V	1/	1/	1/	1/	"
		"	65	"	"	"	"	"					"					"	"	"	"	"	"	"
		"	66	"	"	"	"	"					"					"	"	"	"	"	"	"
		"	67	"	"	"	"	"					"					"	"	"	"	"	"	"
		"	68	"	"	"	"	"					"					"	"	"	"	"	"	"
		"	69	"	"	"	"	"					"					"	"	"	"	"	"	"
		"	70	"	"	"	"	"					"					"	"	"	"	"	"	"
		"	71	22/	22/	22/	22/	22/					"					"	22/	22/	22/	22/	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = 125°C and V_{IC} tests are omitted.																						
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																						
7 T_C=25°C	Func-tional test	3014	72	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = 125°C and T_C = -55°C.																						
9 T_C=25°C	t_{PLH1}	GALPAT Fig. 6	73	7/	7/	7/	7/	7/	9/	9/	9/	9/	GND	9/	9/	9/	9/	GND	7/	7/	7/	7/	7/
	t_{PHL1}	GALPAT Fig. 6	74	7/	7/	7/	7/	7/	"	"	"	"	"	"	"	"	"	GND	7/	7/	7/	7/	7/
	t_{PLH2}	Sequential Fig. 6	75	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/	8/	8/
	t_{PHL2}	Sequential Fig. 6	76	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/	8/	8/
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = 125°C.																						
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.																						

See footnotes at end of table.

1/ For unprogrammed devices, select an appropriate address to acquire the desired output state.

2/ For unprogrammed devices (circuit D), apply 12.0 V on pin 8 (A0) and pin 1 (A7).

3/ For unprogrammed device types 01 and 02 (circuit B), apply 12.0 V on pin 2 (A6); for unprogrammed device types 04 and 05 (circuit B), apply 12.0 V on pin 2 (A1).

4/ For unprogrammed devices (circuit A), apply 11.0 V on pin 23 (A8).

5/ CE_4 and CE_3 may be “GND” or “2.4 V”.

6/ The functional test shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II and 3.3.2.2). All bits shall be tested. The functional tests shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V. Terminal conditions shall be as follows:

a. Inputs: H = 3.0 V, L = 0.0 V.

b. Outputs: Output voltage shall be either:

(1) H = 2.4 V minimum and L = 0.5 V maximum when using a high-speed checker double comparator, or
(2) H ≥ 1.0 V and L < 1.0 V when using a high-speed checker single comparator.

7/ GALPAT (PROGRAMMED PROM). This program will test all bits in the array, the addressing and interaction between bits for ac performance, t_{PLH1} and t_{PHL1}. Each bit in the pattern is fixed by being programmed with an “H” or “L”. The GALPAT tests shall be performed with V_{CC} = 4.5 V and 5.5 V.

Description:
Step 1. Word 0 is read.
Step 2. Word 1 is read.
Step 3. Word 0 is read.
Step 4. Word 2 is read.
Step 5. Word 0 is read.
Step 6. The reading procedure continues back and forth between word 0 and the next higher numbered word until word 511 is reached, then increments to the next word and reads back and forth as in step 1 through step 6 and shall include all words.
Step 7. Pass execution time = $(n^2 + n)$ x cycle time. n = 512.

8/ SEQUENTIAL (PROGRAMMED PROM). This program will test all bits in the array for t_{PLH2} and t_{PHL2}. The SEQUENTIAL tests shall be performed with V_{CC} = 4.5 V and 5.5 V.

Description:
Step 1. Each word in the pattern is tested from the enable lines to the output lines for recovery.
Step 2. Word 0 is addressed. Enable line is pulled high to low and low to high. t_{PHL2} and t_{PLH2} are
Step 3. Word 1 is addressed. Same enable sequence as above.
Step 4. The reading procedure continues until word 511 is reached.
Step 5. Pass execution time = 512 x cycle time.

9/ The outputs are loaded per figure 6.

10/ For uprogrammed device types 01 and 02 (circuit C), apply 10.0 V on pin 23 (A8); 0.5 V on pin 2 (A6); and 5.0 V on all other address pins. For unprogrammed device type 03 (circuit C), apply 10.0 V on pin 6 (A8); 0.5 V on pin 22 (A1); and 5.0 V on all other address pins.

11/ For unprogrammed devices (circuit F), apply 12.0 V on pin 3 (A2) and 0.0 V on pin 4 (A3).

12/ I_{OL} = 8 mA for circuit B devices; I_{OL} = 16 mA for circuit F devices.

13/ For unprogrammed device types 01, 02, 04, and 05 (circuit G) select an appropriate address to obtain the desired output state.

14/ For programmed device type 02 (circuit G) apply 4.5 V to pin 24; 10.5 V to pin 1; 3.0 V to pins 23, 19, 18, 8, 7, 6, 4, 3, and 2; and 0.0 V to pins 21, 20, 12, and 5.

15/ For unprogrammed device type 01 (circuit G) apply 10.5 V to pins 6 and 1; 5.5 V to pin 24; 3.0 V to pins 23, 19, 18, 8, 7, 6, 4, 3, and 2; 0.0 V to pins 21, 20, 12, and 5.

16/ For programmed device type 02 (circuit G) apply 10.5 V to pin 1; 4.5 V to pin 24; 3.0 V to pins 23, 19, 18, 8, 7, 6, 4, 3, and 2; and 0.0 V to pins 21, 20, 5, and 12.

17/ For unprogrammed device type 02 (circuit G) apply 10.5 V to pins 6 and 1; 4.5 V to pin 24; 3.0 V to pins 23, 19, 18, 8, 7, 4, and 2; 2.0 V to pin 3; 0.0 V to pins 21, 20, 12, and 5.

18/ For unprogrammed device type 02 (circuit G) apply 10.5 V to pins 1 and 6; 5.5 V to pin 24; 3.0 V to pins 23, 19, 18, 8, 7, 4, 3 and 2; 0.0 V to pins 5, 12, 20, and 21.

19/ For programmed device type 04 (circuit G) apply 10.5 V to pin 16; 4.5 V to pin 20; 3.0 V to pins 1, 2, 3, 4, 5, 18, and 19; 0.0 V to pins 10 and 15.

20/ For programmed device type 05 (circuit G) apply 10.5 V to pin 16; 4.5 V to pin 20; 3.0 V to pins 1, 2, 3, 4, 5, 18, and 19; 0.0 V to pins 10 and 15.

21/ For unprogrammed device type 05 (circuit G) apply 10.5 V to pins 17 and 3; 4.5 V to pin 20; 3.0 V to pins 2, 4, 5, 16, 18, and 19; 0.0 V to pins 1, 10, and 15.

22/ For unprogrammed device type 05 (circuit G) apply 10.5 V to pins 3 and 17; 5.5 V to pin 20; 3.0 V to pins 2, 4, 5, 16, 18, and 19; 0.0 V to pins 1, 10, and 15.

23/ At the manufacturer's option, this may be prepared with V_{IH} = 5.5 and test limits of 50 μA maximum.

24/ At the manufacturer's option, this may be performed with V_{IO} = 0.5 V and test limits of -1 μA minimum to -250 μA maximum.

25/ For unprogrammed device type 02 (circuit H) apply 5.0V to pin 24; 0.0V to pins 3, 5, 6, 7, 8, 20, and 21; 3.0V to pins 1, 2, 18, 19, and 23; 9.0V to pin 4.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

c. For qualification, at least 25 percent of the sample selected for life testing shall be programmed (see 3.3.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the life test.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535 and as follows:

a. End-point electrical tests shall be as specified in table II herein.

b. Subgroup 2 shall be omitted for devices in package Z.

c. For moisture resistance and salt atmosphere of subgroups 3 and 5, omit initial conditioning for devices in package Z.

4.5 Methods of inspection. Methods of inspection shall be as specified and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.6 Programming procedure identification. The programming procedure to be utilized shall be identified by the manufacturer's circuit designator.

4.7 Programming procedure for circuit A. The waveforms on figure 7a, the programming characteristics in table IVA and the following procedures shall apply:

a. Connect the device in the electrical configuration for programming.

b. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.

c. Disable the chip by applying V_{IH} to the $\overline{CE}_1$ and $\overline{CE}_2$ inputs and V_{IL} to the CE_3 and CE_4 inputs. The CE inputs are TTL compatible.

d. Disable the programming circuitry by applying a voltage of V_{OPD} to the outputs of the PROM.

e. Raise V_{CC} to V_{PH} as specified on the waveforms on figure 7a.

f. After a delay of t_D, apply only one V_{OPE} pulse with duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.

g. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{PH} level by applying V_{OPE} pulses to each output to be programmed allowing a delay of t_D between pulses as shown on figure 7a.

h. Repeat steps 4.7b through 4.7g for all other bits to be programmed.

i. Lower V_{CC} to 4.5 volts following a delay of t_D from the last programming pulse applied to an output.

j. Enable the chip by applying V_{IL} to the $\overline{CE}_1$ and $\overline{CE}_2$ inputs and V_{IH} to the CE_3 and CE_4 inputs and verify the program.

k. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVA. Programming characteristics for circuit A.

Parameter	Symbol	Limits 1/			Unit
		Min	Recommended	Max	
Address input voltage 2/	V_{IH} V_{IL}	2.4 0.0	5.0 0.4	5.0 0.8	V V
V_{CC} required during programming	V_{PH} V_{PL}	12.0 4.5	12.0 4.5	12.5 5.5	V V
Programming input low current	I_{ILP}	----	-300	-600	µA
Programming voltage transition time	t_{TLH} t_{THL}	1 1	1 1	10 10	µs µs
Programming delay	t_D	10	10	100	µs
Programming pulse width	t_P	90	100	110	µs
Programming duty cycle	D.C.	----	50	90	%
Output voltage Enable 3/ Disable 4/	 V_{OPE} V_{OPD}	 10.5 4.5	 10.5 5.0	 11.0 5.5	 V V
Output voltage enable current	I_{OPE}	----	----	10	mA

1/ T_A = +25°C.

2/ Address and chip enable shall not be left open for V_{IH}.

3/ V_{OPE} supply shall be capable of sourcing 10 mA.

4/ Disable condition can be met with output open circuit.

4.8 Programming procedure for circuit B. The waveforms on figure 7b, the programming characteristics of table IVB, and the following procedures shall apply:

a. Connect the device in the electrical configuration for programming.

b. Raise V_{CC} to 5.5 volts.

c. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.

d. Disable the chip by applying V_{IH} to the $\overline{CE}_1$ and $\overline{CE}_2$ and V_{IL} to the CE_3 and CE_4 inputs (device types 01 and 02) or V_{IH} to the CE input (device types 04 and 05). The CE input is TTL compatible.

e. Apply the V_{PP} pulse to the programming pin $\overline{CE}_2$ (device types 01 and 02) or $\overline{CE}$ (device types 04 and 05). In order to insure that the output transistor is off before increasing the voltage on the output pin, the programming pin's voltage pulse shall precede the output pin's programming pulse by T_{D1} and leave after the output pin's programming pulse by T_{D2} (see figure 7b).

f. Apply only one V_{OUT} pulse with duration of t_P to the output selected for programming. The outputs shall be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.

g. Other bits in the same word may be programmed sequentially by applying V_{PP} pulses to each output to be programmed.

h. Repeat 4.8c through 4.8g for all other bits to be programmed.

i. Enable the chip by applying V_{IL} to the $\overline{CE}_1$ and $\overline{CE}_2$ and V_{IH} to the CE_3 and CE_4 inputs (device types 01 and 02) or V_{IL} to the $\overline{CE}$ inputs (device types 04 and 05) and verify the program. Verification may check for a low output by requiring the device to sink 12 mA at V_{CC} = 4.0 V and 0.2 mA at V_{CC} = 7.0 V at T_A = 25°C.

j. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject. .

TABLE IVB. Programming characteristics for circuit B.

Parameter	Symbol	Conditions	Limits 1/			Unit
			Min	Recommended	Max	
V_{CC} required during programming	V_{CCP}		5.4	5.5	5.6	V
Rise time of programming pulse to data out or programming pin	t_{TLH}		0.34	0.40	0.46	V/µs
Programming voltage on programming pin	V_{PP}		32.5	33	33.5	V
Output programming voltage	V_{OUT}		25.6	26	26.5	V
Programming pin pulse width ($\overline{CE}_2$) 2/	t_{PP}	Chip disabled, V_{CC} = 5.5 V		100	180	ns
Pulse width of programming voltage	t_P	Chip disabled, V_{CC} = 5.5 V	1		40	µs
Required current limit of power supply feeding programming pin and output during programming	I_L	V_{PP} = 33 V, V_{OUT} = 26 V, V_{CC} = 5.5 V	240			mA
Required time delay between disabling memory output and application of output programming pulse	T_{D1}	Measured at 10% levels	70	80	90	µs
Required time delay between removal of programming pulse and enabling memory output	T_{D2}	Measured at 10% levels	100			ns
Output current during verification	I_{OLV1}	Chip enabled, V_{CC} = 4.0 V	11	12	13	mA
	I_{OLV2}	Chip enabled, V_{CC} = 7.0 V	0.19	0.2	0.21	mA
Address input voltage	V_{IH}		2.4	5.0	5.5	V
	V_{IL}		0.0	0.4	0.8	V
Maximum duty cycle during automatic programming of program pin and output pin	D.C.	t_P / t_C	----	----	25	%

1/ T_A = +25°C.

2/ $\overline{CE}_1$ is the programming pin for device types 04 and 05.

4.9 Programming procedures for circuits C and H. The waveforms on figure 7c, the programming characteristics in table IVC, and the following procedures shall be used for programming the device:

4.9.1 Device types 01 and 02.

a. Connect the device in the electrical configuration for programming.

b. Terminate all device outputs with a 10 kΩ resistor to V_{CC}. Apply $\overline{CE}_1 = V_{IH}$, $\overline{CE}_2 = V_{IL}$, $CE_3 = V_{IH}$, and $CE_4 = V_{IH}$.

c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP}.

d. After a t_D delay (10μs), apply only one V_{OUT} pulse to the output to be programmed. Program one output at a time.

e. After a t_D delay (10μs), pulse CE_1 input to logic "0" for a duration of t_P.

f. After a t_D delay (10μs), remove the V_{OUT} pulse from the programmed output. Programming a fuse will cause the output to go to a high-level logic in the verify mode.

g. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OUT} pulses to each output to be programmed allowing a delay of t_D between pulses as shown on figure 7c.

h. Repeat 4.9.1c through 4.9.1g for all other bits to be programmed.

i. To verify programming, after t_D (10 μs) delay, lower V_{CC} to V_{CCH} and apply a logic "0" level to both $\overline{CE}_1$ and $\overline{CE}_2$ inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} and verify that the programmed output remains in the "1" state.

j. For class S and B devices, if any bit does not verify as programmed it shall be considered a programming reject.

4.9.2 Device type 03.

a. Connect the device in the electrical configuration for programming.

b. Terminate all device outputs with a 10 kΩ resistor to V_{CC}. Apply $\overline{CE}_1 = V_{IL}$, $\overline{CE}_2 = V_{IH}$, and strobe = V_{IH}.

c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP}.

d. After a t_D delay (10μs), apply to FE_1 (pin 13) a voltage source of +5.0 ± 0.5 V, with 10 mA sourcing current capability.

e. After a t_D delay (10μs), apply only one V_{OUT} pulse to the output to be programmed. Program one output at a time.

f. After a t_D delay (10μs), raise FE_2 (pin 11) from GND to +5.0 ± 0.5 V for 1 ms, and return to GND.

g. After a t_D delay (10 μs), remove the V_{OUT} pulse from the programmed output.

h. Programming a fuse will cause the output to go to a high level logic in the verify mode. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OUT} pulses to each output to be programmed allowing a delay to t_D between pulses as shown on figure 7c.

i. Repeat 4.9.2c through 4.9.2h for all other bits to be programmed.

j. To verify programming after a t_D (10 µs) delay, return FE_1 to GND. Raise V_{CC} to V_{CCH}. The programmed output should remain in the high state. Again lower V_{CC} to V_{CCL} and verify that the programmed output remains in the high state.

k. For class S and B devices, if any bit does not verify as programmed it shall be considered a programming reject.

TABLE IVC. Programming characteristics for circuits C and H.

Parameter	Symbol	Conditions	Limits			Unit
			Min	Recommended	Max	
Programming voltage to V_{CC}	V_{CCP} 1/	I_{CCP} = 375 ±75 mA Transient or steady-state	8.5	8.75	9.0	V
Verification upper limit	V_{CCH}		5.3	5.5	5.7	V
Verification lower limit	V_{CCL}		4.3	4.5	4.7	V
Verify threshold	V_S 2/		1.4	1.5	1.6	V
Programming supply current	I_{CCP}	V_{CCP} = 8.75 ±0.25 V	300		450	mA
Input voltage, high level "1"	V_{IH}		2.4		5.5	V
Input voltage, low level "0"	V_{IL}		0	0.4	0.8	V
Input current	I_{IH}	V_{IH} = 5.5 V			50	µA
Input current	I_{IL}	V_{IL} = 0.4 V			-500	µA
Output programming voltage	V_{OUT} 3/	I_{OUT} = 200 ±20 mA Transient or steady-state	16	17	18	V
Output programming current	I_{OUT}	V_{OUT} = 17 ±1 V	180	200	220	mA
Programming voltage transition time	t_{TLH}		10		50	µs
$\overline{CE}$ programming pulse width	t_P		300	400	500	µs
Pulse sequence delay	t_D		10			µs

1/ Bypass V_{CC} to GND with a 0.01 µF capacitor to reduce voltage spikes.

2/ V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

3/ Care should be taken to insure the 17 ±1 V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

4.10 Programming procedure for circuit D. The waveforms on figure 7d, the programming characteristics of table IVD, and the following procedures shall apply:

a. Connect the device in the electrical configuration for programming.

b. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.

c. Disable the chip by applying V_{IH} to the $\overline{CE}_1$ and $\overline{CE}_2$ inputs and V_{IL} to the CE_3 and CE_4 inputs. The chip enable input is TTL compatible.

d. After a delay of t_D, apply only one V_{OUT} pulse with a duration of t_p to the ouput selected for programming. The other outputs may be left open or tied to V_{IH}. The outputs shall be programmed one output at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.

e. Other bits in the same word may be programmed sequentially by applying V_{OUT} pulses to each output to be programmed.

f. Repeat 4.10b through 4.10e for all other bits to be programmed.

g. Enable the chip by applying V_{IL} to the $\overline{CE}_1$ and $\overline{CE}_2$ inputs and V_{IH} to the CE_3 and CE_4 inputs and verify the program.

h. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVD. Programming characteristics for circuit D.

Parameter	Symbol	Conditions 1/	Limits			Unit
			Min	Recommended	Max	
V_{CC} required during programming	V_{CCP}		4.75	5.0	5.25	V
Verification V_{CC} read	V_{CCL}	Programming read verify	4.2	4.4	5.0	V
Input voltage, high level "1"	V_{IH}	Do not leave inputs open	2.4	5.0	5.0	V
Input voltage, low level "0"	V_{IL}	Do not leave inputs open	0	0	0.4	V
Output programming voltage	V_{OUT}	Applied to output to be programmed	20	20.5	21	V
Output programming current	I_{OUT}	If pulse generator is used, set current limit to the max value			100	mA
Programming voltage transition time	t_{TLH}		0.5	1.0	3.0	µs
Programming pulse width	t_P		50	100	180	µs
Programming duty cycle	D. C.	Maximum duty cycle to maintain T_A < +85°C		20	20	%
Required delay between disabling memory output and application of output programming pulse	t_D		30			ns

1/ Recommended T_A = +25°C; maximum T_A = +85°C.

4.11 Programming procedure for circuit F. The waveforms on figure 7f, the programming characteristics on table IVF, and the following procedures shall apply:

a. Connect the device in the electrical configuration for programming.

b. Raise V_{CC} to 5.5 Volts.

c. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.

d. Disable the chip by applying V_{IH} to the $\overline{CE}$ inputs and V_{IL} to the CE inputs. The chip enable inputs are TTL compatible.

e. Apply the V_{PP} pulse to the programming pin $\overline{CE}_2$. In order to insure that the output transistor is off before increasing voltage on the output pin, the programming pin's voltage pulse shall precede the output pin's programming pulse by TD_1 and leave after the programming pin's programming pulse by TD_2 (see figure 7f).

f. Apply only one V_{OUT} pulse with duration of t_P to the output selected for programming. The outputs shall be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.

g. Other bits in the same word may be programmed sequentially by applying V_{OUT} pulses to each output to be programmed.

h. Repeat steps 4.11c through 4.11g for all other bits to be programmed.

i. Enable the chip by applying V_{IL} to the $\overline{CE}$ inputs and V_{IH} to the CE inputs, and verify the program. Verification may check for a low output by requiring the device to sink 12 mA at V_{CC} = 4.0 V and 0.2 mA at V_{CC} = 7.0 V at T_A = 25°C.

j. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVF. Programming characteristics for circuit F – Continued.

Parameter	Symbol	Conditions	Limits 1/			Unit
			Min	Recommended	Max	
V_{CC} required during programming	V_{CCP}		5.4	5.5	5.6	V
Rise time of programming pulse data out or programming pin	t_{TLH}		0.34	0.40	0.46	V/µs
Programming voltage on programming pin	V_{PP}		32.5	33	33.5	V
Output programming voltage	V_{OUT}		25.5	26	26.5	V
Programming pin pulse width ($\overline{CE}$)	t_{PP}	Chip disabled, V_{CC} = 5.5 V		100	180	ns
Pulse width of programming voltage	t_P	Chip disabled, V_{CC} = 5.5 V	1		40	µs
Required current limit of power supply feeding programming pin and output during programming	I_L	V_{PP} = 33 V, V_{OUT} = 26 V, V_{CC} = 5.5 V	240			mA
Required time delay between disabling memory output and application of output programming pulse	T_{D1}	Measured at 10% levels	70	80	90	µs
Required time delay between removal of programming pulse and enabling memory output	T_{D2}	Measured at 10% levels	100	----	----	ns
Output current during verification	I_{OLV1}	Chip enabled, V_{CC} = 4.0 V	11	12	13	mA
	I_{OLV2}	Chip enabled, V_{CC} = 7.0 V	0.19	0.2	0.21	mA
Address input voltage	V_{IH}		2.4	5.0	5.5	V
	V_{IL}		0.0	0.4	0.8	V
Maximum duty cycle during automatic programming of program pin and output pin	D. C.	t_P / t_C	----	----	25	%

1/ T_A = +25°C.

4.12 Programming procedure for circuit G. The programming characteristics on table IVG and the following procedures shall be used for programming:

a. Connect the device in the electrical configuration for programming. The waveforms on figure 7g and the programming characteristics of table IVG shall apply to these procedures.

b. Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more 'active low' chip Enable inputs. NOTE: Address and enable inputs must be driven with TTL logic levels during programming and verification.

c. Increase V_{CC} from nominal to V_{CCP} (10.5 ±0.5 V) with a slew rate limit of I_{RR} (1.0 to 10.0 V/μs). Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0 volts.

d. Select the output where a logical high is desired by raising that output voltage to V_{OP} (10.5 ±0.5 V). Limit the slew rate to I_{RR} (1.0 to 10.0 V/μs). This voltage change may occur simultaneously with the V_{CC} increase to V_{CCP}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kΩ minimum (remember that the outputs of the device are disabled at this time).

e. Enable the device by taking the chip Enable(s) to a low level. This is done with a pulse PWE for 10 μs. The 10 μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.

f. Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 5.0 (±0.25 V). The device must be enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits.

g. If the device is not to be tested for V_{OH} over the entire operating range subsequent to programming, the verification of Step f is to be performed at a V_{CC} level of 4.0 volts (±0.2 V). V_{OH}, during the 4 volt verification, must be at least 2.0 volts. The 4 volt V_{CC} verification assures minimum V_{OH} levels over the entire operating range.

h. Repeat steps 4.12b through 4.12f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25 percent. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

i. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject.

TABLE IVG. Programming characteristics for circuit G.

Parameter	Symbol	Conditions	Limits 1/			Unit
			Min	Recommended	Max	
Required V_{CC} during programming	V_{CCP}		10.0	10.5	11.0	V
I_{CC} during programming	I_{CCP}	V_{CC} = 11 V			750	mA
Required output voltage for programming	V_{OP}		10.0	10.5	11.0	V
Output current while programming	I_{OP}	V_{OUT} = 11 V			20	mA
Rate of voltage change of V_{CC} or output	I_{RR}		1.0		10.0	V/µs
Programming pulse width (Enabled)	PWE		9	10	11	µs
Required V_{CC} for verification	V_{CCV}		3.8	4.0	4.2	V
Maximum duty cycle for V_{CC} at V_{CCP}	MDC			25	25	%
Address set-up time	t_1		100			ns
V_{CCP} set-up time	t_2	2/	5			µs
V_{CCP} hold time	t_5		100			ns
V_{OP} set-up time	t_3		100			ns
V_{OP} hold time	t_4		100			ns

1/ T_A = +25°C.

2/ V_{CCP} set-up time may be greater than 0 if V_{CCP} rises at the same rate or faster than V_{OP}.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. PIN and compliance identifier, if applicable (see 1.2).

c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

d. Requirements for certificate of compliance, if applicable.

e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.

f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

g. Requirements for product assurance options.

h. Requirements for special lead lengths, or lead forming, if applicable. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

i. Requirement for programming the device, including processing option. The device may be programmed pre- or post-burn-in, if applicable.

j. Requirements for "JAN" marking.

k. Packaging Requirements (see 5.1)

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA LAND AND MARITIME-VQ, 3990 E. Broad Street, Columbus, Ohio 43218-3990.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

GND ..... Ground zero voltage potential.
V_{IN} ..... Voltage level at an input terminal
V_{IC} ..... Input clamp voltage
I_{IN} ..... Current flowing into an input terminal

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.4). Longer length leads and lead forming should not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.8.1) and programmed by the maintenance activity, except where use quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry Type	Circuit Designator	Fusible Links	Symbol/ FSCM no.
01	7640/Harris Corporation	A	NiCr	CDWO/34371
01	5340-1/Monolithic Memories, Inc.	B	NiCr	CECD/50364
01	82S140/Signetics Corporation	C	NiCr	CDKB/18324
01	82S140/ e2v aerospace & defense, inc.	C	ZVE	0C7V7
01	93438/Fairchild Corporation	D	NiCr	CFJ/07263
01	54S475/National Semiconductor	G	TiW	CCXP/27014
02	7641/Harris Corporation	A	NiCr	----
02	5341-1/Monolithic Memories, Inc.	B	NiCr	----
02	82S141/Signetics Corporation	C	NiCr	----
02	82S141/e2v aerospace & defense, inc.	H	ZVE	0C7V7
02	93448/Fairchild Corporation	D	NiCr	----
02	54S474/National Semiconductor	G	TiW	----
03	82S115/Signetics Corporation	C	NiCr	----
03	82S115/ e2v aerospace & defense, inc.	C	ZVE	0C7V7
04	5348-1/Monolithic Memories, Inc.	B	NiCr	----
04	54S473/National Semiconductor	G	TiW	----
05	5349-1/Monolithic Memories, Inc.	B	NiCr	----
05	29621/Raytheon Company	F	NiCr	CRP/07933
05	54S472/National Semiconductor	G	TiW	----

6.8 Change from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extent of the changes.

Custodians:
Army - CR
Navy - EC
Air Force - 85
DLA - CC

Preparing activity:
DLA - CC

Review activities:
Army – SM, MI
Navy - AS, CG, MC, SH
Air Force – 03, 19, 99

(Project 5962-2013-005)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organization and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.

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