INCH POUND

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MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, CMOS 4096 BIT STATIC RANDOM ACCESS MEMORY (RAM) MONOLITHIC SILICON

Inactive for new design after 24 July 1995.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF-38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS static, 4096-bit random access memories. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device type. The device type is as follows:

Device type	Circuit organization	Address access time
01, 03 (T_C = -55°C "instant-on" to +125°C) 1/	4096 words / 1-bit	t_{AVQV} = 35 ns, 55 ns
02, 04 (T_C = -55°C "instant-on" to +125°C) 1/	1024 words / 4-bit	t_{AVQV} = 35 ns, 55 ns

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
V	GDIP1-T18, CDIP2-T18	18	Dual in line package
X	See figure 1	18	flat package
Y	GDFP2-F18	18	flat package
3	CQCC3-N18	18	Rectangular leadless chip carrier

1/ $T_C = T_A$ at test time equals zero. "Instant-on" is defined as all functional characteristics guaranteed at all temperatures 50 ms after power is applied.

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to bipolar@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil.

AMSC N/A FSC 5962

1.3 Absolute maximum ratings.

Voltage on any pin with respect to ground 2/ .... -0.5 V dc to +7.0 V
Storage temperature range .... -65°C to +150°C
Power dissipation (P_D) .... 1.0 mW
Lead temperature (soldering, 5 seconds) .... +270°C
Maximum junction temperature (T_J) 3/ .... +150°C
Thermal resistance, junction-to-case (θ_{JC}) ....
Cases V, Y and 3 (See MIL-STD-1835)
Case X.. 55°C/W 4/
Maximum dc output current .... 20 mA

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}-V_{SS}) .... 4.5 V dc to 5.5 V dc
High level input voltage (V_{IH}) (all inputs).......................... 2.0 V dc to 6.0 V dc (device 01, 02)
High level input voltage (V_{IH}) (all inputs).......................... 2.0 V dc to V_{CC} (device 03, 04)
Low level input voltage (V_{IL}) (all inputs)........................... -3.0 V dc to +0.8 V dc
Operating case temperature (T_C)................................... -55°C to +125°C

Operating Condition	DeviceType 01			Device Type 02			Device Type 03			Device Type 04		
	Min	Max	Units	Min	Max	Units	Min	Max	Units	Min	Max	Units
Read Cycle Time (t_{AVAV})	35		ns	35		ns	55		ns	55		ns
Address access time (t_{AVQV})		35	ns		35	ns		55	ns		55	ns
Chip select access time (t_{ELQV})		35	ns		35	ns		55	ns		65 8/	ns
Output hold time from address change (t_{AVQX})	5		ns	0		ns	5		ns	5		ns
Chip select to output in low Z (t_{ELQL}) 5/ 6/	5		ns	10		ns	5		ns	10		ns
Chip deselect to output in high Z (t_{EHQZ}) 5/ 6/	0	30	ns	0	20	ns	0	30	ns	0	20	ns
Chip select to power up time (t_{ELPU})	0		ns	0		ns	0		ns	0		ns
Chip deselect to power down time (t_{EHPD})		20	ns		30	ns		20	ns		30	ns
Write cycle time (t_{AVAV})	35		ns	35		ns	55		ns	55		ns
Pulse width, chip select to end of write (t_{ELWH}) 7/	35		ns	30		ns	45		ns	50		ns
Address valid to end of write (t_{AVWH})	35		ns	30		ns	45		ns	50		ns
Pulse width, write (t_{WLWH})	20		ns	30		ns	25		ns	40		ns
Data valid to end of write (t_{DVWH})	20		ns	20		ns	25		ns	20		ns
Address set up to write start (t_{AVWL})	0		ns	0		ns	0		ns	0		ns
Write recovery time (t_{WHAX})	0		ns	5		ns	10		ns	5		ns
Data hold from write end (t_{WHDX})	10		ns	0		ns	10		ns	0		ns
Write enabled to output in high Z (t_{WLQZ}) 6/	0	20	ns	0	10	ns	0	25	ns	0	20	ns
Output active from end of write (t_{WHQX}) 6/ 7/	0		ns	0		ns	0		ns	0		ns

2/ Under absolute maximum ratings, the voltage values are with respect to the most negative supply voltage, V_{SS}. Throughout the remainder of this specification, the voltage values are with respect to V_{SS}.
3/ Maximum junction temperature (T_J) may be increased to 175°C during the burn in and steady state life test.
4/ When a thermal resistance value is included in MIL-STD-1835, it will supersede the value stated herein.
5/ At any given temperature and voltage condition, t_{ELQL} maximum is less than t_{EHQZ} minimum both for a given device and from device to device.
6/ Tansition is measured ± 500 mV from steady state voltage with specified loading.
7/ The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
8/ Chip deselected less than 55 ns prior to selection.

2.0 APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and standards. The following specifications and standards form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.3.2 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.3.3 Functional tests. The functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be submitted to the qualifying activity for approval.

3.3.4 Truth tables. The truth table shall be as specified on figure 4.

3.3.5 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.3 Screening. Screening shall be in accordance with MIL-PRF-38535, and shall be conducted prior to qualification, and conformance inspection. The following additional criteria shall apply:

a. A cell bit stress test may be used for the special electrical screen test of method 5004. The cell bit stress test shall be conducted per table III test number 42 for device types 01, 03, and test number 54 for device types 02 and 04. The functional test shall be the checkerboard / checkboard algorithm of the appendix. This test shall be performed once at the first high temperature (125°C) functional test only.

b. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

c. Interim and final electrical tests shall be as specified in table II, except interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.

d. Additional screening for space level product shall be as specified in MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ 3/	Device	Limits		Unit
				Min	Max	
Low level input leakage current (all input pins)	I_{IL}	V_{CC} = 5.5 V V_{IN} = GND	All		-10	µA
High level input leakage current (all input pins)	I_{IH}	V_{CC} = 5.5 V V_{IN} = 5.5 V	All		10	µA
Output leakage current	I_{LO}	$\overline{CS}$ = V_{IH}, V_{CC} = 5.5 V V_{OUT} = GND to 5.5 V	All		±50	µA
Power supply current	I_{CC}	V_{CC} = 5.5 V $\overline{CS}$ = V_{IL}, outputs open	01,02		110	mA
			03,04		140	mA
Standby current	I_{SB}	V_{CC} = 4.5 V to 5.5 V CS = V_{IH}	01,02		10	mA
			03		25	mA
			04		30	mA
Output low voltage	V_{OL}	I_{OL} = 12.0 mA V_{IL} = 0.8 V V_{IH} = 2.0 V V_{CC} = 4.5 V	01,03		0.4	V
		I_{OL} = 8.0 mA	02,04		0.4	V
Output high voltage	V_{OH}	V_{IL} = 0.8 V V_{IH} = 2.0 V V_{CC} = 4.5 V I_{OH} = - 4.0 mA	All	2.4		V
Output short circuit current 4/, 5/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = GND	All		-350	mA
Input capacitance	C_{IN}	V_{IN} = 0 V, f = 1 MHz T_C = 25°C	All		5	pF
Output capacitance	C_0	V_{IN} = 0 V, f = 1 MHz T_C = 25°C	All		7	pF
Peak power on 5/	I_{PO}	V_{CC} = 4.5 V, $\overline{CS}$ = 2.4 V	All		10	mA
Read cycle time 2/	t_{AVAV}	See table III and figure 5	01,02	35		ns
			03,04	55		ns
Address access time	t_{AVQV}		01,02		35	ns
			03,04		55	ns
Chip select access time 3/	t_{ELQV}		01,02		35	ns
			03		55	ns
			04 6/		65	ns
Chip select to output in low Z 5/ 7/	t_{ELQX}		01,03	5		ns
			02,04	10		ns
Chip deselect to output in high Z 5/ 7/	t_{EHQZ}		01,03	0	30	ns
			02,04	0	20	ns
Output hold from address change	t_{AVQX}		01,03,04	5		ns
			02	0		ns
Chip select to power up time 5/	t_{ELPU}		All	0		ns
Chip deselect to power down time 5/	t_{EHPD}		01,03		20	ns
			02,04		30	ns
Write cycle time	t_{AVAV}		01,02	35		ns
			03,04	55		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ 2/ 3/	Device	Limits		Unit
				Min	Max	
Chip select to end of write	t_{ELWH}	See table III and figure 5	01	35		ns
			02	30		ns
			03	45		ns
			04	50		ns
Address valid to end of write	t_{AVWH}		01	35		ns
			02	30		ns
			03	45		ns
			04	50		ns
Address setup time	t_{AVWL}		All	0		ns
Write pulse width	t_{WLWH}		03	25		ns
			04	40		ns
			01	20		ns
			02	30		ns
Write recovery time	t_{WHAX}		01	0		ns
			02,04	5		ns
			03	10		ns
Data valid to end of write	t_{DVWH}		01,02,04	20		ns
			03	25		ns
Data hold time	t_{WHDX}		01,03	10		ns
			02,04	0		ns
Write enable to output in high Z 7/, 5/	t_{WLQZ}		01,04	0	20	ns
			02	0	10	ns
			03	0	25	ns
Output active from end of write 7/, 5/	t_{WHQX}		All	0		ns

1/ Output levels are tested in static state and are specified over voltage range of V_{CC}.

2/ Unless otherwise specified, the dynamic load shall be in accordance with figure 5 (load A).

3/ Complete terminal conditions are as specified in table III.

4/ Duration not to exceed 1 second.

5/ Not tested.

6/ Chip deselected for a finite time that is less than 55 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access occurs according to Read Cycle No. 1.)

7/ Transition is measured $\pm$ 500 mV from steady state voltage using figure 5 (load B).

4.4 Technology Conformance Inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Electrical test requirements shall be in accordance with table II herein.
b. Subgroups 5 and 6 shall be omitted.
c. Subgroups 4 (C_{in}, C_o measurement) shall be measured only for initial qualification and after process or design changes which may affect input and output capacitance. Capacitance shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz and a signal amplitude not to exceed 50 mV rms. Perform C_{in} and C_o parameter measurements to table I limits.

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III)	
	Class S devices 1/	Class B Devices 1/
Interim electrical parameters	2, 8 *	2, 8 *, 10
Final electrical test parameters	1**, 2, 3, 7**, 8	1**, 2, 3, 7**, 8*, 10, 11
Group A test requirements	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8*, 9, 10, 11
Group B end point electrical test parameters when using the method 5005 QCI option.	1, 2, 3, 7, 8, 9, 10, 11	N/A
Group C end-point electrical parameters	1, 2, 3, 7, 8, 9, 10, 11	2, 10
Group D end-point electrical parameters	1, 2, 3, 7, 8	2, 10

* Maximum temperature only.
** PDA applies to subgroups 1 and 7
1/ For subgroup 4, see 4.4.1c.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535 and as follows.

a. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883 method 3015. The option to categorize devices as ESD sensitive without performing the test is not allowed. Device types categorized as ESD sensitive shall be further tested using method 3015 modified as follows:

(1) For use in this specification method 3015 table I pin combination number (4) shall be “input (B) to V+ A)” and combination number (5) shall be “output (B) to V+ (A)”.

(2) The reverse polarity procedure shall be applicable to all pin combinations.

(3) Only those device types that pass ESDS testing at 1,000 volts or greater shall be considered as conforming to the requirements of this specification.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End-point electrical tests shall be as specified in table II herein.

b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of Inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 Life test, burn in, cool down, and electrical test procedure. When devices are measured at 25°C following application of the life or burn in test condition, all devices shall be cooled to 35°C prior to removal of bias voltages.

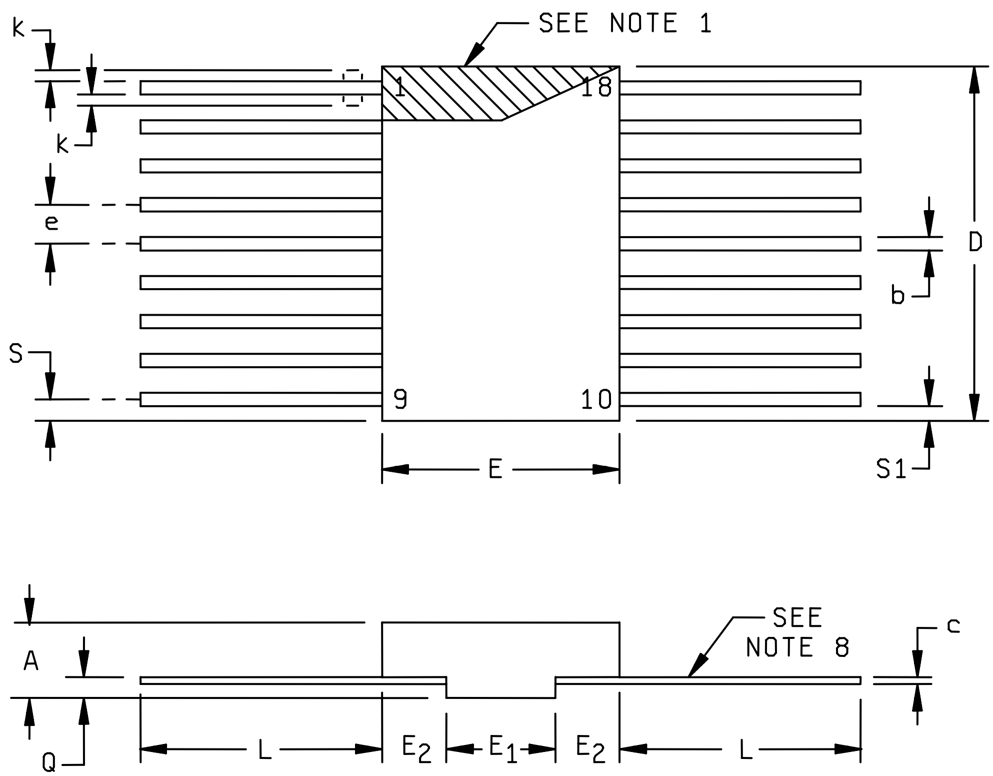


FIGURE 1. Case outline X (18 lead, ¼” x ½” flat package).

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.045	.092	1.14	2.34	
b	.015	.019	0.38	0.48	5
c	.003	.007	0.08	0.18	5
D		.455		11.56	3
E	.295	.320	7.49	8.13	
E1	.130	.150	3.3	3.81	
E2	.030		0.76		
e	.050 BSC		1.27 BSC		4, 6
k	.005	.018	0.13	0.46	9
L	.250	.370	6.35	9.40	
Q	.010	.040	0.25	1.02	2
S		.045		1.14	7
S1	.005		0.13		

NOTES:

1. Index area, A notch or A pin identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternatively, a tab (dim k) may be used to identify pin one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body. Dimension Q shall be .0085 inch (0.22 mm) minimum when lead finish A is applied.
3. This dimension allows for off center lid, meniscus and glass overrun.
4. The basic pin spacing is .050 inch (1.27 mm) between centerlines. Each pin centerline shall be located within ± .005 inch (0.13 mm) of its exact longitudinal position relative to pins 1 and 18.
5. All leads – increase maximum limit by .003 inch (0.08 mm) measured at the center of the flat, when lead finish A or B is applied.
6. Sixteen spaces.
7. Applies to all four corners (leads number 1, 9, 10, and 18).
8. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
9. Optional, see note 1. If a pin 1 identification mark is used in addition to this tab, the minimum limit of dimension K does not apply.

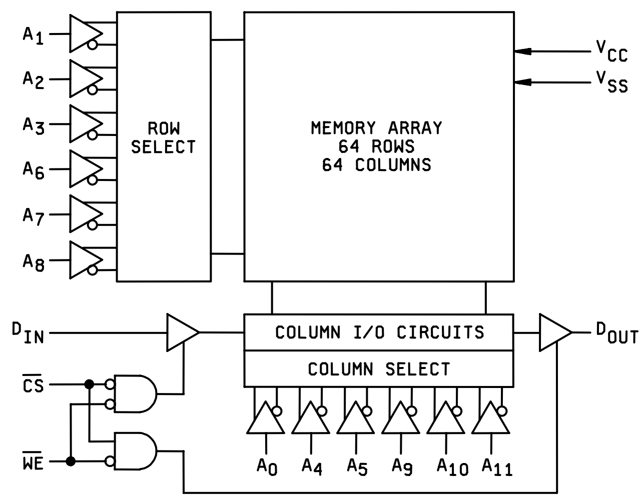
FIGURE 1. Case outline X (18 lead, ¼" x ½" flat package) – Continued.

Pin Number Case V, X, Y, and 3	Device Type 01 and 03
1	A_0
2	A_1
3	A_2
4	A_3
5	A_4
6	A_5
7	D_{OUT}
8	$\overline{WE}$
9	V_{SS}
10	$\overline{CS}$
11	D_{IN}
12	A_{11}
13	A_{10}
14	A_9
15	A_8
16	A_7
17	A_6
18	V_{CC}

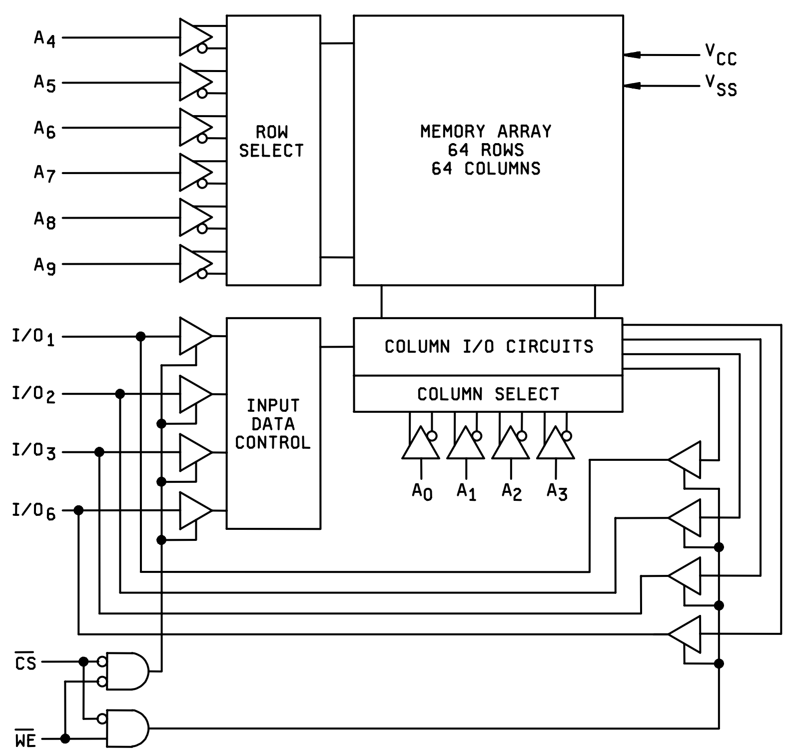
Pin Number Case V, X, Y, and 3	Device Type 02 and 04
1	A_6
2	A_5
3	A_4
4	A_3
5	A_0
6	A_1
7	A_2
8	$\overline{CS}$
9	V_{SS}
10	$\overline{WE}$
11	I/O_4
12	I/O_3
13	I/O_2
14	I/O_1
15	A_9
16	A_8
17	A_7
18	V_{CC}

FIGURE 2. Terminal connections.

DEVICE TYPES 01 AND 03



DEVICE TYPES 02 AND 04



NOTE: Address numbering may vary between vendors.

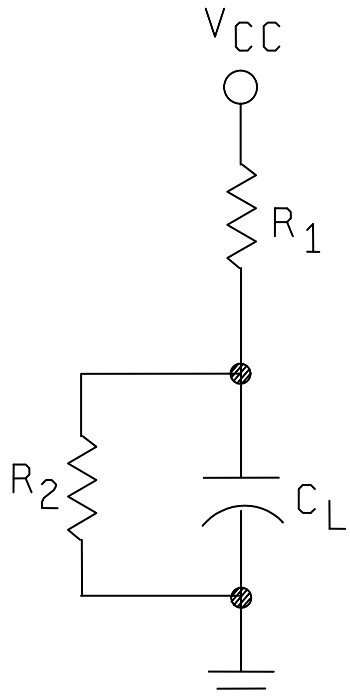
FIGURE 3. Block diagrams.

Device types 01, 02, 03 and 04

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power	I/O
H	X	Not selected	High Z	Stand by	High Z
L	L	Write	High Z	Active	D_{IN}
L	H	Read	D_{OUT}	Active	D_{OUT}

H = High voltage level.
L = Low voltage level.
X = Don't care (high or low).

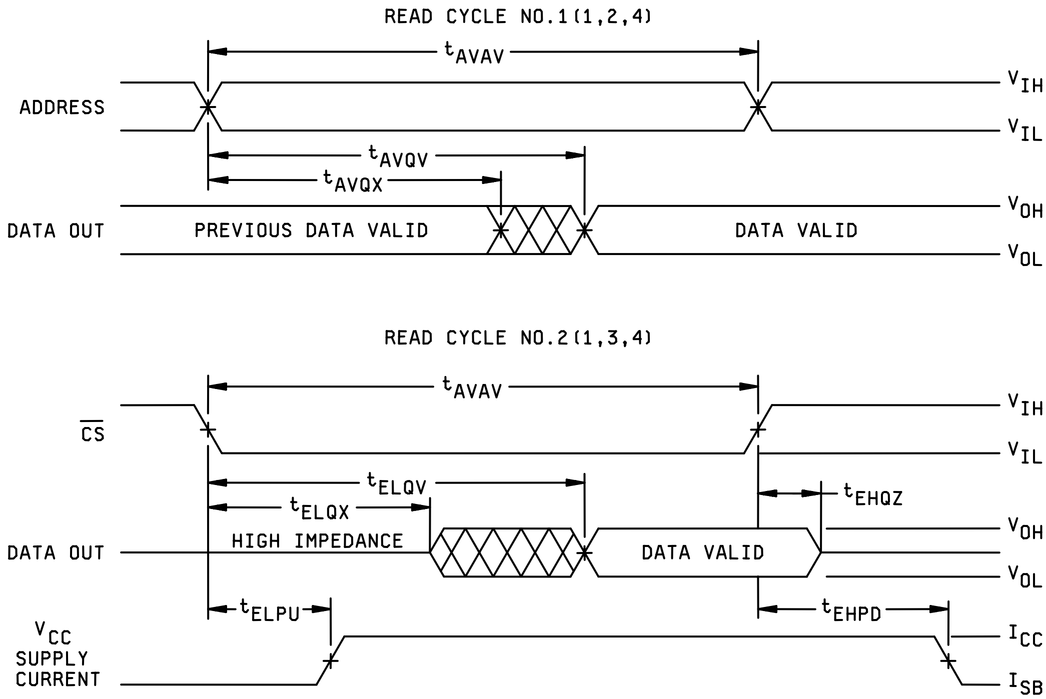
FIGURE 4. Truth table.



Device types 01, 02, 03, and 04

NOTES:
1. V_{CC} is defined in table III.
2. Load A: (including probe and jig capacitance)
   R_1 = 481 Ω ±5%; R_2 = 255 Ω ±5%; C_L = 30 pF (device 02 and 04)
   R_1 = 329 Ω ±5%; R_2 = 202 Ω ±5%; C_L = 30 pF (device 01 and 03)
3. Load B: (Including probe and jig capacitance)
   R_1 = 481 Ω ±5%; R_2 = 255 Ω ±5%; C_L = 5 pF (device 02 and 04)
   R_1 = 329 Ω ±5%; R_2 = 202 Ω ±5%; C_L = 5 pF (device 01 and 03)

FIGURE 5. Load circuit and timing diagram.



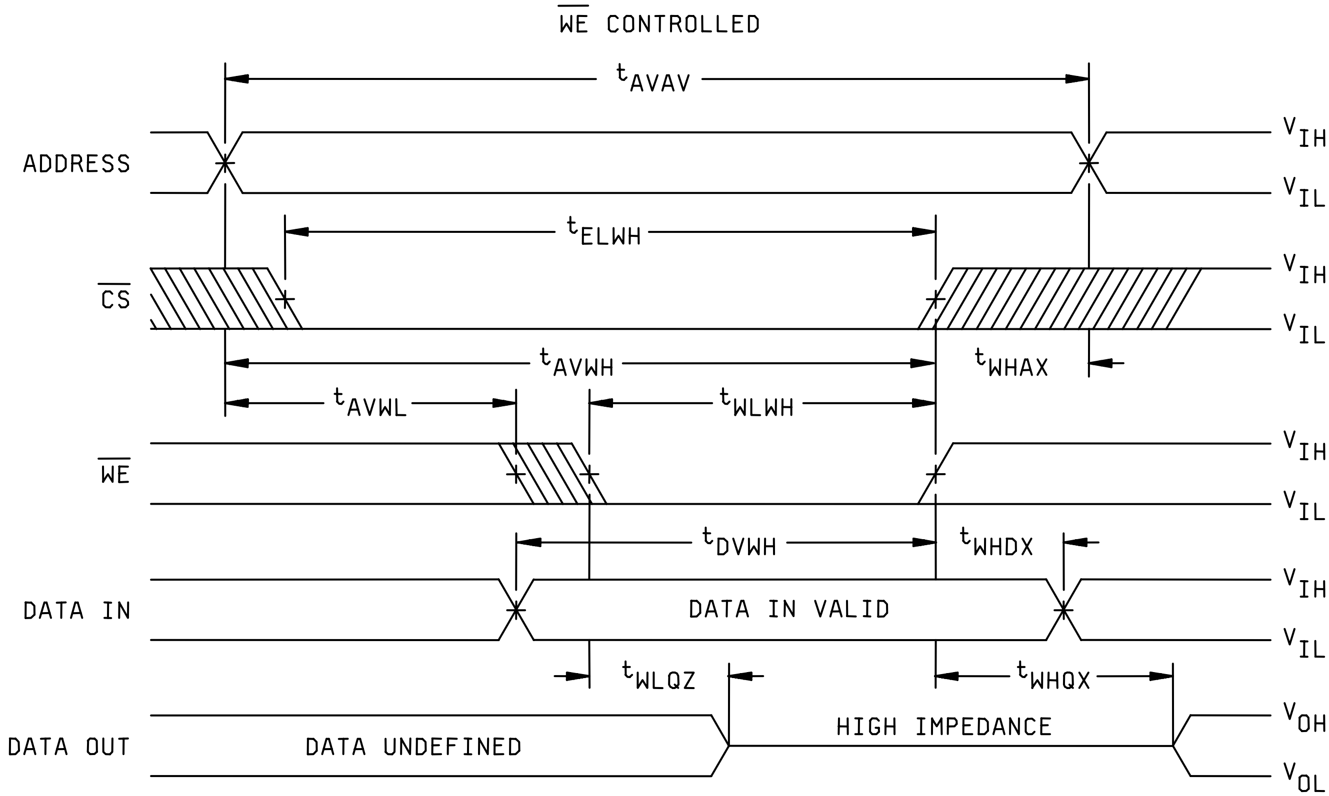
WAVEFORMS

NOTES:

1. $\overline{WE}$ is high for read cycles.
2. Device is continuously selected, $\overline{CS}$ transition low.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. See table 1 for limits and complete terminal conditions.
5. Input and output timing reference levels are 1.5 volts with input pulse levels of ground to 3.0 volts.
6. t_{ELQX} and t_{EHQZ} are measured at ± 500 mV from steady state with 5 pF load.

Read cycle waveforms and test conditions for device types 01,02, 03, and 04

FIGURE 5. Load circuit and timing diagram - Continued.



WAVEFORMS

NOTES:
1. See table I for limits and complete terminal conditions.
2. Input and output timing reference levels are 1.5 volts with input pulse levels of ground to 3.0 volts.
3. t_{WHQX} and t_{WLQZ} are measured at ±500 mV from steady state with 5 pF load.

Write cycle waveforms and test conditions for device types 01, 02, 03, and 04

FIGURE 5. Load circuit and timing diagram - Continued.

TABLE III. Group A inspection for device types 01 and 03.
Terminal conditions (Outputs not designated are open or resistive coupled to GND or voltages;
Inputs not designated are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 3,V,X,Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorith 1/
			Test no.	A0	A1	A2	A3	A4	A5	D_{OUT}	$\overline{WE}$	V_{SS}	$\overline{CS}$	D_{IN}	A11	A10	A9	A8	A7	A6	V_{CC}	
1	V_{OH}	3006	1	2/	2/	2/	2/	2/	2/	-4 mA	4.5 V	GND	GND	2/	2/	2/	2/	2/	2/	2/	4.5 V	
T_C=+25°C	V_{OL}	3007	2	3/	3/	3/	3/	3/	3/	12 mA	4.5 V	“	“	3/	3/	3/	3/	3/	3/	3/	4.5 V	
	I_{IH}	3010	3	5.5 V	GND	GND	GND	GND	GND		GND	“	GND	GND	GND	GND	GND	GND	GND	GND	5.5 V	
			4	GND	5.5 V	GND	“	“	“		“	“	“	“	“	“	“	“	“	“	“	
			5	“	GND	5.5 V	“	“	“		“	“	“	“	“	“	“	“	“	“	“	
			6	“	“	GND	5.5 V	“	“		“	“	“	“	“	“	“	“	“	“	“	
			7	“	“	“	GND	5.5 V	“		“	“	“	“	“	“	“	“	“	“	“	
			8	“	“	“	“	GND	5.5 V		“	“	“	“	“	“	“	“	“	“	“	
			9	“	“	“	“	“	GND		5.5 V	“	“	“	“	“	“	“	“	“	“	
			10	“	“	“	“	“	“		GND	“	5.5 V	“	“	“	“	“	“	“	“	
			11	“	“	“	“	“	“		“	“	GND	5.5 V	“	“	“	“	“	“	“	
			12	“	“	“	“	“	“		“	“	“	GND	5.5 V	“	“	“	“	“	“	
			13	“	“	“	“	“	“		“	“	“	“	GND	5.5 V	“	“	“	“	“	
			14	“	“	“	“	“	“		“	“	“	“	“	GND	5.5 V	“	“	“	“	
			15	“	“	“	“	“	“		“	“	“	“	“	“	GND	5.5 V	“	“	“	
			16	“	“	“	“	“	“		“	“	“	“	“	“	“	GND	5.5 V	“	“	
			17	“	“	“	“	“	“		“	“	“	“	“	“	“	“	GND	5.5 V	“	
	I_{IL}	3009	18	“	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		5.5 V	“	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	
			19	5.5 V	GND	5.5 V	“	“	“		“	“	“	“	“	“	“	“	“	“	“	
			20	“	5.5 V	GND	“	“	“		“	“	“	“	“	“	“	“	“	“	“	
			21	“	“	5.5 V	GND	“	“		“	“	“	“	“	“	“	“	“	“	“	
			22	“	“	“	5.5 V	GND	“		“	“	“	“	“	“	“	“	“	“	“	
			23	“	“	“	“	5.5 V	GND		“	“	“	“	“	“	“	“	“	“	“	
			24	“	“	“	“	“	5.5 V		GND	“	“	“	“	“	“	“	“	“	“	
			25	“	“	“	“	“	“		5.5 V	“	GND	“	“	“	“	“	“	“	“	
			26	“	“	“	“	“	“		“	“	5.5 V	GND	“	“	“	“	“	“	“	
			27	“	“	“	“	“	“		“	“	“	5.5 V	GND	“	“	“	“	“	“	
			28	“	“	“	“	“	“		“	“	”	“	5.5 V	GND	“	“	“	“	“	
			29	“	“	“	“	“	“		“	“	“	“	“	5.5 V	GND	“	“	“	“	
			30	“	“	“	“	“	“		“	“	“	“	“	“	5.5 V	GND	5.5 V	5.5 V	5.5 V	
			31	“	“	“	“	“	“		“	“	“	“	“	“	“	5.5 V	GND	“	“	
			32	“	“	“	“	“	“		“	“	“	“	“	“	“	5.5 V	5.5 V	GND	“	
	I_{L01*}		33	GND	GND	GND	GND	GND	GND	5.5 V	2.0 V	“	2.0 V	GND	GND	GND	GND	GND	GND	GND	“	
			34	GND	GND	GND	GND	GND	GND	5.5 V	0.8 V	“	“	GND	GND	GND	GND	GND	GND	GND	“	
	I_{L02*}		35	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	2.0 V	“	“	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	“	
			36	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	GND	0.8 V	“	“	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	“	
	I_{SB}		37	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V		GND	“	4.5 V	GND	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	4.5 V	
			38	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V		2.0 V	“	2.0 V	GND	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	5.5 V	
	I_{CC}	3005	39	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V		0.8 V	“	0.8 V	GND	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	5.5 V	
2	Same tests, terminal conditions, and limits as subgroup 1, except T_C = 125°C.																					
3	Same tests, terminal conditions, and limits as subgroup 1, except T_C = -55°C.																					
4	C_{in}	3012	40	6/	6/	6/	6/	6/	6/		6/	GND	6/	6/	6/	6/	6/	6/	6/	6/	GND	
T_C=+25°C	C_0	3012	41							6/		GND									GND	

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 – Continued.
Terminal conditions (Outputs not designated are open or resistive coupled to GND or voltages;
Inputs not designated are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 3,V,X,Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorith 1/
			Test no.	A0	A1	A2	A3	A4	A5	D_{OUT}	$\overline{WE}$	V_{SS}	$\overline{CS}$	D_{IN}	A11	A10	A9	A8	A7	A6	V_{CC}	
BIT STRESS TEST			42	7/	7/	7/	7/	7/	7/	7/	7/	GND	7/	7/	7/	7/	7/	7/	7/	7/	7/	CKBD a $\overline{CKBD}$
7 T_C=+25°C	tAVQV	Fig 5	43	8/	8/	8/	8/	8/	8/	8/	8/	“	8/	8/	8/	8/	8/	8/	8/	8/	4.5 V	“
			44	8/	8/	8/	8/	8/	8/	8/	8/	“	8/	8/	8/	8/	8/	8/	8/	8/	5.5 V	“
			45	9/	9/	9/	9/	9/	9/	9/	9/	“	9/	9/	9/	9/	9/	9/	9/	9/	4.5 V	“
			46	9/	9/	9/	9/	9/	9/	9/	9/	“	9/	9/	9/	9/	9/	9/	9/	9/	5.5 V	“
			47	10/	10/	10/	10/	10/	10/	10/	10/	“	10/	10/	10/	10/	10/	10/	10/	10/	4.5 V	“
			48	10/	10/	10/	10/	10/	10/	10/	10/	“	10/	10/	10/	10/	10/	10/	10/	10/	5.5 V	“
			49	11/	11/	11/	11/	11/	11/	11/	11/	“	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	“
			50	11/	11/	11/	11/	11/	11/	11/	11/	“	11/	11/	11/	11/	11/	11/	11/	11/	5.5 V	“
			51	12/	12/	12/	12/	12/	12/	12/	12/	“	12/	12/	12/	12/	12/	12/	12/	12/	4.5 V	“
			52	12/	12/	12/	12/	12/	12/	12/	12/	“	12/	12/	12/	12/	12/	12/	12/	12/	5.5 V	“
			53	13/	13/	13/	13/	13/	13/	13/	13/	“	13/	13/	13/	13/	13/	13/	13/	13/	4.5 V	“
			54	13/	13/	13/	13/	13/	13/	13/	13/	“	13/	13/	13/	13/	13/	13/	13/	13/	5.5 V	“
	tELQV1		55	14/	14/	14/	14/	14/	14/	14/	14/	“	14/	14/	14/	14/	14/	14/	14/	14/	4.5 V	“
	tELQV2		56	14/	14/	14/	14/	14/	14/	14/	14/	“	14/	14/	14/	14/	14/	14/	14/	14/	5.5 V	“
	tELQV1		57	14/	14/	14/	14/	14/	14/	14/	14/	“	14/	14/	14/	14/	14/	14/	14/	14/	4.5 V	MARC
	tELQV2		58	14/	14/	14/	14/	14/	14/	14/	14/	“	14/	14/	14/	14/	14/	14/	14/	14/	5.5 V	MARC
8	Same tests, terminal conditions, and limits as subgroup 7, except T_C = 125°C and -55°C.																					
9 T_C=+25°C	tAVQV	Fig 5	59	15/	15/	15/	15/	15/	15/	15/	15/	GND	15/	15/	15/	15/	15/	15/	15/	15/	4.5 V	GALPA and GALRE
			60	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tELQV1		61	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			62	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tELQV2		63	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			64	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tAVAV		65	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			66	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tELWH		67	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			68	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tAVWH		69	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			70	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tAVWL		71	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			72	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tWLWH		73	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			74	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tWHAX		75	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			76	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tDVWH		77	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			78	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 – Continued.
Terminal conditions (Outputs not designated are open or resistive coupled to GND or voltages;
Inputs not designated are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 3,V,X,Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorith 1/
			Test no.	A0	A1	A2	A3	A4	A5	D_{OUT}	$\overline{WE}$	V_{SS}	$\overline{CS}$	D_{IN}	A11	A10	A9	A8	A7	A6	V_{CC}	
9 T_C=+25°C	tWHDX	Fig 5	79 80	15/ "	15/ "	15/ "	15/ "	15/ "	15/ "	15/ "	15/ "	GND "	15/ "	15/ "	15/ "	15/ "	15/ "	15/ "	15/ "	15/ "	4.5 V 5.5 V	GALP and GALRE
	tAVQX		81 82	" "	" "	" "	" "	" "	" "	" "	" "	" "	" "	" "	" "	" "	" "	" "	" "	" "	4.5 V 5.5 V	GALP and GALRE
10	Same tests, terminal conditions, and limits as subgroup 9, except T_C = 125°C.																					
11	Same tests, terminal conditions, and limits as subgroup 9, except T_C = -55°C.																					

See footnotes at end of device types 01 and 03.

1/ See appendix for description of algorithms.

2/ An input preconditioning logic sequence shall be applied that results in a logic “1” at the output to be measured. Logic input levels during measurement shall be: V_{IL} = 0.8 V; V_{IH} = 2.0 V.

3/ An input preconditioning logic sequence shall be applied that results in a logic “0” at the output to be measured. Logic input levels during measurement shall be:

Types 01, 03	V_{IL}	V_{IH}	I_{OL}
	0.8 V	2.0 V	12.0 mA

4/ I_{SB} = 10 mA for device type 01; 25 mA for device type 03. The device manufacturer may at his option do either test or both tests.

5/ I_{CC} = 110 mA for device type 01, 140 mA for device type 03.

6/ See 4.4.1c.

7/ V_{IL} = GND, V_{IH} = 6.0 V, pause time = 250 ms/loop max, $\overline{CS}$ = high, only performed once at 125°C, and V_{CC} = 7.0 V min.

8/ V_{IL} = 0.8 V and V_{IH} = 2.0 V.

9/ Algorithm has 60 ns where chip is deselected between the write.

10/ V_{IL} = GND, V_{IH} = 3.0 V, and all address setup times are at minimums.

11/ V_{IL} = GND, V_{IH} = 3.0 V, and all write pulse timing are at minimums.

12/ V_{IL} = GND, V_{IH} = 3.0 V, and all address ending times are at minimums.

13/ V_{IL} = GND, V_{IH} = 3.0 V, and t_{AVQV} is measured at minimum timing.

14/ V_{IL} = GND, V_{IH} = 3.0 V, t_{ELQV1} and t_{ELQV2} are measured at minimum timing.

15/ V_{IL} = 0.0 V, V_{IH} = 3.0 V, and all parameters are measured at minimum timing.

16/ t_{AVQV} = 35 ns for device type 01; 55 ns for device type 03.

17/ t_{ELQV1} = 35 ns for device type 01; 55 ns for device type 03.

18/ t_{ELQV2} = 35 ns for device type 01; 55 ns for device type 03.

19/ t_{AVAV} = 35 ns for device type 01; 55 ns for device type 03.

20/ t_{ELWH} = 35 ns for device type 01; 45 ns for device type 03.

21/ t_{AVWH} = 35 ns for device type 01; 45 ns for device type 03.

22/ t_{WLWH} = 35 ns for device type 01; 25 ns for device type 03.

23/ t_{WHAX} = 20 ns for device type 01; 10 ns for device type 03.

24/ t_{DVWH} = 20 ns for device type 01; 25 ns for device type 03.

* The device manufacturer may at his option, do either test or both tests.

TABLE III. Group A inspection for device types 02 and 04.
Terminal conditions (Outputs not designated are open or resistive coupled to GND or voltages;
Inputs not designated are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 3,V,X,Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorith 1/
			Test no.	A6	A5	A4	A3	A0	A1	A2	$\overline{CS}$	V_{SS}	$\overline{WE}$	I/04	I/03	I/02	I/01	A9	A8	A7	V_{CC}	
1 T_C=+25°C	V_{OH}	3006	1	2/	2/	2/	2/	2/	2/	2/	GND	GND	3.0 V	2/	2/	2/	2/	2/	2/	2/	4.5 V	
			2	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	
			3	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	
			4	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	
	V_{OL}	3007	5	3/	3/	3/	3/	3/	3/	3/	“	“	“	3/	3/	3/	3/	3/	3/	3/	“	
			6	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	
			7	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	
			8	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	
	I_{IH}	3010	9	5.5 V	GND	GND	GND	GND	GND	GND	GND	“	GND	GND	GND	GND	GND	GND	GND	GND	5.5 V	
			10	GND	5.5 V	GND	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	
			11	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	
			12	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	“	“	“	
			13	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	“	“	
			14	“	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	“	
			15	“	“	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	
			16	“	“	“	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	
			17	“	“	“	“	“	“	“	GND	“	5.5 V	“	“	“	“	“	“	“	“	
			18	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“	“	“	“	“	
			19	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“	“	“	“	
			20	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“	“	“	
			21	“	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“	“	
			22	“	“	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“	
			23	“	“	“	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	
			24	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	
	I_{IL}	3009	25	“	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	“	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	“	
			26	5.5 V	GND	5.5 V	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	
			27	“	5.5 V	GND	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	
			28	“	“	5.5 V	GND	“	“	“	“	“	“	“	“	“	“	“	“	“	“	
			29	“	“	“	5.5 V	GND	“	“	“	“	“	“	“	“	“	“	“	“	“	
			30	“	“	“	“	5.5 V	GND	“	“	“	“	“	“	“	“	“	“	“	“	
			31	“	“	“	“	“	5.5 V	GND	“	“	“	“	“	“	“	“	“	“	“	
			32	“	“	“	“	“	“	5.5 V	GND	“	“	“	“	“	“	“	“	“	“	
			33	“	“	“	“	“	“	“	5.5 V	“	GND	“	“	“	“	“	“	“	“	
			34	“	“	“	“	“	“	“	“	“	5.5 V	GND	“	“	“	“	“	“	“	
			35	“	“	“	“	“	“	“	”	“	“	5.5 V	GND	“	“	“	“	“	“	
			36	“	“	“	“	“	“	“	“	“	“	“	5.5 V	GND	“	“	“	“	“	
			37	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	GND	“	“	“	“	
			38	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	GND	“	“	“	
			39	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	GND	“	“	
			40	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	GND	“	
	I_{L01}		41	GND	GND	GND	GND	GND	GND	GND	2.0 V	“	2.0 V	5.5 V	GND	GND	GND	GND	GND	GND	“	
			42	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	GND	“	“	“	“	“	
			43	“	“	“	“	“	“	“	“	“	“	“	GND	5.5 V	“	“	“	“	“	
			44	“	“	“	“	“	“	“	“	“	“	“	GND	GND	5.5 V	“	“	“	“	
	I_{L02}		45	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	“	“	“	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	“	
			46	“	“	“	“	“	“	“	“	“	“	5.5 V	GND	5.5 V	“	“	“	“	“	
			47	“	“	“	“	“	“	“	“	“	“	“	5.5 V	GND	“	“	“	“	“	
			48	“	“	“	“	“	“	“	“	“	“	“	5.5 V	5.5 V	GND	“	“	“	“	
	I_{CC}	3005	49	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	0.8 V	“	0.8 V	GND	GND	GND	GND	2.0 V	2.0 V	2.0 V	“	
	I_{SB}		50	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	4.5 V	“	GND	GND	GND	GND	GND	2.0 V	2.0 V	2.0 V	4.5 V	
			51	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	“	2.0 V	GND	GND	GND	GND	2.0 V	2.0 V	2.0 V	5.5 V	
2	Same tests, terminal conditions, and limits as subgroup 1, except T_C = 125°C																					
3	Same tests, terminal conditions, and limits as subgroup 1, except T_C = -55°C																					

See footnotes at end of device type 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 – Continued.
Terminal conditions (Outputs not designated are open or resistive coupled to GND or voltages;
Inputs not designated are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 3,V,X,Y Test no.	1 A6	2 A5	3 A4	4 A3	5 A0	6 A1	7 A2	8 $\overline{CS}$	9 V_{SS}	10 $\overline{WE}$	11 I/04	12 I/03	13 I/02	14 I/01	15 A9	16 A8	17 A7	18 V_{CC}	Algorith 1/
4 T_C=+25°C	C_{in}	3012	52	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/					6/	6/	6/	GND	
	C_0	3012	53									“		6/	6/	6/	6/				GND	
BIT STRESS TEST			54	7/	7/	7/	7/	7/	7/	7/	7/	“	7/	7/	7/	7/	7/	7/	7/	7/	7/	CKBD $\overline{\text{CKB}}$
7 T_C=+25°C	tAVQV	Fig 5	55	8/	8/	8/	8/	8/	8/	8/	8/	“	8/	8/	8/	8/	8/	8/	8/	8/	4.5 V	“
			56	8/	8/	8/	8/	8/	8/	8/	8/	“	8/	8/	8/	8/	8/	8/	8/	8/	5.5 V	“
			57	9/	9/	9/	9/	9/	9/	9/	9/	“	9/	9/	9/	9/	9/	9/	9/	9/	4.5 V	“
			58	9/	9/	9/	9/	9/	9/	9/	9/	“	9/	9/	9/	9/	9/	9/	9/	9/	5.5 V	“
			59	10/	10/	10/	10/	10/	10/	10/	10/	“	10/	10/	10/	10/	10/	10/	10/	10/	4.5 V	“
			60	10/	10/	10/	10/	10/	10/	10/	10/	“	10/	10/	10/	10/	10/	10/	10/	10/	5.5 V	“
			61	11/	11/	11/	11/	11/	11/	11/	11/	“	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	“
			62	11/	11/	11/	11/	11/	11/	11/	11/	“	11/	11/	11/	11/	11/	11/	11/	11/	5.5 V	“
			63	12/	12/	12/	12/	12/	12/	12/	12/	“	12/	12/	12/	12/	12/	12/	12/	12/	4.5 V	“
			64	12/	12/	12/	12/	12/	12/	12/	12/	“	12/	12/	12/	12/	12/	12/	12/	12/	5.5 V	“
			65	13/	13/	13/	13/	13/	13/	13/	13/	“	13/	13/	13/	13/	13/	13/	13/	13/	4.5 V	“
			66	13/	13/	13/	13/	13/	13/	13/	13/	“	13/	13/	13/	13/	13/	13/	13/	13/	5.5 V	“
	tELQV1		67	14/	14/	14/	14/	14/	14/	14/	14/	“	14/	14/	14/	14/	14/	14/	14/	14/	4.5 V	“
	tELQV2		68	14/	14/	14/	14/	14/	14/	14/	14/	“	14/	14/	14/	14/	14/	14/	14/	14/	5.5 V	“
	tELQV1		69	14/	14/	14/	14/	14/	14/	14/	14/	“	14/	14/	14/	14/	14/	14/	14/	14/	4.5 V	MARC
	tELQV2		70	14/	14/	14/	14/	14/	14/	14/	14/	“	14/	14/	14/	14/	14/	14/	14/	14/	5.5 V	MARC
8	Same tests, terminal conditions, and limits as subgroup 7, except T_C = 125°C and -55°C.																					
9 T_C=+25°C	tAVQV	Fig 5	71	15/	15/	15/	15/	15/	15/	15/	15/	GND	15/	15/	15/	15/	15/	15/	15/	15/	4.5 V	GALP and GALRE
			72	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tELQV1		73	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			74	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tAVAV		75	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			76	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tWLWH		77	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			78	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tWHAX		79	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			80	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tDVWH		81	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			82	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tELQV2		83	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			84	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tELWH		85	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			86	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tAVWH		87	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			88	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	
	tAVWL		89	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	4.5 V	“
			90	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	“	5.5 V	

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 – Continued.
Terminal conditions (Outputs not designated are open or resistive coupled to GND or voltages;
Inputs not designated are high ≥ 2.0 V, low ≤ 0.8 V or open).

Subgroup	Symbol	MIL-STD-883 method	Cases 3,V,X,Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	Algorit 1/
			Test no.	A6	A5	A4	A3	A0	A1	A2	$\overline{CS}$	V_{SS}	$\overline{WE}$	I/04	I/03	I/02	I/01	A9	A8	A7	V_{CC}	
9 T_C=+25°C	tWHDX	Fig 5	91	15/	15/	15/	15/	15/	15/	15/	15/	GND	15/	15/	15/	15/	15/	15/	15/	15/	4.5 V	GALF an GALR
	tWHDX		92	15/	15/	15/	15/	15/	15/	15/	15/	GND	15/	15/	15/	15/	15/	15/	15/	15/	5.5 V	GALF an GALR
	tAVQX		93	15/	15/	15/	15/	15/	15/	15/	15/	GND	15/	15/	15/	15/	15/	15/	15/	15/	4.5 V	GALF an GALR
	tAVQX		94	15/	15/	15/	15/	15/	15/	15/	15/	GND	15/	15/	15/	15/	15/	15/	15/	15/	5.5 V	GALF an GALR
10	Same tests, terminal conditions, and limits as subgroup 9, except T_C = 125°C.																					
11	Same tests, terminal conditions, and limits as subgroup 9, except T_C = -55°C.																					

1/ See appendix for description of algorithms.

2/ An input preconditioning logic sequence shall be applied that results in a logic “1”at the output to be measured. Logic input levels during measurement shall be: V_{IL} = 0.8 V; V_{IH} = 2.0 V. Forcing current I_{OL} shall be -4.0 mA.

3/ An input preconditioning logic sequence shall be applied that results in a logic “0” at the output to be measured. Logic input levels during measurement shall be:

	V_{IL}	V_{IH}	I_{OL}
Types 02, 04	0.8 V	2.0 V	8.0 mA

4/ I_{CC} = 110 mA for device type 02, 140 mA for device type 04.

5/ I_{SB} = 10 mA for device type 02; 30 mA for device type 04. The device manufacturer, may at his option, do either test or both tests.

6/ See 4.4.1c.

7/ V_{IL} = GND, V_{IH} = 6.0 V, pause time = 250 ms/loop max, $\overline{CS}$ = high, only performed once at 125°C, and V_{CC} = 0.7 V min.

8/ V_{IL} = 0.8 V and V_{IH} = 2.0 V.

9/ Algorithm has 60 ns where chip is deselected between the write.

10/ V_{IL} = GND, V_{IH} = 3.0 V, and all address setup times are at a minimum.

11/ V_{IL} = GND, V_{IH} = 3.0 V, and all write pulse timing are at minimums.

12/ V_{IL} = GND, V_{IH} = 3.0 V, and all address ending timing are at minimums.

13/ V_{IL} = GND, V_{IH} = 3.0 V, and tAVQV measured at minimum timing.

14/ V_{IL} = GND, V_{IH} = 3.0 V, tELQV1 and tELQV2 are measured at minimum timing.

15/ V_{IL} = 0.0 V, V_{IH} = 3.0 V, and all parameters are measured at minimum timing.

16/ tAVQV = 35 ns for device type 02; 55 ns for device type 04.

17/ tELQV1 and tELQV2 = 35 ns for device type 02; 65 ns for device type 04.

18/ tAVAV = 35 ns for device type 02; 55 ns for device type 04.

19/ tWLWH = 30 ns for device type 02; 40 ns for device type 04.

20/ tWHAX = 5 ns for device type 02; 5 ns for device type 04.

21/ tDVWH = 20 ns for device type 02; 20 ns for device type 04.

22/ tELWH = 30 ns for device type 02; 50 ns for device type 04.

23/ tAVWH = 30 ns for device type 02; 50 ns for device type 04.

24/ tAVWL = 30 ns for device type 02; 50 ns for device type 04.

25/ tAVQX is 0 ns for device type 02; 5 ns for device type 04.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but it is not mandatory)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. The acquisition document should specify the following:

a. Title, number, and date of the specification.
b. PIN and compliance identifier, if applicable (see 1.2).
c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
d. Requirement for certificate of compliance, if applicable.
e. Requirements for notification of change of product or process to the acquiring activity in addition to notification to the qualifying activity, if applicable.
f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.
g. Requirement for product assurance options.
h. Requirements for special lead lengths or lead forming, if applicable. These requirements will not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by, or direct shipment to the Government.
i. Requirements for "JAN" marking.
k. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

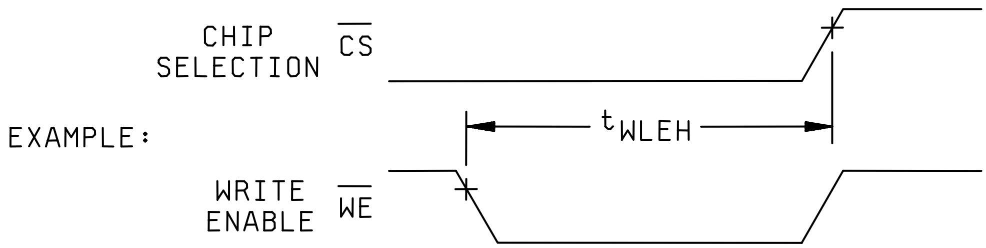
V_{CC}..Supply voltage
V_{SS}..Common or reference voltage node
C_{E}...Chip selection, input
D_{IN}..Data input
D_{OUT}..Data output
A_0 thru A_{11}...Address input
WE...Read or write input
I_{OHZ}...High impedance state high output current
I_{OLZ}...High impedance state low output current
I_{CC}..Supply current from V_{CC} supply
t_{AVAV}..Read cycle time
t_{AVWL}..Address set up time
t_{WLWH}...Write pulse width
t_{WHAX}...Write recovery time
t_{DVWH}...Data valid to end of write
t_{WHDX}...Data hold time
t_{AVQX}..Output hold time from address change
t_{AVQV}..Address access time
t_{ELQV}..Chip selection to output valid
t_{AVAV}..Write cycle time
t_{ELWH}..Chip selection to end of write
t_{AVWH}...Address valid to end of write
t_{ELQX}..Chip selection to output active
t_{EHQZ}..Chip deselection to output in high impedance
t_{ELPU}..Chip selection to power up time
t_{EHPD}..Chip deselection to power down time
t_{WLQZ}...Write enabled to output in high impedance
t_{WHQX}...Output active from end of write
I_{OZH}, I_{OZL}...Output leakage current
T_C..Case temperature
T_A..Ambient temperature

6.5.1 Timing parameter abbreviations. All timing abbreviations used lower case characters with upper case character subscripts. The initial character is always t and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transition. Thus the format is:

```
                                                      t    X     X     X     X
                                                           |     |     |     |
Signal name from which interval is defined ________________|     |     |     |
Transition direction for first signal ___________________________|     |     |
Signal name to which interval is defined ______________________________|     |
Transition direction for second signal ______________________________________|
```

a. Signal definitions:
A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable
O = Output current
P = Supply current

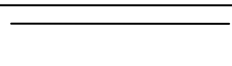
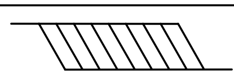
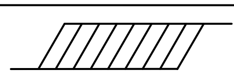
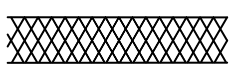
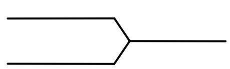
b. Transition definitions:
H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid
Z = Transition to off (high impedance)
U = up
N = Down



The example shows Write pulse setup time defined as t_{WLEH}-time from Write Enable to low to Chip Enable High.

c. Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

d. Waveforms:

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming will not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic industry type. Generic industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Device type	Commercial type	Cage number
01	7C147/Cypress Semiconductor	65786
02	7C148/ Cypress Semiconductor	--------
03	2147/ Cypress Semiconductor	--------
04	2148/ Cypress Semiconductor	--------

6.8 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extent of the changes.

FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope Functional algorithms are test patterns which define the exact sequence of the tests used to verify proper operation of a random access memory (RAM). Each algorithm serves a specified purpose for the testing of the device. This Appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 FUNCTIONAL PATTERNS.

A.2.1 Pattern 1.

CKBD

a. Write a checkerboard pattern into memory (0 in address 0) from address 0 to N.
b. When the $\overline{CS}$ off test is performed, attempt to write the complement pattern into cell memory with the device not selected.
c. Read checkerboard pattern in the memory.

A.2.2 Pattern 2.

$\overline{\text{CKBD}}$. Same as CKBD only with data complemented.

A.2.3 Pattern 3.

MARCH

a. Write test word into every location.
b. The addressing is then scanned from location “0” to location “N”.
c. At each address, the test word is read and a complemented test word is written back into the same location.
d. The addressing is then scanned in reverse from location “N” to location “O”.
e. At each address, the complemented test word is read and the test word is written back in.

A.2.4 Pattern 4.

GALPAT. This program will test all bits in the array. The addressing and interaction between bits for ac performance. The memory is initialized by writing a field of “1” and then a field of “0” into the cell memory.

a. Write a “1” in word location 0 (reference location).
b. Word 0 is read.
c. Word 1 is read.
d. Word 0 is read.
e. Word 2 is read.
f. Word 0 is read.
g. The reading procedure continues back and forth between word 0 and the next higher number word until word 4095 (01, 03) or 1023 (02, 04) is reached. Then increment to the next word which becomes the reference location and then step a through g again until all the words in the memory are used at least once as a reference.

A.2.5 Pattern 5.

Diagonal GALRESH (with row column ping pong read GG II). This pattern will test all bits in the array for writing interaction for switching performance.

a. Initialize the memory by writing a field of 0's.

b. Perform the following read write sequence moving the test bit along the diagonal of the memory; and reading only the row and column of the test bit in ping pong fashion:

RO = read "0" WI = Write "1" etc.

	STEP								
	1	2	3	4	5	6	7	8	9
BACKGROUND BIT		RO		RO		RO		RO	
TEST BIT	RO		WI		RI		WO		RO

c. Reinitialize the memory by writing a field of 1's.

d. Perform the following read write sequence moving the test bit along the diagonal of the memory; and reading only the row and column of the test bit in ping pong fashion:

	STEP								
	1	2	3	4	5	6	7	8	9
BACKGROUND BIT		RI		RI		RI		RI	
TEST BIT	RI		WO		RO		WI		RI

Custodians:
Army – CR
Navy - EC
Air Force – 11
DLA - CC

Preparing activity:

DLA - CC

(Project 5962-2005-052)

Review activities:
Army – MI, SM
Navy – AS, CG, MC, SH, TD
Air Force – 03, 19, 99

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NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil .