INCH-POUND

MIL-M-38510/755B
21 November 2003
SUPERSEDING
MIL-M-38510/755A
29 June 1992

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, ADVANCED CMOS, TRANSCEIVERS, MONOLITHIC SILICON, POSITIVE LOGIC

Reactivated after 21 Nov. 2003 and may be used for either new or existing design acquisitions.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, advanced CMOS, logic microcircuits. Two product assurance classes and a choice of case outlines, lead finishes, and radiation hardness assurance (RHA) are provided and are reflected in the complete Part or Identifying Number (PIN). For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535 (see 6.3).

1.2 Part or identifying number (PIN). The PIN should be in accordance with MIL-PRF-38535 and as specified herein.

1.2.1 Device types. The device types should be as follows:

Device type	Circuit
01	1/
02	1/
03	Octal bidirectional transceiver with three-state outputs
04	1/
05	Octal noninverting bus transceiver with three-state outputs
06	Octal bidirectional transceiver with three-state outputs
07	Octal bidirectional transceiver with three-state outputs
08	Octal transceiver/register with three-state outputs
09	Octal transceiver/register with three-state outputs

1.2.2 Device class. The device class should be the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines should be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	Flat pack
L	GDIP3-T24 or CDIP4-TF24	24	Dual-in-line
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
S	GDFP2-F20 or CDFP3-F20	20	Flat pack
Z	GDFP1-G20	20	Flat pack with gull wing
2	CQCC1-N20	20	Square leadless-chip-carrier
3	CQCC1-N28	28	Square leadless-chip-carrier

1/ Devices 01, 02, and 04 were intended to be added in the future, see 6.7

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAC, 3990 East Broad St., Columbus, OH 43216-5000, or email to cmos@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at www.dodssp.daps.mil.

AMSC N/A FSC 5962

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{CC})	-0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} +0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
Clamp diode current (I_{IK}, I_{OK})	±20 mA
DC output current (I_{OUT})	±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND})	±100 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 3/ 4/

Supply voltage range (V_{CC})	+3.0 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Maximum low level Input voltage(V_{IL})	0.90 V dc at V_{CC} = 3.0 V dc
	1.35 V dc at V_{CC} = 4.5 V dc
	1.65 V dc at V_{CC} = 5.5 V dc
Minimum high level Input voltage (V_{IH})	2.10 V dc at V_{CC} = 3.0 V dc
	3.15 V dc at V_{CC} = 4.5 V dc
	3.85 V dc at V_{CC} = 5.5 V dc
Input rise and fall rate (t_r, t_f) maximum:	
V_{CC} = 3.6 V, V_{CC} = 5.5 V	8 ns/V

Minimum set-up time, high or low, bus to clock (t_s):		Device types 08	09
V_{CC} = 3.0 V dc;	T_C = +25°C, -55°C	5.0 ns	3.0 ns
	T_C = +125°C	6.0 ns	4.0 ns
V_{CC} = 4.5 V dc;	T_C = +25°C, -55°C	4.0 ns	2.0 ns
	T_C = +125°C	4.5 ns	2.5 ns

Minimum hold time, high or low, bus to clock (t_h):		Device types 08	09
V_{CC} = 3.0 V dc;	T_C = +25°C, +125°C	1.0 ns	0.0 ns
	T_C = -55°C	1.5 ns	0.0 ns
V_{CC} = 4.5 V dc;	T_C = +25°C, +125°C	1.5 ns	1.0 ns
	T_C = -55°C	2.0 ns	1.0 ns

Minimum clock pulse width, high or low (t_w):		Device types 08	09
V_{CC} = 3.0 V dc;	T_C = +25°C, -55°C	5.0 ns	3.5 ns
	T_C = +125°C	5.0 ns	4.5 ns
V_{CC} = 4.5 V dc;	T_C = +25°C, -55°C	5.0 ns	2.0 ns
	T_C = +125°C	5.0 ns	3.5 ns

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s):	
Device type 03	300 krads (Si)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with MIL-PRF-38535.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ Operation from 2.0 V dc to 3.0 V dc is provided for compatibility with data retention and battery back-up systems. Data retention implies no input transitions and no stored data loss with the following conditions: $V_{IH} \geq 70$ percent of V_{CC}, $V_{IL} \leq 30$ percent of V_{CC}, $V_{OH} \geq 70$ percent of V_{CC} at –20 µA, $V_{OL} \leq 30$ percent of V_{CC} at 20 µA.

4/ Unless otherwise specified, the values listed above shall apply over the full V_{CC} and T_C recommended operating range.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and Standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

EIA/JEDEC Standard No. 78 - IC Latch-Up Test

JEDEC Standard No. 20 - Standard for Description of 54/74ACXXXXX and 54/74ACTXXXXX Advanced High-Speed CMOS Devices

(Copies of these documents are available on line at http://www.jedec.org or from Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.4).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.2 Truth tables. The truth tables shall be as specified on figure 2.

3.3.3 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity or preparing activity upon request.

3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3 herein.

3. 4 Electrical performance characteristics and post irradiation end-point electrical parameter limits. Unless otherwise specified, the electrical performance characteristics and postirradiation end-point electrical parameter limits are as specified in table I and apply over the case operating temperature range specified. Test conditions for these specified characteristics and limits are as specified in table I.

3.5 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I. Radiation hardness assurance level M, D, P, L , R, and F (see MIL-PRF-38535) in table I are postirradiation end-point electrical parameters.

3.7 Radiation hardness assurance identifier. The radiation hardness assurance identifier shall be in accordance with MIL-PRF-38535 and herein (see 3.6).

3.8 Marking. Marking shall be in accordance with MIL-PRF-38535. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.

3.9 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 37 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method	Symbol	Test Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
High level output voltage 3006	V_{OH1} 3/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10\ V$ $V_{IL} = 0.90\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$		All	3.0 V	1, 2, 3	2.9		V
	V_{OH2} 3/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15\ V$ $V_{IL} = 1.35\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$		All	4.5 V	1, 2, 3	4.4		
	V_{OH3} 4/ 5/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$ $V_{IL} = 1.65\ V$		All	5.5 V	1, 2, 3	5.4		
		For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$	M	03		1	5.4		
			D				5.4		
			P, L, R, F				5.4		
	V_{OH4} 3/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10\ V$ $V_{IL} = 0.90\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -4.0\ mA$		All	3.0 V	1, 2, 3	2.4		
	V_{OH5} 4/ 5/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15\ V$ $V_{IL} = 1.35\ V$		All	4.5 V	1, 2, 3	3.7		
		For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -24\ mA$	M	03		1	3.7		
			D				3.7		
			P, L, R, F				3.7		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
High level output voltage 3006	V_{OH6} 3/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$ $V_{IL} = 1.65\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -24\ mA$		All	5.5 V	1, 2, 3	4.7		V
	V_{OH7} 4/ 5/ 6/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$ $V_{IL} = 1.65\ V$		All	5.5 V	1, 2, 3	3.85		
		For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ mA$	M	03		1	3.85		
			D				3.85		
			P, L, R, F				3.85		
Low level output voltage 3007	V_{OL1} 3/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10\ V$ $V_{IL} = 0.90\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ \mu A$		All	3.0 V	1, 2, 3		0.1	V
	V_{OL2} 3/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15\ V$ $V_{IL} = 1.35\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ \mu A$		All	4.5 V	1, 2, 3		0.1	
	V_{OL3} 4/ 5/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$ $V_{IL} = 1.65\ V$		All	5.5 V	1, 2, 3		0.1	
		For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ \mu A$	M	03		1		0.1	
			D					0.1	
			P, L, R, F					0.1	
	V_{OL4} 3/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10\ V$ $V_{IL} = 0.90\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = 12\ mA$		All	3.0 V	1, 3		0.4	
						2		0.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
Low level output voltage 3007	V_{OL5} 4/ 5/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15\ V$ $V_{IL} = 1.35\ V$		All	4.5 V	1, 3		0.4	V
						2		0.5	
		For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = 24\ mA$	M	03		1		0.4	
			D					0.4	
			P, L, R, F					0.4	
	V_{OL6} 3/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$ $V_{IL} = 1.65\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = 24\ mA$		All	5.5 V	1, 3		0.4	
						2		0.5	
	V_{OL7} 4/ 5/ 6/	For all inputs affecting output under test, $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$ $V_{IL} = 1.65\ V$		All	5.5 V	1, 2, 3		1.65	
		For all other inputs, $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ mA$	M	03		1		1.65	
			D					1.65	
			P, L, R, F					1.65	
Positive input clamp voltage 3022	V_{IC+} 4/ 5/	For input under test, $I_{IN} = 1\ mA$		All	GND	1	0.4	1.5	V
			M	03		1	0.4	1.5	
			D				0.4	1.5	
			P, L, R, F				0.4	1.5	
Negative input clamp voltage 3022	V_{IC-} 4/ 5/	For input under test, $I_{IN} = -1\ mA$		All	Open	1	-0.4	-1.5	V
			M	03		1	-0.4	-1.5	
			D				-0.4	-1.5	
			P, L, R, F				-0.4	-1.5	
Input current low 3009	I_{IL} 4/ 5/	For input under test, $V_{IN} = GND$ For all other inputs, $V_{IN} = V_{CC}$ or GND		All	5.5 V	1		-0.1	µA
						2		-1.0	
			M	03		1		-0.1	
			D					-0.1	
			P, L, R, F					-0.1	
Input current high 3010	I_{IH} 4/ 5/	For input under test, $V_{IN} = V_{CC}$ For all other inputs, $V_{IN} = V_{CC}$ or GND		All	5.5 V	1		0.1	µA
						2		1.0	
			M	03		1		0.1	
			D					0.1	
			P, L, R, F					0.1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test Conditions 1/ -55°C ≤ T_C ≤ +125°C +3.0 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified	Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
						Min	Max	
Input/output capacitance 3012	$C_{I/O}$ 7/	See 4.4.1c T_C = +25°C	All	5.5 V	4		15	pF
Input capacitance (control inputs) 3012	C_{IN}	See 4.4.1c T_C = +25°C	All	GND	4		10	pF
Power dissipation capacitance	C_{PD} 8/	See 4.4.1c T_C = +25°C	03	5.0 V	4		60	pF
			05, 06, 07				45	
			08				80	
			09				65	
Quiescent supply current, output three-state 3005	I_{CCZ} 4/ 5/ 7/	For all inputs, V_{IN} = V_{CC} or GND	All	5.5 V	1		2.0	µA
					2		40.0	
		M	03		1		15.0	
		D			1		75.0	
		P, L, R, F			1		0.7	mA
Quiescent supply current, output high 3005	I_{CCH} 4/ 5/	For all inputs, V_{IN} = V_{CC} or GND	All	5.5 V	1		2.0	µA
					2		40.0	
		M	03		1		15.0	
		D			1		75.0	
		P, L, R, F			1		0.7	mA
Quiescent supply current, output low 3005	I_{CCL} 4/ 5/	For all inputs, V_{IN} = V_{CC} or GND	All	5.5 V	1		2.0	µA
					2		40.0	
		M	03		1		15.0	
		D			1		75.0	
		P, L, R, F			1		0.7	mA
Three-state output leakage current low 3020	I_{OZL} 4/ 5/ 9/	V_{OUT} = GND	All	5.5 V	1		-0.6	µA
					2		-11.0	
		M	03		1		-1.0	
		D					-3.0	
		P, L, R, F					-20.0	
Three-state output leakage current high 3021	I_{OZH} 4/ 5/ 9/	V_{OUT} = V_{CC}	All	5.5 V	1		0.6	µA
					2		11.0	
		M	03		1		1.0	
		D					3.0	
		P, L, R, F					20.0	
Low level ground bounce noise	V_{GBL} 10/ 11/	V_{LD} = 2.5 V I_{OL} = +24 mA V_{IN} = 4.5 V or 0.0 V see figure 3	01, 02	4.5 V	4	0.0	1000	mV
			03-09			0.0	2000	
High level ground bounce noise	V_{GBH} 10/ 11/	V_{LD} = 2.5 V I_{OH} = -24 mA V_{IN} = 4.5 V or 0.0 V see figure 3	01, 02	4.5 V	4	0.0	1000	mV
			03-09			0.0	2000	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
Latch-up input/ output over-voltage	I_{CC} (O/V1) 12/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $V_{over} = 10.5\ V$		All	5.5 V	2		200	mA
Latch-up input/ output positive over-current	I_{CC} (O/I1+) 12/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $I_{trigger} = +120\ mA$		All	5.5 V	2		200	mA
Latch-up input/ output negative over-current	I_{CC} (O/I1-) 12/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $I_{trigger} = -120\ mA$		All	5.5 V	2		200	mA
Latch-up supply over-voltage	I_{CC} (O/V2) 12/	$t_w \ge 100\ \mu s$ $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$ $V_{CCQ} = 5.5\ V$ $V_{over} = 9.0\ V$		All	5.5 V	2		100	mA
Truth table test output voltage 3014	4/ 5/ 13/	$V_{IL} = 0.45\ V$ $V_{IH} = 2.50\ V$ Verify output V_{OUT}	M	03	3.0 V	7	L	H	
			D				L	H	
			P, L, R, F				L	H	
		$V_{IL} = 0.60\ V$, $V_{IH} = 3.70\ V$ Verify output V_{OUT}		All	4.5 V	7, 8	L	H	
Maximum clock frequency 3003	f_{MAX}	$C_L = 50\ pF$ $R_L = 500\ \Omega$ See 4.4.1f		08, 09	3.0 V	9, 10, 11	90		MHz
				08, 09	4.5 V	9, 10, 11	100		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
Propagation delay time, data to output 3003	t_{PHL1}, t_{PLH1} 4/ 5/ 14/ 15/	C_L = 50 pF minimum R_L = 500Ω see figure 4		03	3.0 V	9, 11	1.0	8.5	ns
						10	1.0	11.5	
				05		9, 11	1.0	12.0	
						10	1.0	13.0	
				06		9, 11	1.0	5.5	
						10	1.0	6.0	
				07		9, 11	1.0	5.0	
						10	1.0	5.5	
				08, 09		9, 11	1.0	12.0	
						10	1.0	15.0	
			M	03		9	1.0	8.5	
			D				1.0	8.5	
			P, L, R, F				1.0	8.5	
		C_L = 50 pF minimum R_L = 500Ω see figure 4		03	4.5 V	9, 11	1.0	6.5	ns
						10	1.0	8.5	
				05		9, 11	1.0	8.5	
						10	1.0	9.5	
				06		9, 11	1.0	4.0	
						10	1.0	4.5	
				07		9, 11	1.0	4.0	
						10	1.0	4.5	
				08, 09		9, 11	1.0	8.0	
						10	1.0	10.0	
			M	03		9	1.0	6.5	
			D				1.0	6.5	
			P, L, R, F				1.0	6.5	
Propagation delay time, clock to bus 3003	t_{PHL2}, t_{PLH2} 14/ 15/	C_L = 50 pF minimum R_L = 500Ω see figure 4		08, 09	3.0 V	9, 11	1.0	16.0	ns
						10	1.0	20.0	
				08, 09	4.5 V	9, 11	1.0	11.0	
						10	1.0	14.0	
Propagation delay time, SBA/SAB to bus 3003	t_{PHL3}, t_{PLH3} 14/ 15/	C_L = 50 pF minimum R_L = 500Ω see figure 4		08, 09	3.0 V	9, 11	1.0	13.5	ns
						10	1.0	17.0	
				08, 09	4.5 V	9, 11	1.0	10.0	
						10	1.0	12.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
Propagation delay time, output enable, $\overline{OE}$, $\overline{G}$, $\overline{OEBA}$ or OEAB to output 3003	t_{PZH1}, t_{PZL1} 4/ 5/ 14/ 15/	C_L = 50 pF minimum R_L = 500Ω see figure 4		03	3.0 V	9, 11	1.0	12.0	ns
						10	1.0	14.5	
				05		9, 11	1.0	18.0	
						10	1.0	20.0	
				06		9, 11	1.0	8.0	
						10	1.0	8.5	
				07		9, 11	1.0	8.0	
						10	1.0	8.5	
				08, 09		9, 11	1.0	13.0	
						10	1.0	15.5	
			M	03		9	1.0	12.0	
			D				1.0	12.0	
			P, L, R, F				1.0	12.0	
		C_L = 50 pF minimum R_L = 500Ω see figure 4		03	4.5 V	9, 11	1.0	9.0	ns
						10	1.0	10.5	
				05		9, 11	1.0	12.0	
						10	1.0	13.0	
				06		9, 11	1.0	6.0	
						10	1.0	6.5	
				07		9, 11	1.0	6.0	
						10	1.0	6.5	
				08, 09		9, 11	1.0	9.5	
						10	1.0	11.0	
			M	03		9	1.0	9.0	
			D				1.0	9.0	
			P, L, R, F				1.0	9.0	
Propagation delay time, output enable, DIR to bus 3003	t_{PZH2}, t_{PZL2} 14/ 15/	C_L = 50 pF minimum R_L = 500Ω see figure 4		08, 09	3.0 V	9, 11	1.0	13.5	ns
						10	1.0	16.0	
				08, 09	4.5 V	9, 11	1.0	10.5	
						10	1.0	12.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method	Symbol	Test Conditions 1/ $-55°C \le T_C \le +125°C$ $+3.0\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified		Device type 2/	V_{CC}	Group A subgroups	Limits 1/		Unit
							Min	Max	
Propagation delay time, output disable, $\overline{OE}$, $\overline{G}$, $\overline{OEBA}$ or OEAB to output 3003	t_{PHZ1}, t_{PLZ1} 4/ 5/ 14/ 15/	C_L = 50 pF minimum R_L = 500Ω see figure 4		03	3.0 V	9, 11	1.0	12.0	ns
						10	1.0	14.0	
				05		9, 11	1.0	15.0	
						10	1.0	16.5	
				06		9, 11	1.0	7.5	
						10	1.0	8.0	
				07		9, 11	1.0	7.5	
						10	1.0	8.0	
				08, 09		9, 11	1.0	12.0	
						10	1.0	14.0	
			M	03		9	1.0	12.0	
			D				1.0	12.0	
			P, L, R, F				1.0	12.0	
		C_L = 50 pF minimum R_L = 500Ω see figure 4		03	4.5 V	9, 11	1.0	9.0	ns
						10	1.0	10.5	
				05		9, 11	1.0	12.0	
						10	1.0	13.0	
				06		9, 11	1.0	6.0	
						10	1.0	6.5	
				07		9, 11	1.0	6.0	
						10	1.0	6.5	
				08, 09		9, 11	1.0	10.0	
						10	1.0	11.5	
			M	03		9	1.0	9.0	
			D				1.0	9.0	
			P, L, R, F				1.0	9.0	
Propagation delay time, output disable, DIR to bus 3003	t_{PHZ2}, t_{PLZ2} 14/ 15/	C_L = 50 pF minimum R_L = 500Ω see figure 4		08, 09	3.0 V	9, 11	1.0	14.0	ns
						10	1.0	16.5	
				08, 09	4.5 V	9, 11	1.0	10.0	
						10	1.0	12.0	

1/ Each input/output, as applicable, shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. V_{IC} (pos) tests, the GND terminal can be open. T_C = +25°C.

b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. T_C = +25°C.

c. All I_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively, and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

2/ The word “All” in the device type column means non-RHA and preirradiation limits for all devices. Where. M, D, P, L, R, and F in the conditions column specify the postirradiation limits for those device types specified in the device type column.

TABLE I. Electrical performance characteristics - Continued.

3/ This parameter is provided as design information only.

4/ RHA samples do not have to be tested at either -55°C and +125°C prior to irradiation.

5/ When performing postirradiation electrical measurements for any RHA level, T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ±5°C.

6/ Transmission driving tests are performed at V_{CC} = 5.5 V dc with a 2 ms duration maximum.

7/ Set output enable control pins to V_{CC} or GND, as applicable, to disable the outputs.

8/ Power dissipation capacitance (C_{PD}) determines the no load dynamic power consumption, $P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$ and the dynamic current consumption, $I_S = (C_{PD} + C_L)V_{CC}f + I_{CC}$. For both C_{PD} and I_S, f is the frequency of the input signal and d is the duty cycle of the input signal.

9/ Three-state output conditions are required. For I_{OZL}, set outputs to high state. For I_{OZH}, set outputs to low state. Set output enable control pins to $V_{IL} = V_{IL(MAX)}$ and $V_{IH} = V_{IH(MIN)}$, as required. For I/O pins, the I_{IH} and I_{IL} measurements shall not be directly performed. These measurements are included in the I_{OZH} and I_{OZL} limits, respectively.

10/ This test is for qualification only. Ground bounce tests are performed on a nonswitching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture with all outputs fully dc loaded (I_{OL} maximum and I_{OH} maximum = i.e., ±24 mA) and 50 pF of load capacitance (see figure 3). The loads must be located as close as possible to the device output. Inputs are then conditioned with 1 MHz pulse ($t_r = t_f$ = 3.5 ±1.5 ns) switching simultaneously and in phase such that one output is forced low and all others (possible) are switched. The low level ground bounce noise is measured at the quiet output using a F.E.T. oscilloscope probe with at least 1 MΩ impedance. Measurement is taken from the peak of the largest positive pulse with respect to the nominal low level output voltage (figure 3). The device inputs are then conditioned such that the output under test is at a high nominal V_{OH} level. The high level ground bounce measurement is then measured from nominal V_{OH} level to the largest negative peak. This procedure is repeated such that all outputs are tested at a high and low level with a maximum number of outputs switching.

11/ When using in asynchronous TTL compatible systems, ground bounce (V_{GBL} and V_{GBH}) = 2000 mV can be a possible problem.

12/ See EIA/JEDEC STD. No. 78 for electrically induced latch-up test methods and procedures. The values listed for $I_{trigger}$ and V_{over} are to be accurate within ±5 percent.

13/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth tables and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. H ≥ 2.5 V, L < 2.5 V; high inputs = 3.7 V and low inputs = 0.6 V for V_{CC} = 4.5 V and H ≥ 1.5 V, L < 1.5 V; high inputs = 2.5 V and low inputs = 0.45 V for V_{CC} = 3.0 V. Tests at V_{CC} = 3.0 V are for RHA specified devices only (T_A = +25°C ±5°C). Functional tests at V_{CC} = 3.0 V are worst case for RHA specified devices.

14/ Device are tested at V_{CC} = 3.0 V and V_{CC} = 4.5 V at T_C = +125°C for sample testing and at V_{CC} = 3.0 V and V_{CC} = 4.5 V at T_C = +25°C for screening. Other voltages of V_{CC} and temperatures are guaranteed, if not tested. See 4.4.1d.

15/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum ac limits for V_{CC} = 5.5 V are 1.0 ns and guaranteed by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

Device types	03, 06, 07	05	08, 09	
Case outlines	R, S, 2, and Z	R, S, 2	K, L	3
Terminal number	Terminal symbol			
1	$T/\overline{R}$	OEAB	CAB	NC
2	A0	A0	SAB	CAB
3	A1	A1	DIR	SAB
4	A2	A2	A0	DIR
5	A3	A3	A1	A0
6	A4	A4	A2	A1
7	A5	A5	A3	A2
8	A6	A6	A4	NC
9	A7	A7	A5	A3
10	GND	GND	A6	A4
11	B7	B7	A7	A5
12	B6	B6	GND	A6
13	B5	B5	B7	A7
14	B4	B4	B6	GND
15	B3	B3	B5	NC
16	B2	B2	B4	B7
17	B1	B1	B3	B6
18	B0	B0	B2	B5
19	$\overline{OE}$	$\overline{OEBA}$	B1	B4
20	V_{CC}	V_{CC}	B0	B3
21	- - -	- - -	$\overline{G}$	B2
22	- - -	- - -	SBA	NC
23	- - -	- - -	CBA	B1
24	- - -	- - -	V_{CC}	B0
25	- - -	- - -	- - -	$\overline{G}$
26	- - -	- - -	- - -	SBA
27	- - -	- - -	- - -	CBA
28	- - -	- - -	- - -	V_{CC}

NC = No connection.

FIGURE 1. Terminal connections.

Device types 03

Input		Operation
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B data to bus A
L	H	Bus A data to bus B
H	X	High impedance state

Device type 05

Output enable Input		Operation
$\overline{OEBA}$	OEAB	
L	L	B data to A bus
H	H	A data to B bus
H	L	Isolation

Device type 06

Input			Valid direction I/P – O/P	Output
$\overline{OE}$	T/$\overline{R}$	Applied inputs		
H	X	X	X	X
L	H	H	A to B	L
L	H	L	A to B	H
L	L	H	B to A	L
L	L	L	B to A	H

Device type 07

Input			Valid direction I/P – O/P	Output
$\overline{OE}$	T/$\overline{R}$	Applied inputs		
H	X	X	X	X
L	H	H	A to B	L
L	H	L	A to B	H
L	L	H	B to A	H
L	L	L	B to A	L

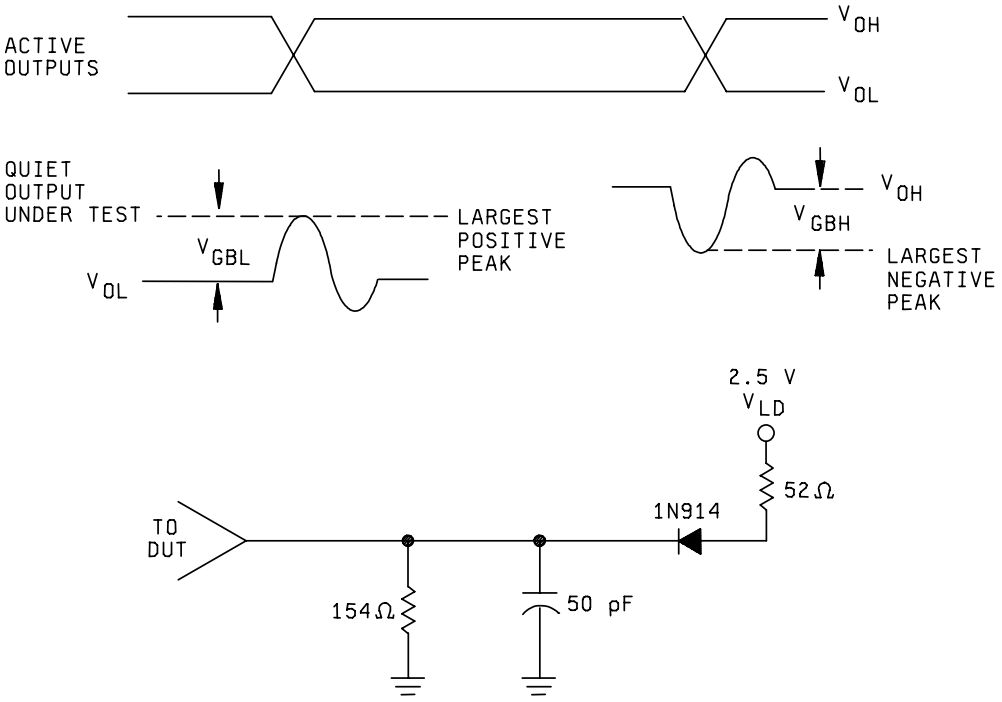
Device types 08 and 09

Inputs						Data I/O 1/		Operation
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A0-A7	B0-B7	
H	X	H or L	H or L	X	X			Isolation
H	X	↑	X	X	X	Input	Input	Clock A data into A register
H	X	X	↑	X	X			Clock B data into B register
L	H	X	X	L	X			Real time A data input to B bus 2/
L	H	↑	X	L	X	Input	Output	Clock A data into A register 2/
L	H	H or L	X	H	X			A register data to B bus 2/
L	H	↑	X	H	X			Clock A data into A register and output to B bus 2/
L	L	X	X	X	L			Real time B data to A bus 2/
L	L	X	↑	X	L	Output	Input	Clock B data into B register 2/
L	L	X	H or L	X	H			B register data into B bus 2/
L	L	X	↑	X	H			Clock B data into B register and output to A bus 2/

1/ The data output functions may enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.
2/ For device type 09, these data inputs are inverted.

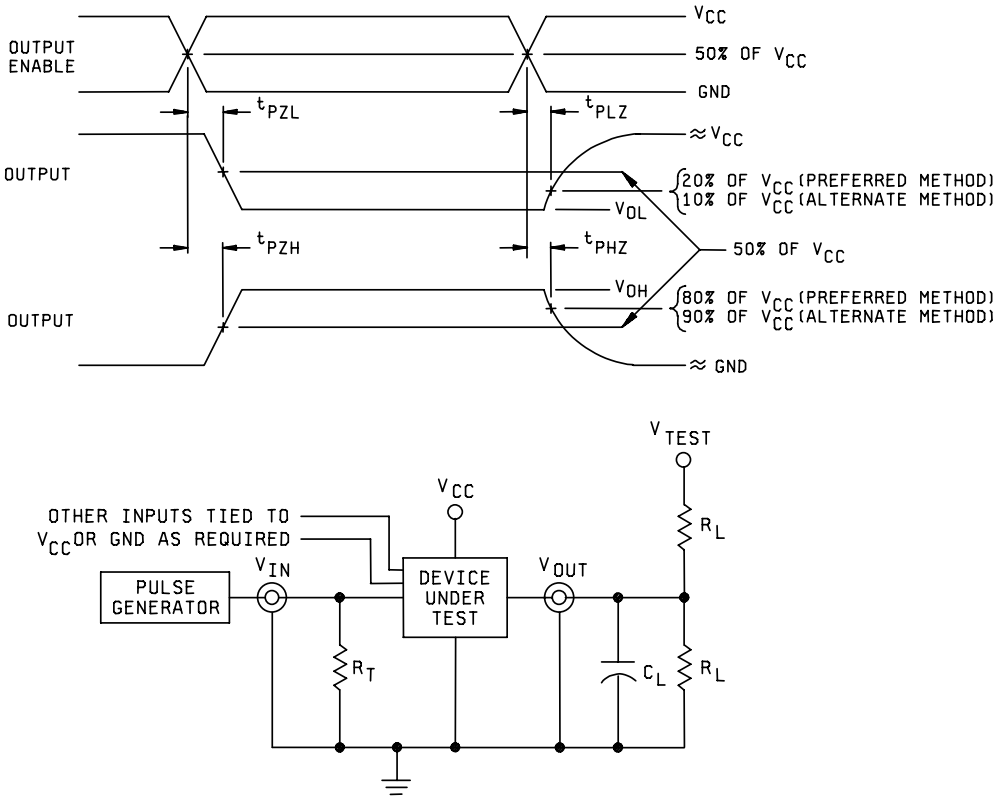
H = High level
L = Low level
Z = High-impedance
X = Don't care
↑ = Low-to-high transition of the clock.

FIGURE 2. Truth tables.



NOTE: Resistor and capacitor tolerances = ±10%.

FIGURE 3. Voltage levels for ground bounce.

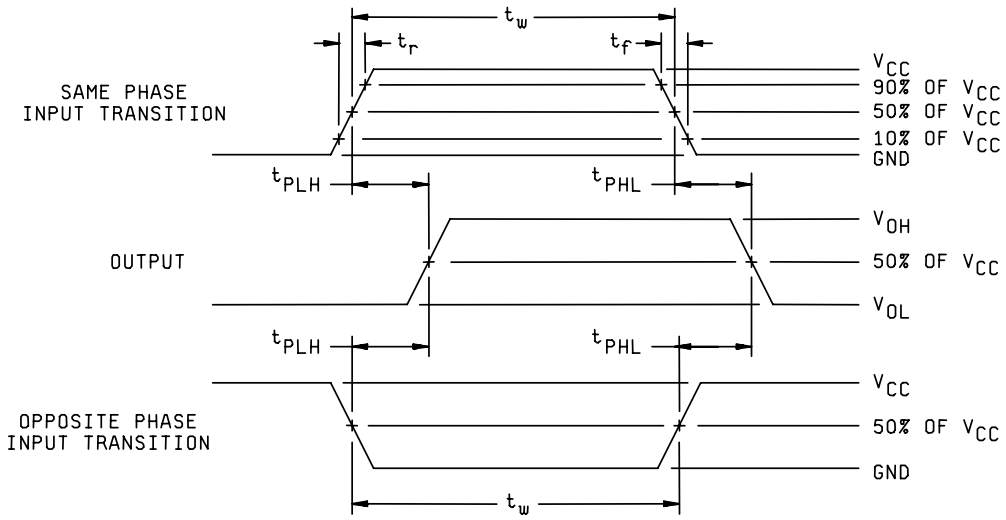


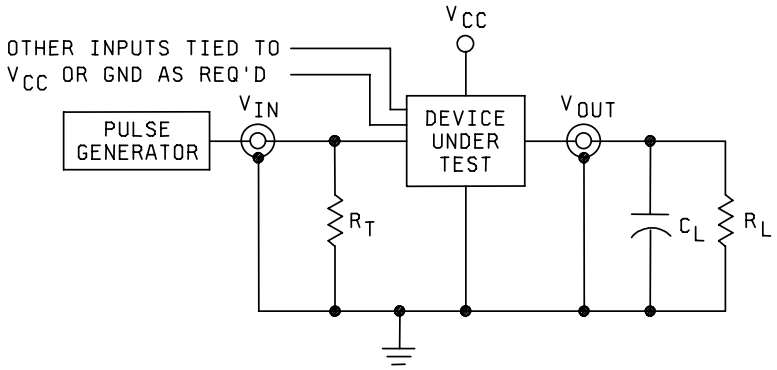
NOTES:

1. Preferred methods:
   When measuring t_{PHZ} or t_{PZH}: V_{TEST} = GND.
   When measuring t_{PLZ} or t_{PZL}: V_{TEST} = 2(V_{CC}).

2. Alternate method:
   When measuring t_{PHZ} or t_{PZH}: V_{TEST} = OPEN.
   When measuring t_{PLZ} or t_{PZL}: V_{TEST} = 2(V_{CC}).
3. C_L = 50pF or equivalent (includes test jig and probe capacitance).
4. R_L = 500Ω or equivalent.
5. R_T = 50Ω or equivalent.
6. V_{IN} = 0 V to V_{CC}.

FIGURE 4. Switching waveforms and test circuit.





NOTES:

1. t_r, $t_f \leq 3$ ns, PRR $\leq$ 10 MHz, duty cycle = 50 percent. For synchronous and asynchronous inputs, use as a maximum, the minimum pulse width or recovery time listed in section 1.4 herein, as applicable, in place of the duty cycle.
2. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
3. R_L = 500Ω or equivalent.
4. R_T = 50Ω or equivalent.

FIGURE 4. Switching waveforms and test circuit – Continued.

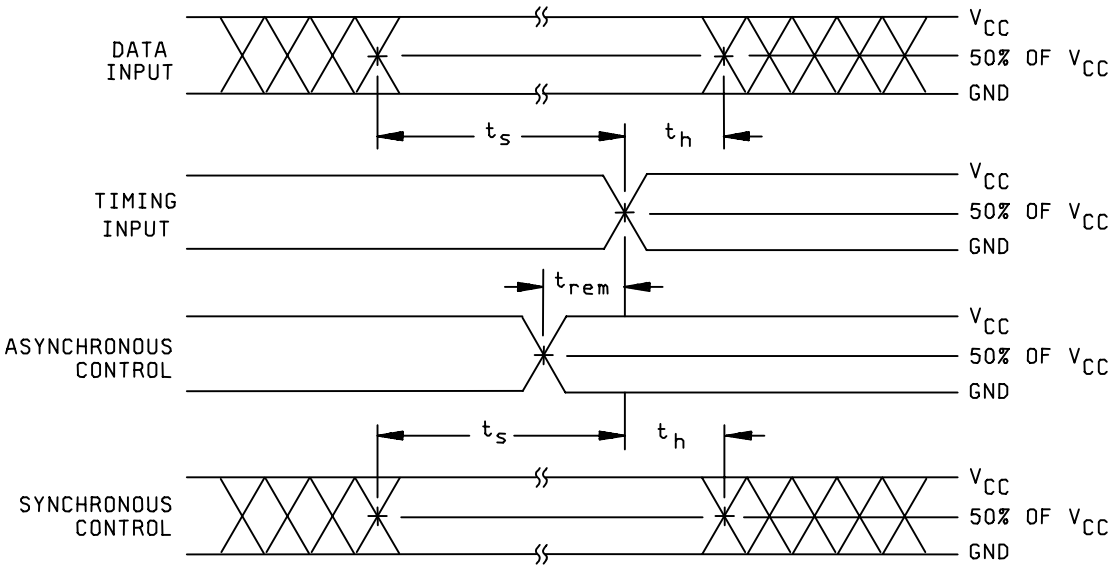


FIGURE 4. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.1.1 Burn-in and life test circuits. Burn-in and life test circuits shall be constructed so that the devices are stressed at the maximum operating conditions stated in 4.2c or 4.2d, as applicable, or equivalent as approved by the qualifying activity.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (post-burn-in) electrical parameters of method 5004 and substitute lines 1 through 7 of table II herein.

c. Static burn-in, test condition A, method 1015 of MIL-STD-883. Test duration for each static test shall be 24 hours minimum for class S devices and in accordance with table I of method 1015 for class B devices.

(1) For static burn-in I, the output enable control pin(s) shall be connected to the resistors in parallel to V_{CC} or GND, as applicable, to enable the outputs. The directional control pin(s) shall be connected to either V_{CC} or GND. All other inputs shall be connected to GND. Outputs may be open or connected to $V_{CC}/2$. Resistors R1 are optional on both inputs and open outputs, and required on outputs connected to $V_{CC}/2$ ±0.5 V. R1 = 220Ω to 47 kΩ.

(2) For static burn-in II, the output enable control pin(s) shall be connected to the resistors in parallel to V_{CC} or GND, as applicable, to enable the outputs. The directional control pin(s) shall be connected to either V_{CC} or GND. All other inputs shall be connected through the R1 resistors to V_{CC}. Outputs may be open or connected to $V_{CC}/2$ ±0.5 V. Resistors R1 are optional to open outputs, and required on outputs connected to $V_{CC}/2$ ±0.5 V. R1 = 220Ω to 47 kΩ.

(3) V_{CC} = 5.5 V +0.5 V, -0.00 V.

d. Dynamic burn-in, test condition D, method 1015 of MIL-STD-883.

(1) Input resistors = 220Ω to 2 kΩ ±20 percent.

(2) Output resistors = 220Ω ±20 percent.

(3) V_{CC} = 5.5 V +0.5 V, -0.00 V.

(4) The output enable control pin(s) shall be connected through the resistors in parallel to V_{CC} or GND, as applicable, to enable the outputs. The directional control pin(s) shall be connected to either V_{CC} or GND. All other inputs shall be connected through the resistors in parallel to a clock pulse (CP). Outputs shall be connected to $V_{CC}/2$ through the resistors.

(5) CP = 25 kHz to 1 MHz square wave; duty cycle = 50 percent ±15 percent; V_{IH} = 4.5 V to V_{CC}, V_{IL} = 0 V ±0.5 V; t_r, $t_f \leq$ 100 ns.

e. Interim and final electrical test parameters shall be as specified in table II.

f. For class S devices, post dynamic burn-in, or class B devices, post static burn-in, electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

4.2.1 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. Static burn-in I and II failures shall be cumulative for determining the PDA.

c. The PDA for class B devices shall be in accordance with MIL-PRF-38535 for static burn-in. Dynamic burn-in is not required.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified number of failed devices times 100 divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

a. Tests shall be performed in accordance with table II herein.

b. O/V and O/I (latch-up) tests and $V_{GBL/H}$ (ground bounce) tests shall be measured only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up test shall be considered destructive. Test all applicable pins on 5 devices with no failures.

c. C_{IN}, $C_{I/O}$, and C_{PD} shall be measured only for initial qualification and after process or design changes that may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For C_{IN}, C_{OUT}, and C_{PD}, test all applicable pins on five devices with zero failures.

d. Subgroups 9 and 11 shall be measured only for initial qualification and after process or design changes which may affect dynamic performance.

e. Subgroups 7 and 8 tests shall be sufficient to verify the truth table.

f. f_{MAX} shall be measured only for initial qualification and after process or design changes that may affect the device frequency. Test all applicable pins on 22 devices with zero failures.

TABLE II. Burn-in and electrical test requirements.

Line no.	MIL-PRF-38535 test requirements	Class S device 1/			Class B device 1/		
		Reference paragraph	Table I subgroups 2/	Table III delta limits 3/	Reference paragraph	Table I subgroups 2/	Table III delta limits 3/
1	Interim electrical parameters		1			1	
2	Static burn-in I (method 1015)	4.2c 4.5.2	Req'd 4/			Not req'd	
3	Same as line 1		1	Δ			
4	Static burn-in II (method 1015)	4.2c 4.5.2	Req'd 4/		4.2c 4.5.2	Req'd 5/	
5	Same as line 1	4.2e	1*	Δ	4.2e	1*	Δ
6	Dynamic burn-in (method 1015)	4.2d 4.5.2	Req'd 4/			Not req'd	
7	Same as line 1	4.2e	1	Δ			
8	Final electrical parameters		1*, 2, 7*, 9			1*, 2, 7*, 9 5/	
9	Group A test requirements	4.4.1	1, 2, 3, 4, 7, 8, 9, 10, 11		4.4.1	1, 2, 3, 4, 7, 8, 9, 10, 11	
10	Group B test when using the method 5005 QCI option	4.4.2	1, 2, 3, 7, 8, 9, 10, 11	Δ			
11	Group C end-point electrical parameters	4.4.3	1, 2, 3, 7, 8, 9, 10, 11	Δ	4.4.3	1, 2	Δ
12	Group D end-point electrical parameters	4.4.4	1, 2, 3		4.4.4	1, 2	
13	Group E end-point electrical parameters	4.4.5	1, 7, 9		4.4.5	1, 7, 9	

1/ Blank spaces indicate tests are not applicable.

2/ * indicates PDA applies to subgroups 1 and/or 7, as applicable (see 4.2.1).

3/ Δ indicates delta limits and shall be required only on table I, subgroup 1, where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (line 1).

4/ On all class S lots, the device manufacturer shall maintain read-and-record data (as a minimum on disk) for burn-in electrical parameters (group A, subgroup 1). For preburn-in and interim electrical parameters, the read-and-record requirements are for delta measurements only.

5/ The device manufacturer may, at his option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias). When the manufacturer elects to perform the subgroup 1 electrical parameter measurements without delta measurements, there is no requirement to perform the pre-burn-in electrical tests (first interim electrical parameters test in table II).

TABLE III. Delta limits at 25°C.

Parameter 1/	Device types	Limits
I_{CCZ}, I_{CCH}, I_{CCL}	All	±100 nA

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine deltas (Δ).

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

a. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 1 of group C inspection and shall consist of tests specified in table III herein.

b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.7 herein). RHA levels for device classes B and S shall be as specified in MIL-PRF-38535.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes B and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for construction.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

d. RHA tests for device classes B and S for levels M, D, P, L, R, and F shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the devices.

e. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

f. For device classes B and S, the devices shall be subjected to radiation hardness assurance tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.5.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

a. Input tested high, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω ±20%, V_{IN} = 5.0 V dc +5%, R_{IN} = 1 kΩ ±20%, and all outputs are open.

b. Inputs tested low, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω ±20%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ ±20%, and all outputs are open.

4.4.5.1.1 Accelerated aging test. Accelerated aging shall be performed on class B and S devices requiring an RHA level greater that 5k rads (Si). The post-anneal end point electrical parameter limits shall be as specified in table I herein and shall be the preirradiation end point electrical parameter limit at +25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Burn-in and life test cool down procedures. When the burn-in and life tests are completed and prior to removal of bias voltages, the devices under test (DUT) shall be cooled to within 10°C of their power stable condition at room temperature; then, electrical parameter end-point measurements shall be performed.

4.5.3 Quiescent supply current. When performing quiescent supply current measurements (I_{CC}), the meter shall be placed so that all currents flow through the meter.

4.6 Data reporting. When specified in the purchase order or contract, a copy of the following data, as applicable, shall be supplied.

a. Attributes data for all screening tests (see 4.2) and variables data for all static burn-in, dynamic burn-in, RHA tests and steady-state life tests (see 3.6).

b. A copy of each radiograph.

c. The technology conformance inspection (TCI) data (see 4.4).

d. Parameter distribution data on parameters evaluated during burn-in (see 3.6).

e. Final electrical parameters data (see 4.2e).

f. RHA delta limits.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military service or Defense Agency, or within the military service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. PIN and compliance identifier, if applicable (see 1.2).

c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

d. Requirements for certificate of compliance, if applicable.

e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.

f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.

g. Requirements for product assurance and radiation hardness assurance options.

h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the PIN. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

i. Requirements for "JAN" marking.

j. Packaging requirements (see 5.1).

6.3 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractors parts lists.

6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

C_{IN} ..... Input terminal-to-GND capacitance
GND ..... Ground zero voltage potential
I_{CC} ..... Quiescent supply current
I_{IL} ..... Input current low
I_{IH} ..... Input current high
T_C ..... Case temperature
T_A ..... Ambient temperature
V_{CC} ..... Positive supply voltage
C_{PD} ..... Power dissipation capacitance
V_{IC} ..... Input clamp voltage
V_{GB} ..... Ground bounce voltage
O/V ..... Latch-up over-voltage
O/I ..... Latch-up over-current
t_w ..... Trigger duration (width)
$C_{I/O}$ ..... Input/output terminal-to-GND capacitance

6.6 Logistic support. Lead materials and finishes (see 3.5) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class S for National Aeronautics and Space Administration or class B for Department of Defense (see 1.2.2), lead material and finish A (see 3.5). Longer length leads and lead forming should not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges, post irradiation performance or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

Military device type	Generic-industry type
01 1/	54AC242
02 1/	54AC243
03	54AC245
04 1/	54AC620
05	54AC623
06	54AC640
07	54AC643
08	54AC646
09	54AC648

1/ These devices as of yet have not been characterized.

6.8 Changes from previous. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of changes.

CONCLUDING MATERIAL

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

Review activities:

Army - MI, SM
Navy - AS, CG, MC, SH, TD
Air Force 03, 19, 99

(Project 5962-1986)

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Bus Transceivers ***category:***

Click to view products by E2v ***manufacturer:***

Other Similar products are found below :

74LS645N DS8838 FXL4TD245UMX IDT74CBTLV3257PGG 74LVT245BBT20-13 5962-8683401DA PCA9617ADMR2G 5962-8953501KA 5962-86834012A 5962-7802301Q2A 5962-7802002MFA 5962-7802001MFA 74VHCV245FT(BJ) NCV7349D13R2G TC74VCX164245(EL,F MC74LCX245MNTWG TC7WPB8306L8X,LF(S TC7WPB9307FC(TE85L 74FCT16245CTPVG8 74FCT16543CTPVG 74FCT245CTPYG8 MM74HC245AMTCX 74LVCH16245APVG 74LVX245MTC 5962-9221405M2A NTS0102DP-Q100H 74ALVC16245MTDX 74ALVCH32245BF 74FCT163245APVG 74FCT245ATPYG8 74FCT245CTQG 74FCT3245AQG 74LCXR162245MTX 74VHC245M 74VHC245MX TC7WPB9306FC(TE85L TC7WPB9306FK(T5L,F JM38510/65553BRA ST3384EBDR 74LVC1T45GF,132 74AVC4TD245BQ,115 PQJ7980AHN/C0JL,51 MC100EP16VBDG FXL2TD245L10X 74LVC1T45GM,115 TC74AC245P(F) PSB21150F S LLHR SNJ54LS245FK SNJ54AHC245J SNJ54ABT245AFK