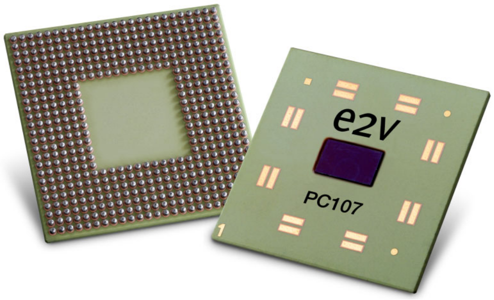
PC107A
PCI Bridge Memory Controller

Datasheet

Features

- Processor Bus Frequency up to 100 MHz
- 64- or 32-bit Data Bus and 32-bit Address Bus
- Provides Support for Either Asynchronous SRAM, Burst SRAM, or Pipelined Burst SRAM
- Compliant with PCI Specification, Revision 2.1
- PCI Interface Operates up to 66 MHz/5.0V Compatible
- IEEE® 1149.1 Compliant, JTAG Boundary-scan Interface
- PD Max = 1W (66 MHz), Full Operating Conditions
- Nap, Doze and Sleep Modes for Power Savings
- Two-channel Integrated DMA Controller
- Message Unit
  - Intelligent Input/Output (Two-wire Interface) Message Controller
  - Two Door Bell Registers
  - Inbound and Outbound Messaging Registers
- Inter-integrated Circuit (Two-wire Interface) Controller, Full Master/Slave Support
- Embedded Programmable Interrupt Controller (EPIC)
  - Five Hardware Interrupts (IRQs) or 16 Serial Interrupts
  - Four Programmable Timers



Description

The PC107A PCI Bridge/Integrated Memory Controller provides a bridge between the Peripheral Component Interconnect, (PCI) bus and PowerPC® 603e, PowerPC 740, PowerPC 750 or PC7400 microprocessors.

PCI support allows system designers to design systems quickly using peripherals already designed for PCI and other standard interfaces available in the personal computer hardware environment. The PC107A provides many other necessities for embedded applications including a high-performance memory controller and dual processor support, 2-channel flexible DMA controller, an interrupt controller, an I_2O-ready message unit, an inter-integrated circuit controller (Two-wire Interface), and low skew clock drivers. The PC107A contains an Embedded Programmable Interrupt Controller (EPIC) featuring five hardware interrupts (IRQ's) as well as sixteen serial interrupts along with four timers. The PC107A uses an advanced, 2.5V HiP3 process technology and is fully compatible with TTL devices.

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Screening

This product is manufactured in full compliance with:

- HiTCE CBGA according to e2v standards
- PBGA upscreening based upon e2v standards
- Full military temperature range (Tj = -55°C, +125°C)
- Industrial temperature range (Tj = -40°C, +110°C)

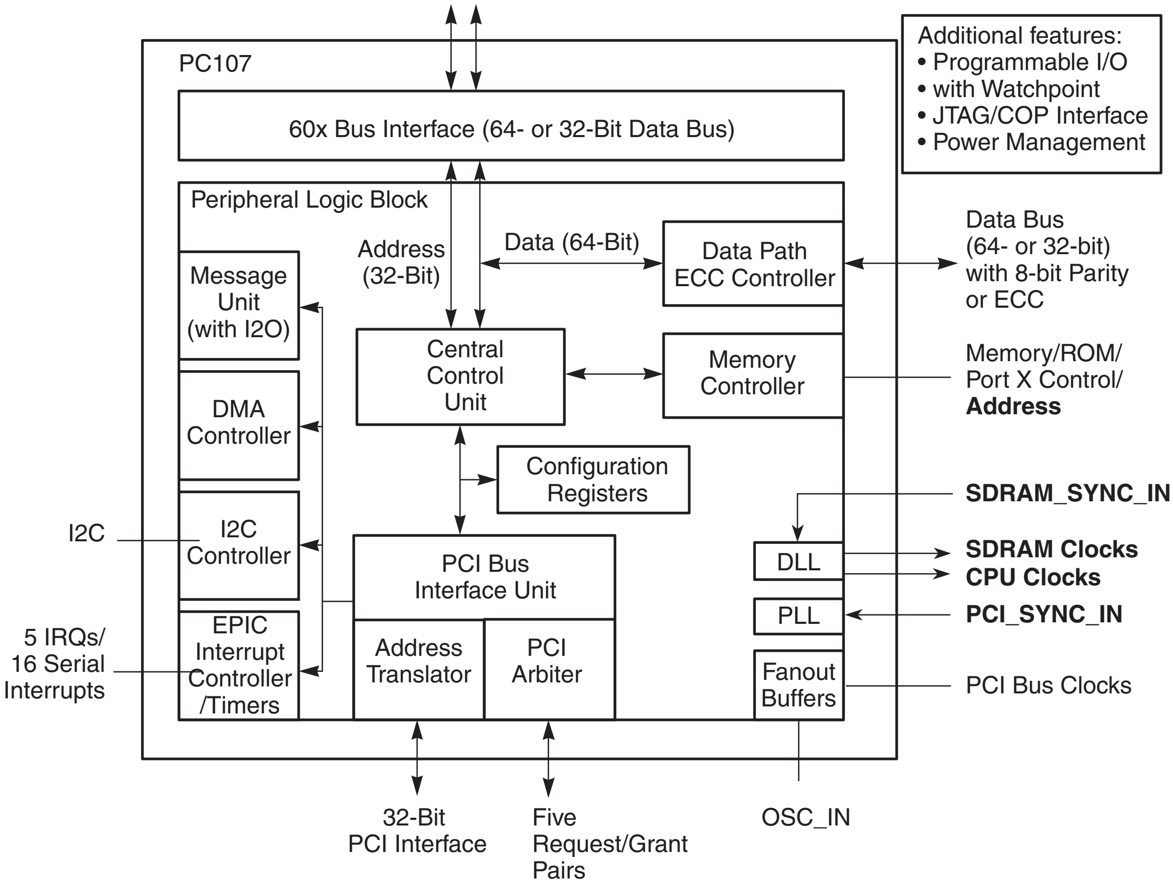
1. General Description

1.1 Simplified Block Diagram

The PC107A integrates a PCI bridge, memory controller, DMA controller, EPIC interrupt controller/timers, a message unit with an Intelligent Input/Output (I_2O) message controller, and an Inter-integrated Circuit (two-wire interface) controller. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

Figure 1-1 shows the major functional units within the PC107A. Note that this is a conceptual block diagram intended to show the basic features rather than an attempt to show how these features are physically implemented.

Figure 1-1. PC107A Block Diagram



1.1.1 General Parameters

The following list provides a summary of the general parameters of the PC107A:

Technology	0.29 µm CMOS, five-layer metal
Die size	50 mm^2
Transistor count	0.96 million
Logic design	Fully-static
Package	Surface mount 503 Plastic Ball Grid Array (C4/PBGA)
Core power supply	2.5 ±5% V DC (nominal; see Table 5-2 on page 12 for recommended operating conditions)
I/O power supply	3.0 to 3.6V DC

1.2 Features

The PC107A provides an integrated high-bandwidth, high-performance interface between up to two 60x processors, the PCI bus, and main memory. This section summarizes the features of the PC107A. Major features of the PC107A are as follows:

- Memory Interface
  - 64-/32-bit 100 MHz bus
  - Programmable timing supporting either FPM DRAM, EDO DRAM or SDRAM
  - High-bandwidth bus (32-/64-bit data bus) to DRAM
  - Supports one to eight banks of 4-, 16-, 64-, or 128-Mbit memory devices, and up to four banks of 256 Mbit SDRAM devices
  - Supports 1M byte to 1 Gbyte DRAM memory
  - 144M bytes of ROM space
  - 8-, 32-, or 64-bit ROM
  - Write buffering for PCI and processor accesses
  - Supports normal parity, read-modify-write (RMW), or ECC
  - Data-path buffering between memory interface and processor
  - Low-voltage TTL logic (LVTTL) interfaces
  - Port X: 8-, 32-, or 64-bit general-purpose I/O port using ROM controller interface with programmable address strobe timing
- 32-bit PCI Interface Operating up to 66 MHz
  - PCI 2.1-compliant
  - PCI 5.0V tolerance
  - Support for PCI locked accesses to memory
  - Support for accesses to PCI memory, I/O, and configuration spaces
  - Selectable big- or little-endian operation
  - Store gathering of processor-to-PCI write and PCI-to-memory write accesses
  - Memory prefetching of PCI read accesses
  - Selectable hardware-enforced coherency
  - PCI bus arbitration unit (five request/grant pairs)

  - PCI agent mode capability
  - Address translation unit
  - Some internal configuration registers accessible from PCI

- Two-channel Integrated DMA Controller (Writes to ROM/Port × Not Supported)
  - Supports direct mode or chaining mode (automatic linking of DMA transfers)
  - Supports scatter gathering-read or write discontinuous memory
  - Interrupt on completed segment, chain, and error
  - Local-to-local memory
  - PCI-to-PCI memory
  - PCI-to-local memory
  - PCI memory-to-local memory
- Message Unit
  - Two doorbell registers
  - An extended doorbell register mechanism that facilitates interprocessor communication through interrupts in a dual-local-processor system
  - Two inbound and two outbound messaging registers
  - I_2O message controller
- Two-wire Interface Controller with Full Master/Slave Support (Except Broadcast All)
- Embedded Programmable Interrupt Controller (EPIC)
  - Five hardware interrupts (IRQs) or 16 serial interrupts
  - Four programmable timers
- Integrated PCI Bus, CPU, and SDRAM Clock Generation
- Programmable PCI Bus, 60x, and Memory Interface Output Drivers
- Dynamic Power Management – Supports 60x Nap, Doze, and Sleep Modes
- Programmable Input and Output Signals with Watchpoint Capability
- Built-in PCI Bus Performance Monitor Facility
- Debug Features
  - Error injection/capture on data path
  - IEEE 1149.1 (JTAG)/test interface
- Processor Interface
  - Supports up to two PowerPC microprocessors with 60x bus interface
  - Supports various operating frequencies and bus divider ratios
  - 32-bit address bus, 64/32-bit data bus supported at 100 MHz
  - Supports full memory coherency
  - Supports optional local bus slave
  - Decoupled address and data buses for pipelining of 60x accesses
  - Store gathering on 60x-to-PCI writes
  - Concurrent transactions on 60x and PCI buses supported

2. Pin Assignments

2.1 Pinout Listings

Table 2-1 provides the pinout listing for the PC107A, 503 PBGA package.

Table 2-1. PC107A Pinout Listing

Signal Name	Package Pin Number	Pin Type	Supply Voltage	Output Driver Type	Notes
60x Processor Interface Signals					
A[0–31]	AE22, AE16, AA14, AE17, AD21, AD14, AD20, AB16, AB20, AB15, AA20, AD13, Y15, AE12, AD15, AB9, AB14, AA8, AC13, Y12, Y11, AE15, AE13, AA16, Y13, AB8, AD12, AE10, AB13, Y9, Y8, AD9	I/O	BV_{DD}	DRV_CPU	(4)
$\overline{\text{AACK}}$	AC7	Output	BV_{DD}	DRV_CPU	
$\overline{\text{ARTRY}}$	Y7	I/O	BV_{DD}	DRV_CPU	(15)
$\overline{\text{BG0}}$	AE11	Output	BV_{DD}	DRV_CPU	
$\overline{\text{BG1}}$	AD11	Output	BV_{DD}	DRV_CPU	
$\overline{\text{BR0}}$	AB17	Input	BV_{DD}	–	
$\overline{\text{BR1}}$	Y14	Input	BV_{DD}	–	(10)
$\overline{\text{CI}}$	AD16	I/O	BV_{DD}	DRV_CPU	
$\overline{\text{DBG0}}$	AC10	Output	BV_{DD}	DRV_MEM_ADDR	
$\overline{\text{DBG1}}$	AD10	Output	BV_{DD}	DRV_MEM_ADDR	
$\overline{\text{DBGLB}}$	AB10	Output	BV_{DD}	DRV_MEM_ADDR	
DH[0–31]	P1, R1, P2, T4, T1, T3, R4, P6, U6, V5, V2, T5, U1, R6, W1, V4, W2, U4, T2, V6, W3, W5, Y1, Y2, Y4, Y5, AA1, AA2, AA4, AB1, AB3, AB4	I/O	BV_{DD}	DRV_CPU	(4)
DL[0–31]	AA7, W6, AB6, AA6, AB5, AC4, AD3, AB7, AE1, W4, N6, M1, N3, N4, N5, N1, M2, R2, V1, P5, P4, N2, U2, AE4, AE6, AE2, AE3, AE7, AD5, AB2, AC2, AC1	I/O	BV_{DD}	DRV_CPU	(4)
DP[0–7]	AE9, AD6, AD8, AD1, AE8, AD7, AD4, AE5	I/O	BV_{DD}	DRV_CPU	(4)
$\overline{\text{GBL}}$	AD17	I/O	BV_{DD}	DRV_CPU	
$\overline{\text{LBCLAIM}}$	Y17	Input	BV_{DD}		
$\overline{\text{TA}}$	AE14	I/O	BV_{DD}	DRV_CPU	(15)
$\overline{\text{TBST}}$	AE21	I/O	BV_{DD}	DRV_CPU	
$\overline{\text{TEA}}$	AB11	Output	BV_{DD}	DRV_CPU	
$\overline{\text{TS}}$	AA10	I/O	BV_{DD}	DRV_CPU	(15)
TSIZ[0–2]	AE19, AD18, AB18	I/O	BV_{DD}	DRV_CPU	(4)

Table 2-1. PC107A Pinout Listing (Continued)

Signal Name	Package Pin Number	Pin Type	Supply Voltage	Output Driver Type	Notes
TT[0–4]	AD19, AC19, AB19, AA19, AA18	I/O	BV_{DD}	DRV_CPU	(4)
$\overline{\text{WT}}$	AC16	I/O	BV_{DD}	DRV_CPU	
PCI Interface Signals					
AD[31–0]	N23, N21, M20, M21, M22, M24, M25, L20, L22, K25, K24, K23, K21, J20, J24, J25, H20, F24, E25, F21, E24, E22, D25, A25, B25, A23, B23, B22, C22, C25, D23, D21	I/O	OV_{DD}	DRV_PCI	(4)(11)
$\overline{\text{C/BE}}$[3–0]	L24, J22, G22, A24,	I/O	OV_{DD}	DRV_PCI	(4)(11)
$\overline{\text{DEVSEL}}$	G23	I/O	OV_{DD}	DRV_PCI	(6)(11)
$\overline{\text{FRAME}}$	G20	I/O	OV_{DD}	DRV_PCI	(6)(11)
$\overline{\text{GNT}}$[4–0]	T24, P22, P21, R22, N20	Output	OV_{DD}	DRV_PCI	(4)(11)
IDSEL	L25	Input	OV_{DD}	–	
$\overline{\text{INTA}}$	V21	Output	OV_{DD}	DRV_PCI	(6)(11)(12)
$\overline{\text{IRDY}}$	H24	I/O	OV_{DD}	DRV_PCI	(6)(11)
$\overline{\text{LOCK}}$	G21	Input	OV_{DD}	–	(6)
PAR	G24	I/O	OV_{DD}	DRV_PCI	(11)
$\overline{\text{PERR}}$	G25	I/O	OV_{DD}	DRV_PCI	(6)(11)(13)
$\overline{\text{REQ}}$[4–0]	W25, V25, U25, T25, T23	Input	OV_{DD}	–	(10)
$\overline{\text{SERR}}$	F25	I/O	OV_{DD}	DRV_PCI	(6)(11)(12)
$\overline{\text{STOP}}$	H21	I/O	OV_{DD}	DRV_PCI	(6)(11)
$\overline{\text{TRDY}}$	H25	I/O	OV_{DD}	DRV_PCI	(6)(11)
Memory Interface Signals					
$\overline{\text{AS}}$	A4	Output	GV_{DD}	DRV_MEM_ADDR	
$\overline{\text{CAS}}$/DQM[0–7]	A2, B1, A11, A10, B3, C2, F12, D11	Output	GV_{DD}	DRV_MEM_ADDR	(4)
CKE	A12	Output	GV_{DD}	DRV_MEM_ADDR	(1)
$\overline{\text{FOE}}$	A13	I/O	GV_{DD}	DRV_MEM_ADDR	(1)(2)
MDH[0–31]	M6, L4, L6, K2, K4, K5, J4, J6, H4, H5, G3, G5, G6, F5, F1, E1, B14, D15, B15, E16, D16, C16, D18, D17, B17, F18, E19, E20, B19, B20, B21, A22	I/O	GV_{DD}	DRV_MEM_DATA	(4)
MDL[0–31]	M5, L1, L2, K1, K3, J1, J2, H1, H2, H6, G2, G4, F4, G1, F2, E2, F14, F15, A16, F17, B16, A17, A18, A19, B18, E18, D19, F19, A20, C19, D20, A21	I/O	GV_{DD}	DRV_MEM_DATA	(3)(4)
PAR/AR[0–7]	D2, C1, A15, A14, D1, D3, F13, C13	I/O	GV_{DD}	DRV_MEM_DATA	(4)
$\overline{\text{RAS/CS}}$[0–7]	E6, C4, D5, E4, C10, F11, B10, B11	Output	GV_{DD}	DRV_MEM_ADDR	(4)
$\overline{\text{RCS0}}$	D10	I/O	GV_{DD}	DRV_MEM_ADDR	(1)(2)

Table 2-1. PC107A Pinout Listing (Continued)

Signal Name	Package Pin Number	Pin Type	Supply Voltage	Output Driver Type	Notes
$\overline{\text{RCS1}}$	B9	Output	GV_{DD}	DRV_MEM_DATA	
$\overline{\text{RCS2}}$	B5	Output	GV_{DD}	DRV_MEM_ADDR	
$\overline{\text{RCS3}}$	D7	Output	GV_{DD}	DRV_MEM_ADDR	
SDBA0	A9	Output	GV_{DD}	DRV_MEM_ADDR	(1)(2)
SDBA1	A8	Output	GV_{DD}	DRV_MEM_ADDR	
$\overline{\text{SDCAS}}$	D4	Output	GV_{DD}	DRV_MEM_ADDR	(1)
SDMA[13–0]	E10, F9, D9, F8, E8, D8, B8, E7, C7, B7, A7, B6, A6, A5	Output	GV_{DD}	DRV_MEM_ADDR	(4)(5)
$\overline{\text{SDRAS}}$	B4	Output	GV_{DD}	DRV_MEM_ADDR	(1)
$\overline{\text{WE}}$	A3	Output	GV_{DD}	DRV_MEM_ADDR	
EPIC Control Signals					
$\overline{\text{INT}}$	Y22	Output	OV_{DD}	DRV_CPU	(16)
IRQ_0 / S_INT	U24	Input	OV_{DD}	–	
IRQ_1 / S_CLK	C24	I/O	OV_{DD}	DRV_PCI	
IRQ_2 / S_RST	T21	I/O	OV_{DD}	DRV_PCI	
IRQ_3 / S_FRAME	U20	I/O	OV_{DD}	DRV_PCI	
IRQ_4/ L_INT	V22	I/O	OV_{DD}	DRV_PCI	
Two-wire Interface Control Signals					
SCL	AB25	I/O	OV_{DD}	DRV_CPU	(8)(12)
SDA	AB24	I/O	OV_{DD}	DRV_CPU	(8)(12)
Clock Signals					
CKO	V20	Output	OV_{DD}	DRV_PCI	
CPU_CLK[0–2]	AA12, AA13, AB12	Output	BV_{DD}	DRV_MEM_ADDR	(4)
OSC_IN	U22	Input	OV_{DD}	–	
PCI_CLK[0–4]	R25, P24, R24, N24, N25	Output	OV_{DD}	DRV_MEM_ADDR	(4)
PCI_SYNC_IN	P20	Input	OV_{DD}	–	
PCI_SYNC_OUT	P25	Output	OV_{DD}	DRV_MEM_ADDR	
SDRAM_CLK[0–3]	D14, D13, E12, E14	Output	GV_{DD}	DRV_MEM_ADDR	(4)
SDRAM_SYNC_IN	E13	Input	GV_{DD}	–	
SDRAM_SYNC_OUT	D12	Output	GV_{DD}	DRV_MEM_ADDR	
Miscellaneous Signals					
$\overline{\text{HRESET}}$	AA23	Input	OV_{DD}	–	
$\overline{\text{HRESET\_CPU}}$	AB21	Output	BV_{DD}	DRV_CPU	(10)(12)
$\overline{\text{MCP}}$	AE20	Output	OV_{DD}	DRV_CPU	(12)(16)
NMI	AC25	Input	OV_{DD}	–	

Table 2-1. PC107A Pinout Listing (Continued)

Signal Name	Package Pin Number	Pin Type	Supply Voltage	Output Driver Type	Notes
$\overline{\text{QACK}}$	AE18	Output	BV_{DD}	DRV_CPU	(10)
$\overline{\text{QREQ}}$	M4	Input	BV_{DD}	–	
$\overline{\text{SRESET}}$	Y18	Output	BV_{DD}	DRV_CPU	(10)
Test/Configuration Signals					
PLL_CFG[0–3]	AC22, AD23, AD22, AE23	Input	OV_{DD}	–	(2)(4)
TCK	W24	Input	OV_{DD}	–	(7)(10)
TDI	Y25	Input	OV_{DD}	–	(7)(10)
TDO	W23	Output	OV_{DD}	DRV_PCI	
$\overline{\text{TEST}}$	AA25	Input	OV_{DD}	–	(7)(10)
$\overline{\text{TEST1}}$	V24	Input	OV_{DD}	–	(8)
$\overline{\text{TEST2}}$	D6	Input	GV_{DD}	–	(9)
TMS	Y24	Input	OV_{DD}	–	(7)(10)
TRIG_IN	W22	Input	OV_{DD}	–	
TRIG_OUT	W21	Output	OV_{DD}	DRV_CPU	(10)
$\overline{\text{TRST}}$	AA24	Input	OV_{DD}	–	(7)(10)(14)
Power and Ground Signals					
AV_{DD}	AE24	Input	–	–	
GND	AA21, AB22, AC11, AC14, AC17, AC20, AC23, AC3, AC5, AC8, AD24, AE25, C12, C15, C18, C21, C23, C3, C6, C9, E3, F10, F16, F20, F23, F6, G11, G13, G15, G18, G8, H19, H3, H7, J23, K20, K6, L19, L3, L7, M23, N19, N7, P3, R19, R23, R7, T20, T6, U3, V19, V23, V7, W11, W13, W15, W18, W8, Y10, Y16, Y19, Y20, Y3, Y6	Input	–	–	
GV_{DD}	B2, C5, C8, C11, C14, C17, C20, E5, E9, E11, E15, E17, F3, G7, G9, G12, G14, G17, G19, J3, J5, J7, L5, M3, M7	Input	–	–	
LAV_{DD}	F7	Input	–	–	
LV_{DD}	D22, F22, H22, K22, N22, T22	Input	–	–	
OV_{DD}	B24, E21, E23, H23, J19, J21, L21, L23, M19, P19, P23, R21, U19, U21, U23, Y23	Input	–	–	
BV_{DD}	P7, R3, R5, U5, U7, V3, W7, W9, W12, W14, W17, AA3, AA5, AA9, AA11, AA15, AA17, AC6, AC9, AC12, AC15, AC18, AC21, AD2	Input	–	–	
V_{DD}	K19, W16, T19, G10, G16, K7, T7, W10, W19, W20, Y21, AA22, AB23, AC24, AD25	Input	–	–	

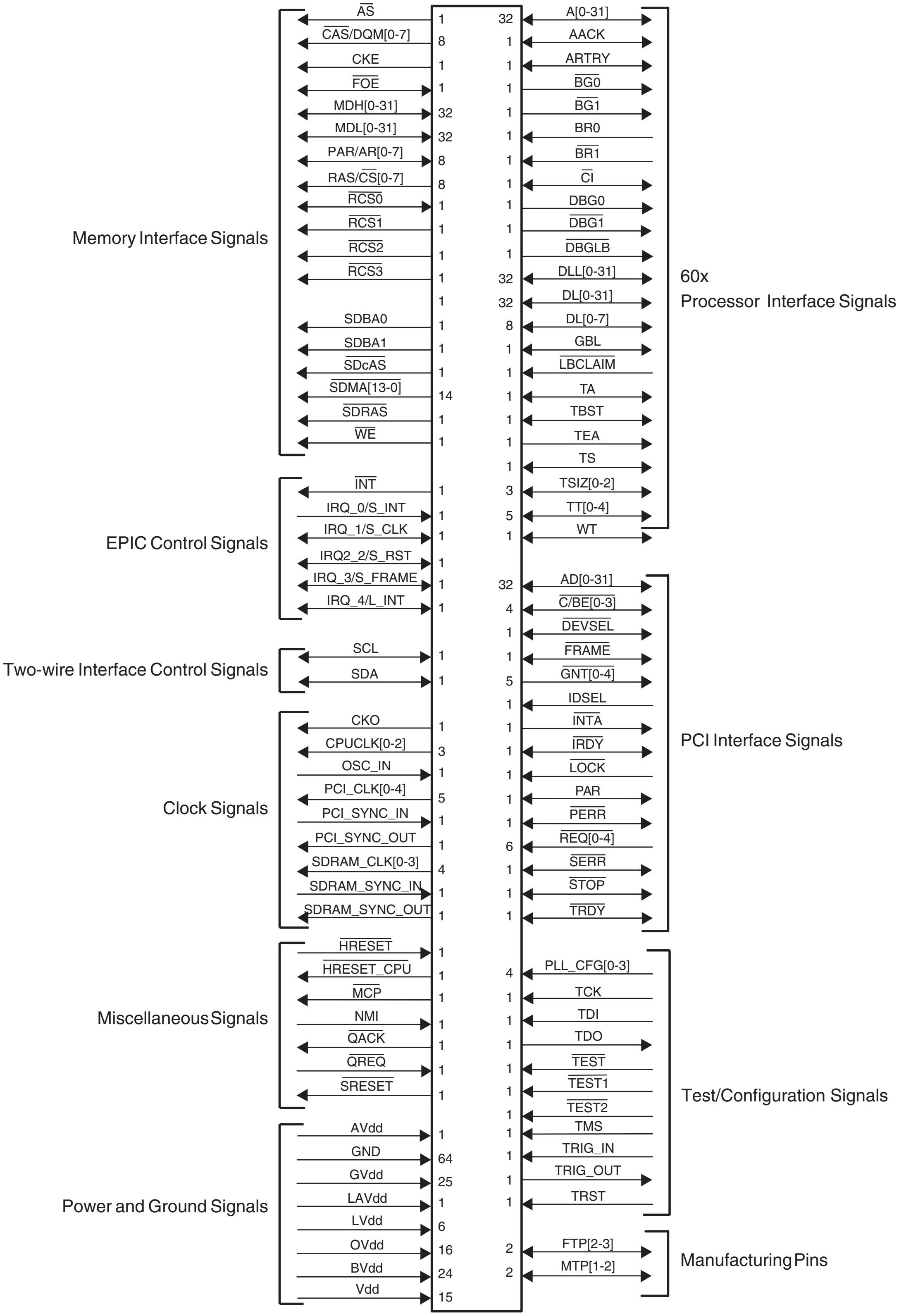
Table 2-1. PC107A Pinout Listing (Continued)

Signal Name	Package Pin Number	Pin Type	Supply Voltage	Output Driver Type	Notes
Manufacturing Pins					
FTP[2–3]	R20, D24	I/O	OV_{DD}	DRV_PCI	(4)(8)
MTP[1–2]	B12, B13	I/O	GV_{DD}	DRV_MEM_ADDR	(4)(9)

Notes:
1. This pin has an internal pull-up resistor which is enabled only when the PC107A is in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a logic "1" is read into configuration bits during reset.
2. This pin is a reset configuration pin.
3. MDL[0] is a reset configuration pin and has an internal pull-up resistor which is enabled only when the PC107 is in the reset state.The value of the internal pull-up resistor is not guaranteed, but is sufficient to insure that a logic '1' is read into configuration bits during reset.
4. Multi-pin signals such as AD[0–31] or DL[0–31] have their physical package pin numbers listed in order corresponding to the signal names. Ex: AD0 is on pin D21, AD1 is on pin D23,... AD31 is on pin N23.
5. SDMA[10–1] are reset configuration pins and have internal pull-up resistors which are enabled only when the PC107 is in the reset state.The values of the internal pull-up resistors is not guaranteed, but are sufficient to ensure that logic "1"s are read into the configuration bits during reset.
6. Recommend a weak pull-up resistor (2 kΩ– 10 kΩ) be placed on this PCI control pin to LV_{DD}.
7. V_{IH} and V_{IL} for these signals are the same as the PCI V_{IH} and V_{IL} entries in Table 7-1, “DC Electrical Specifications.”
8. Recommend a weak pull-up resistor (2 kΩ – 10 kΩ) be placed on this pin to OV_{DD}.
9. Recommend a weak pull-up resistor (2 kΩ – 10 kΩ) be placed on this pin to GV_{DD}.
10. This pin has an internal pull-up resistor; the value of the internal pull-up resistor is not guaranteed, but is sufficient to prevent unused inputs from floating.
11. This pin is affected by programmable PCI_HOLD_DEL parameter, see “PCI Signal Output Hold Timing” on page 28.”
12. This pin is an open drain signal.
13. This pin is a sustained tri-state pin as defined by the *PCI Local Bus Specification.*
14. See “Connection Recommendations” on page 42 for additional information on this pin.
15. A weak pull-up resistor is recommend (2 kΩ – 10 kΩ) to be placed on this pin to BV_{DD}.
16. If BV_{DD} = 2.5V ±5%, this microprocessor interface pin needs to be DC voltage level shifted from OV_{DD} (3.3 ±0.3V) to 2.5V ±5%; this can typically be accomplished with a two resistor voltage divider circuit since the signal is an output only signal.

3. Signal Description

Figure 3-1. PC107A Microprocessor Signal Groups



4. Detailed Specification

This specification describes the specific requirements for the PC107A, in compliance with e2v standard screening.

5. Applicable Documents

1. MIL-STD-883: Test methods and procedures for electronics.
2. SQ32S0100.0: Quality levels for supplied components.

The microcircuits are in accordance with the applicable documents and as specified herein.

5.1 Design and Construction

5.1.1 Terminal Connections

The terminal connections are shown in Table 2-1 on page 5.

5.2 Absolute Maximum Ratings

The tables in this section describe the PC107A DC electrical characteristics. Table 5-1 provides the absolute maximum ratings.

Table 5-1. Absolute Maximum Ratings

Symbol	Characteristic(1)	Value	Unit
V_{DD}	Supply Voltage – Core	-0.3 to 2.75	V
GV_{DD}	Supply Voltage – Memory Bus Drivers	-0.3 to 3.6	V
BV_{DD}	Supply Voltage – Processor Bus Drivers	-0.3 to 3.6	V
OV_{DD}	Supply Voltage – PCI and Standard I/O Buffers	-0.3 to 3.6	V
AV_{DD}/LAV_{DD}	Supply Voltage – PLLs and DLL	-0.3 to 2.75	V
LV_{DD}	Supply Voltage – PCI Reference	-0.3 to 5.4	V
V_{IN}	Input Voltage(2)	-0.3 to 3.6	V
T_J	Operational Die-Junction Temperature Range	-55 to 125	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C

Notes:
1. Functional and tested operating conditions are given in Table 5-2. Absolute maximum ratings are stress ratings only and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. PCI inputs with LV_{DD} = 5V ± 5% V DC may be correspondingly stressed at voltages exceeding LV_{DD} + 0.5V DC.

5.3 Recommended Operating Conditions

Table 5-2 provides the recommended operating conditions for the PC107A.

Table 5-2. Recommended Operating Conditions

Symbol	Characteristic		Recommended Value	Unit	Notes
V_{DD}	Supply Voltage		2.5 ±5%	V	(4)
GV_{DD}	Supply Voltages for Memory Bus Drivers		3.3 ±5%	V	(6)
BV_{DD}	Supply Voltages for Processor Bus Drivers		3.3 ±5%	V	(6)
			2.5 ±5%		
OV_{DD}	I/O Buffer supply for PCI and Standard		3.3 ±0.3	V	(4)
AV_{DD}	PLL Supply Voltage		2.5 ±5%	V	(5)
LAV_{DD}	DLL Supply Voltage		2.5 ±5%	V	(5)
LV_{DD}	PCI Reference		5.0 ±5%	V	(7)(8)
			3.3 ±0.3	V	(7)(8)
V_{IN}	Input Voltage	PCI Inputs	0 to 3.6 or 5.75	V	(1)(2)
		All Other Inputs	0 to 3.6	V	(3)
T_J	Die-Junction Temperature		-55°C to 125°C	°C	

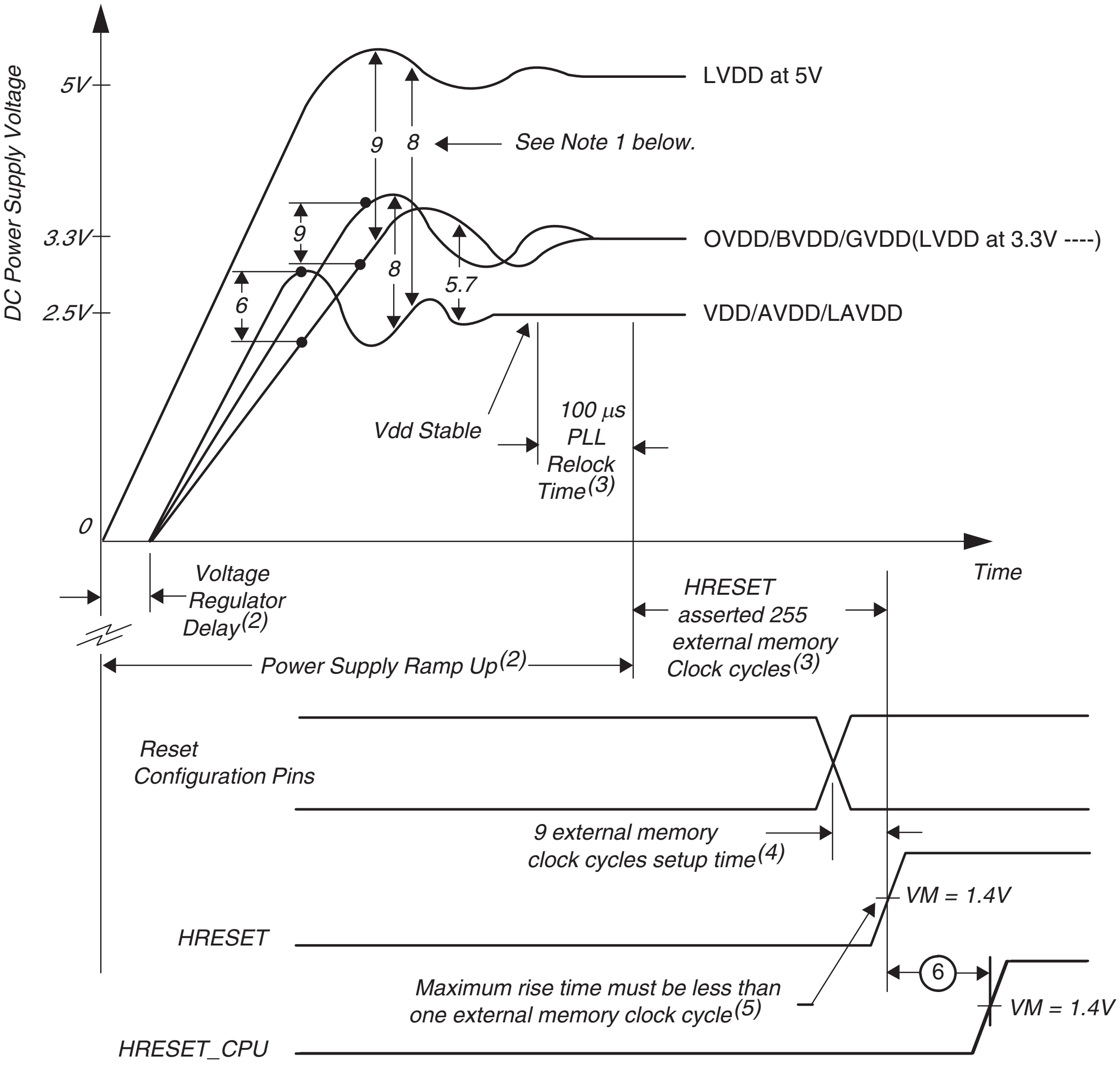
Notes:
1. PCI pins are designed to withstand LV_{DD} + 0.5V DC when LV_{DD} is connected to a 5.0V DC power supply.
2. PCI pins are designed to withstand LV_{DD} + 0.5V DC when LV_{DD} is connected to a 3.3V DC power supply.

Cautions:

3. Input voltage (V_{IN}) must not be greater than the supply voltage ($V_{DD}/AV_{DD}/LAV_{DD}$) by more than 2.5V at all times, including during power-on reset.
4. OV_{DD} must not exceed $V_{DD}/AV_{DD}/LAV_{DD}$ by more than 1.8V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. $V_{DD}/AV_{DD}/LAV_{DD}$ must not exceed OV_{DD} by more than 0.6V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. BV_{DD}/GV_{DD} must not exceed $V_{DD}/AV_{DD}/LAV_{DD}$ by more than 1.8V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. LV_{DD} must not exceed $V_{DD}/AV_{DD}/LAV_{DD}$ by more than 5.4V at any time including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences
8. LV_{DD} must not exceed OV_{DD} by more than 3.6V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

Figure 5-1 shows the supply voltage sequencing and separation cautions.

Figure 5-1. Supply Voltage Sequencing and Separation Cautions



Notes:
1. Numbers associated with waveform separations correspond to caution numbers listed in Table 5-2, “Recommended Operating Conditions,” on page 12.
2. Refer to “Power Supply Voltage Sequencing” on page 41 for additional information.
3. Refer to Table 7-4 on page 24 for additional information on PLL Relock and reset signal assertion timing requirements.
4. Refer to Table 7-5 on page 25 for additional information on reset configuration pin setup timing requirements.
5. $\overline{\text{HRESET}}$ must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the non-reset state.
6. $\overline{\text{HRESET\_CPU}}$ negates 2^{17} memory clock cycles after $\overline{\text{HRESET}}$ negates.

Figure 5-2 shows the undershoot and overshoot voltage of the memory interface of the PC107A.

Figure 5-2. Overshoot/Undershoot Voltage

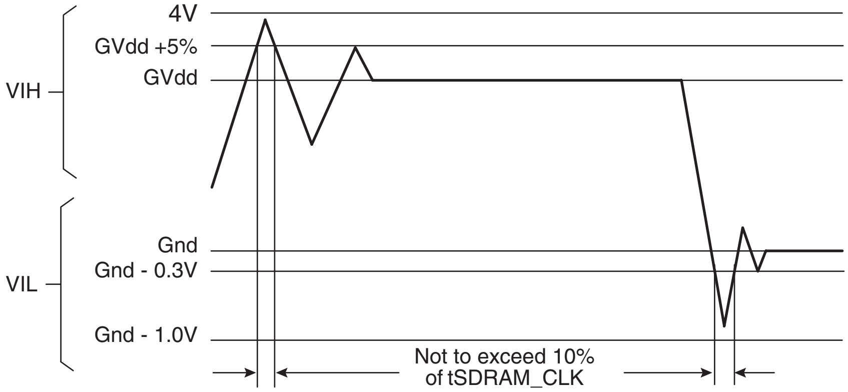


Figure 5-3 and Figure 5-4 show the undershoot/overshoot voltage of the PCI interface for 3.3 and 5V signals, respectively.

Figure 5-3. Maximum AC Waveforms for 3.3V Signaling

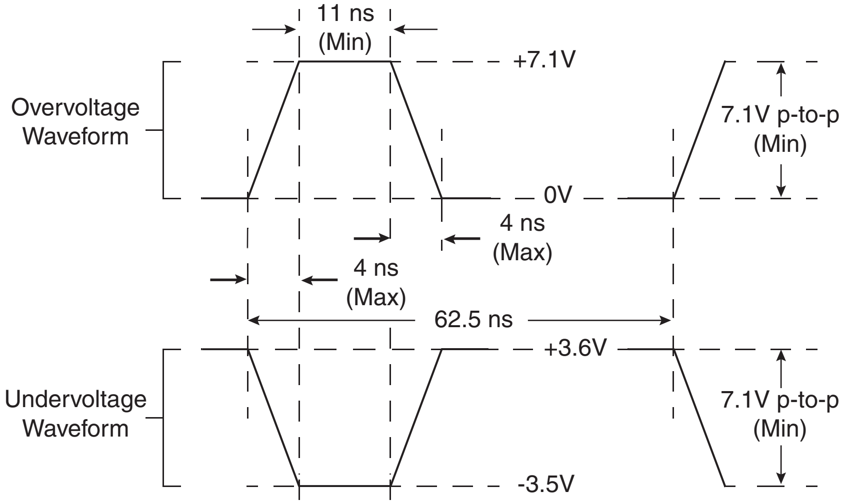
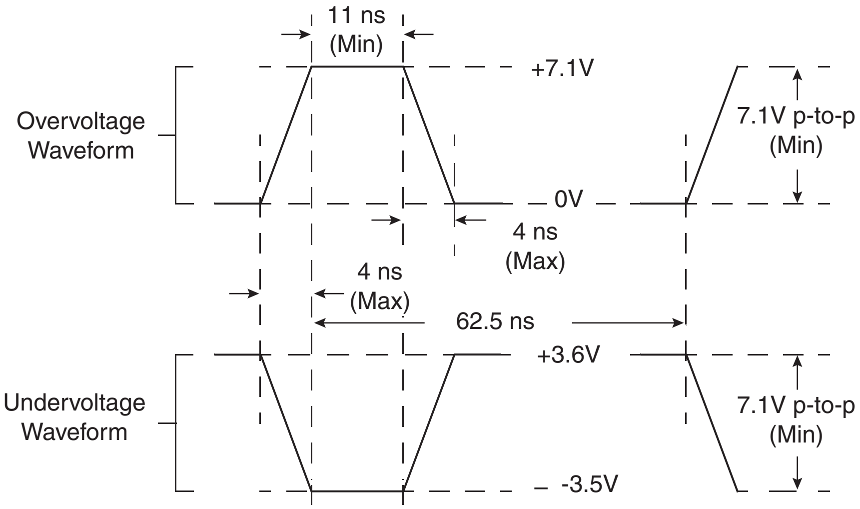


Figure 5-4. Maximum AC Waveforms for 3.3V Signaling



6. Thermal Information

6.1 Package Characteristics

Table 6-1 provides the package thermal characteristics for the PC107A.

Table 6-1. FC-PBGA Package Thermal Characteristics

Symbol	Characteristic(1)	Value	Unit
$R\theta_{JA}$	Junction-to-ambient natural convection(1)(2) (Single-layer board-1s)	30	°C/W
$R\theta_{JMA}$	Junction-to-ambient natural convection(1)(3) (Four-layer board-2s2p)	26	°C/W
$R\theta_{JMA}$	Junction-to-ambient (at 200 ft/min)(1)(3) (Single-layer board-1s)	25	°C/W
$R\theta_{JMA}$	Junction-to-ambient (at 200 ft/min)(1)(3) (Four-layer board-2s2p)	22	°C/W
$R\theta_{JB}$	Junction-to-board(4)	20	°C/W
$R\theta_{JC}$	Junction-to-case(5)	< 0.1	°C/W

Note:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface without thermal grease.

6.1.1 Package Thermal Characteristics for HiTCE

Table 6-2 provides the package thermal characteristics for the PC107 HiTCE.

Table 6-2. Package Thermal Characteristics for HiTCE Package(1)

Characteristic	Value	Unit
	PC107 HiTCE	
Thermal resistance junction to case(2)	0.295	°C/Watt
Thermal resistance junction to bottom of balls	15.8	°C/Watt
Thermal resistance junction to board, Jedec JESD51-8 (2s2p board)	18.4	°C/Watt
Thermal resistance junction to ambient, Jedec JESD51-2 (2s2p board = 2 signals + 2 power planes in board)	26.3	°C/Watt

Notes:
1. Nominal values: means computed with nominal geometry and nominal thermal conductivities of materials as given in legend of each simulation results.
2. In this case thermal resistance junction to case is thermal resistance junction to top of Silicon die, and value almost not depend from substrate used for land grid array. Value depends strongly on heating zone size in Silicon chip assumption. In present simulations heating zone is 5.8 mm × 3.65 mm that is 42% of die size. Assuming the full die size as uniformly power dissipating is not realistic.
   Assuming 8.3 mm × 5.15 mm heating zone (85% of die surface) leads to 0.15°C/watt instead of 0.29°C/watt.

6.1.2 Thermal Management Information

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Table 6-1 has four junction-to-ambient thermal resistances ($R_{\theta JA}$ or $R_{\theta JMA}$). Two test boards are used: single-signal-layer (1s) and four-layer boards with two internal planes (2s2p). Which value is closer to the application depends on the system board thermal resistance and the density of other high-power dissipation components.

To illustrate the process, determine the junction temperature based on the values provided in Table 6-1 for an PC107 that is mounted on a board with many internal planes using arbitrary values. If the PC107 is doing most of the power dissipation, use $R_{\theta JMA}$ of 26°C/W given in Table 6-1. The ambient temperature near the device is 45°C. Suppose the total typical power dissipation at 100 MHz core frequency is 2.1W (see Table 6-3). The junction temperature is:

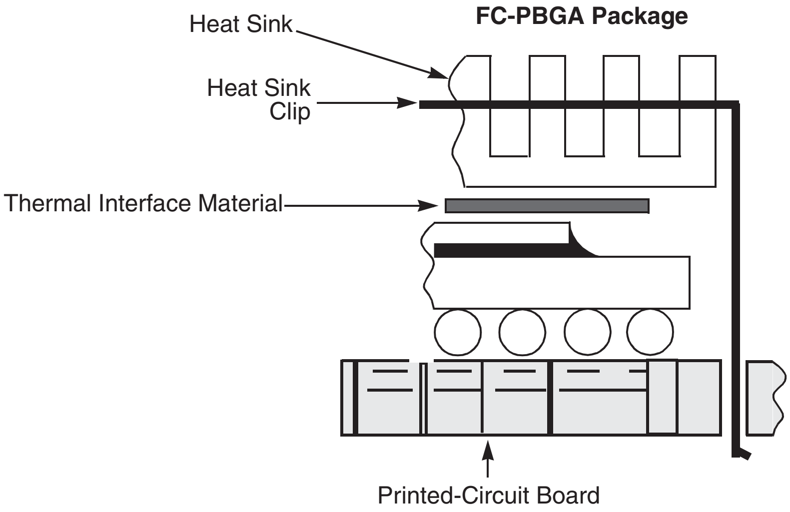
$$T_J = 45 + (2.1 \times 26) = 100°C.$$

If this value is less than the maximum junction temperature noted in Table 5-1, the PC107 will not need a heat sink. If the ambient temperature is higher or the power dissipation is higher because of faster bus speed, the device will probably need a heat sink.

The PC107 may need a heat sink depending on the system. This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design–the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods–spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (see Figure 6-1); however, due to the potential large mass of the heat sink, attachment through the printed-circuit board is suggested. The force of the heat sink on the die should not exceed 6 lb.

The heat sink surface must be flat without protrusions and must be parallel with the die as the heat sink is brought into contact to avoid chipping the edges of the die and the heat sink. Because of the small contact area of the heat sink, it is suggested that the mounting force be centered over the die.

Figure 6-1. Package Exploded Cross-Sectional View with Several Heat Sink Options



The board designer can choose between several types of heat sinks to place on the PC107. There are several commercially available heat sinks for the PC107 provided by the listvendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277

Tyco® Electronics Chip Coolers P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering® 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

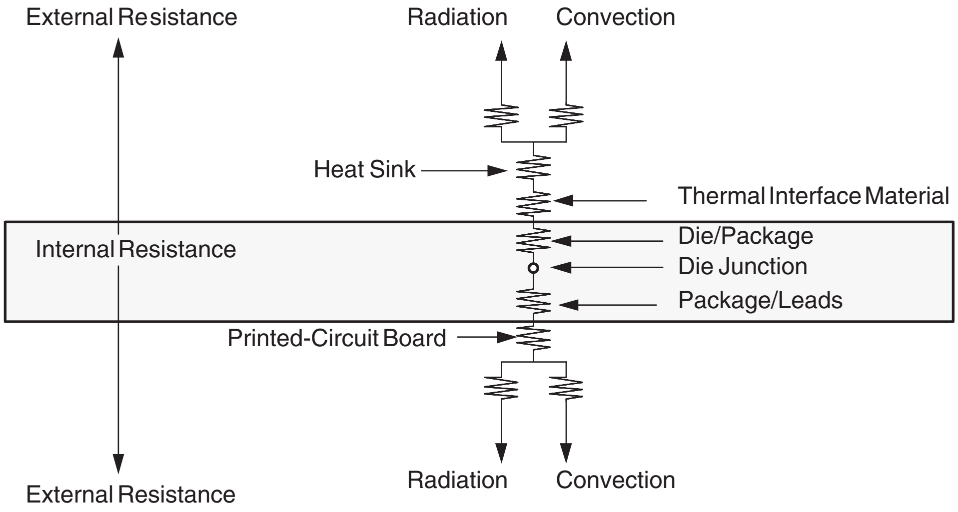
6.1.3 Internal Package Conduction Resistance

For the PBGA packaging technology, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance,
- The die junction-to-ball thermal resistance.

Figure 6-2 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 6-2. C4 Package with Heat Sink Mounted to a Printed-Circuit Board



Note: The internal versus external package resistance

For this PBGA package, heat is dissipated from the component via several concurrent paths. Heat is conducted through the silicon and may be removed to the ambient air by convection and/or radiation. In addition, a second, parallel heat flow path exists by conduction in parallel through the C4 bumps and the epoxy under-fill, to the plastic substrate for further convection cooling off the edges. Then from the plastic substrate, heat is conducted via the leads/balls to the next-level interconnect (printed-circuit board) whereupon the primary mode of heat transfer is by convection and/or radiation.

6.2 Power Characteristics

Table 6-3 provides the preliminary power consumption estimates for the PC107A. Power consumption on the PLL supply pin (AV_{DD}) and the DLL supply pin (LAV_{DD}) < 15 mW. This information is based on characterization data.

Table 6-3. Power Consumption

Mode	PCI_SYNC_IN/Core Frequency (MHz)								Unit	Notes
	25/50		33/33		33/66		66/100			
	V_{DD} Power	I/O Power	V_{DD} Power	I/O Power	V_{DD} Power	I/O Power	V_{DD} Power	I/O Power		
Typical	468	923	351	759	644	1087	933	1122	mW	(1)(2)
Doze	176	697	118	636	235	800	350	915	mW	(1)(2)
Nap	139	744	93	693	185	420	276	970	mW	(1)(2)
Sleep	79	718	45	677	102	841	138	939	mW	(1)(2)

Notes: 1. Power is measured with V_{DD} = 2.625V, GV_{DD} = OV_{DD} = BV_{DD} = 3.45V at 0°C and one DIMM populated in test system.

2. All clock drivers enabled.

7. Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the PC107A.

7.1 Static Characteristics

7.1.1 DC Electrical Specification

Table 7-1 provides the DC electrical characteristics for the PC107A. At recommended operating conditions (see Table 5-2 on page 12)

Table 7-1. DC Electrical Specifications

Characteristics	Conditions[1]	Symbol	Value Min	Value Max	Unit
Input High Voltage[2][3]	PCI only	V_{IH}	0.65*OV_{DD}[3]	LV_{DD}	V
Input Low Voltage	PCI only	V_{IL}	–	0.3*OV_{DD}	V
Input High Voltage[2]	All other pins (GV_{DD} = 3.3V)	V_{IH}	2.0	–	V
Input High Voltage[2]	All other pins (BV_{DD} = 2.5V)	V_{IH}	1.7	–	V
Input Low Voltage	All inputs except PCI_SYNC_IN	V_{IL}	GND	0.8	V
PCI_SYNC_IN Input High Voltage		CV_{IH}	2.4	–	V
PCI_SYNC_IN Input Low Voltage		CV_{IL}	GND	0.4	V
Input Leakage Current for pins using DRV_PCI driver[4]	$0.5V \le V_{IN} \le 2.7V$ at LV_{DD} = 4.75	I_L	–	± 70	µA
Input Leakage Current all others[4]	LV_{DD} = 3.6V ($GV_{DD} \le 3.465$)	I_L	–	± 10	µA
Output High Voltage[5]	I_{OH} = Driver Dependent[5] (GV_{DD} = 3.3V)	V_{OH}	2.4	–	V
Output Low Voltage[5]	I_{OL} = Driver Dependent[5] (GV_{DD} = 3.3V)	V_{OL}	–	0.4	V
Output High Voltage[5]	I_{OH} = Driver Dependent[5] (BV_{DD} = 2.5V) All outputs except CPU_CLKS[0-2]	V_{OH}	1.85	–	V
	I_{OH} = Driver Dependent[5] (BV_{DD} = 2.5V) CPUCLKS[0-2] Only	V_{OH}	2.0	–	V
Output Low Voltage[5]	I_{OL} = Driver Dependent[5] (BV_{DD} = 2.5V) All outputs except CPU_CLK[0-2]	V_{OL}	–	0.4	V
	I_{OL} = Driver Dependent[5] (BV_{DD} = 2.5V) CPU_CLK[0-2] Only	V_{OL}	–	0.3	V
Capacitance[6]	V_{IN} = 0V, f = 1 MHz	C_{IN}	–	7.0	

Notes:
1. These specifications are for the default driver strengths indicated in Table 7-2 on page 21.
2. See Figure 7-15 on page 34 for pins with internal pull-up resistors.
3. The minimum Input high voltage is not compliant with the *PCI Local Bus Specification* (Rev 2.1) which specifies 0.5*OV_{DD} for minimum input high voltage.
4. Leakage current is measured on input pins and on output pins in the high impedance state. The leakage current is measured for nominal OV_{DD}/LV_{DD} and V_{DD} or both Ov_{DD}/LV_{DD} and V_{DD} must vary in the same direction.
5. See Table 7-2 on page 21 for the typical drive capability of a specific signal pin based upon the type of output driver associated with that pin as listed in Table 2-1 on page 5.
6. Capacitance is periodically sampled rather than 100% tested.

7.1.2 Output Driver Characteristics

Table 7-2 provides information on the characteristics of the output drivers referenced in Table 2-1 on page 5. The values are from the PC107A IBIS model (v1.1) and are not tested, for additional detailed information see the complete IBIS model listing at http://www.freescale.com/semiconductor.

Table 7-2. Drive Capability of PC107A Output Pins

Driver Type	Programmable Output Impedance (Ohms)	Supply Voltage	I_{OH}	I_{OL}	Unit	Notes
DRV_CPU	20	BV_{DD} = 3.3V	36.6	18.1	mA	(2)(5)
		BV_{DD} = 2.5V	21.4	15.6	mA	(3)(6)(7)
	40 (default)	BV_{DD} = 3.3V	18.6	9.2	mA	(2)(5)
		BV_{DD} = 2.5V	10.8	7.9	mA	(3)(6)(7)
DRV_PCI	25	OV_{DD} = 3.3V	12.0	12.4	mA	(1)(4)
	50 (default)	OV_{DD} = 3.3V	6.1	6.3	mA	(1)(4)
DRV_MEM_ADDR DRV_PCI_CLK	8 (default)	GV_{DD} = 3.3V	89.0	42.3	mA	(2)(5)
	13.3	GV_{DD} = 3.3V	55.8	26.4	mA	(2)(5)
	20	GV_{DD} = 3.3V	36.6	18.1	mA	(2)(5)
	40	GV_{DD} = 3.3V	18.6	9.2	mA	(2)(5)
DRV_MEM_DATA	20 (default)	GV_{DD} = 3.3V	36.6	18.1	mA	(2)(5)
	40	GV_{DD} = 3.3V	18.6	9.2	mA	(2)(5)

Notes:
1. For DRV_PCI, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.33V label by interpolating between the 0.3V and 0.4V table entries' current values which corresponds to the PCI V_{OH} = 2.97 = 0.9*OV_{DD} (OV_{DD} = 3.3V) where Table Entry Voltage = OV_{DD} - PCI V_{OH}.
2. For all others with GV_{DD} or BV_{DD} = 3.3V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.9V table entry which corresponds to the V_{OH} = 2.4V where Table Entry Voltage = G/BV_{DD} - V_{OH}.
3. For all others with BV_{DD} = 2.5V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.65V table entry by interpolating between the 0.6V and 0.7V table entries' current values which corresponds to the V_{OH} = 1.85V where Table Entry Voltage = BV_{DD} - V_{OH}.
4. For DRV_PCI, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at 0.33V = PCI V_{OL} = 0.1*OV_{DD} (OV_{DD} = 3.3V) by interpolating between the 0.3V and 0.4V table entries.
5. For all others with GV_{DD} or BV_{DD} = 3.3V, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at the 0.4V table entry.
6. For all others with BV_{DD} = 2.5V, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at the 0.4V table entry.
7. For BV_{DD} = 2.5V, the I_{OH} and I_{OL} values are estimated from the io_mem_data_XX_2.5 and io_mem_addr_XX_2.5 sections of the IBIS model where XX = driver output impedance (20 or 40Ω).

7.2 Dynamic Electrical Characteristics

7.2.1 Clock AC Specifications

Table 7-3 provides the clock AC timing specifications as defined in Section.

At recommended operating conditions (see Table 5-2 on page 12) with GV_{DD} = 3.3V ± 5% and LV_{DD} = 3.3 ±0.3V

Table 7-3. Clock AC Timing Specifications

Num	Characteristics and Conditions (1)	Min	Max	Unit	Notes
1a	Frequency of Operation (PCI_SYNC_IN)	12.5	66	MHz	(8)
1b	PCI_SYNC_IN Cycle Time	80	15	ns	(8)
2, 3	PCI_SYNC_IN Rise and Fall Times	–	2.0	ns	(2)
4	PCI_SYNC_IN Duty Cycle Measured at 1.4V	40	60	%	
5a	PCI_SYNC_IN Pulse Width High Measured at 1.4V	6	9	ns	(3)
5b	PCI_SYNC_IN Pulse Width Low Measured at 1.4V	6	9	ns	(3)
7	PCI_SYNC_IN Jitter	–	< 150	ps	
9a	PCI_CLK[0–4] Skew (Pin to Pin)	–	500	ps	
9b	SDRAM_CLK[0–3] Skew (Pin to Pin)	–	350	ps	
9c	CPU_CLK[0–2] Skew (Pin to Pin)	–	350	ps	
9d	SDRAM_CLK[0–3]/CPU_CLK[0–2] Jitter	–	150	ps	
10	Internal PLL Relock Time	–	100	µs	(3)(4)(6)
15	DLL lock range with DLL_STANDARD = 1 (default)	See Figure 7-3 on page 23		ns	(7)
16	DLL lock range with DLL_STANDARD = 0	See Figure 7-4 on page 24		ns	(7)
17	Frequency of Operation (OSC_IN)	12.5	66	MHz	(8)
18	OSC_IN Cycle Time	80	15	ns	(8)
19	OSC_IN Rise and Fall Times	–	5	ns	(5)
20	OSC_IN Duty Cycle Measured at 1.4V	40	60	%	
21	OSC_IN Frequency Stability	–	100	ppm	

Notes:
1. These specifications are for the default driver strengths indicated in Table 7-2 on page 21.
2. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4V to 2.4V.
3. Specification value at maximum frequency of operation.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Rise and fall times for the OSC_IN input is guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.
6. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
7. DLL_STANDARD is bit 7 of the PMC2 register <72>. N is a non-zero integer (1 or 2). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. t_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. See Figure 7-4 on page 24 for DLL locking ranges.
8. See Table 8-1 on page 37 for PCI_SYNC_IN input frequency range for specific PLL_CFG[0–3] settings.

Figure 7-1 shows the PCI_SYNC_IN Input Clock Timing Diagram, Figure 7-2 illustrates how Table 7-3 clock specifications relate to the PC107A Clocking diagram, and Section 7.2.2 "Operating Frequency" on page 24 shows the DLL Locking Range Loop Delay vs. Frequency of Operation.

Figure 7-1. PCI_SYNC-IN Input Clock Timing Diagram

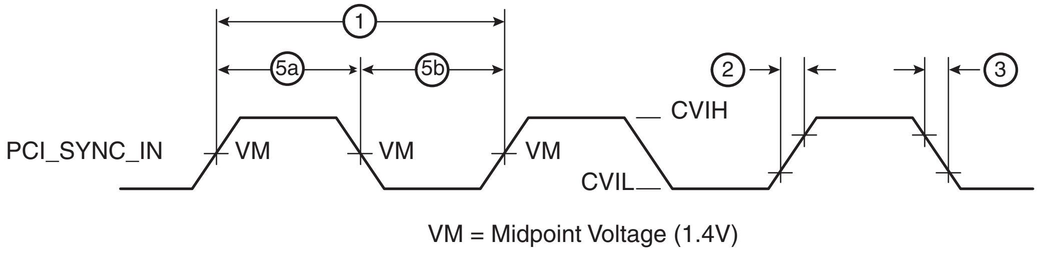
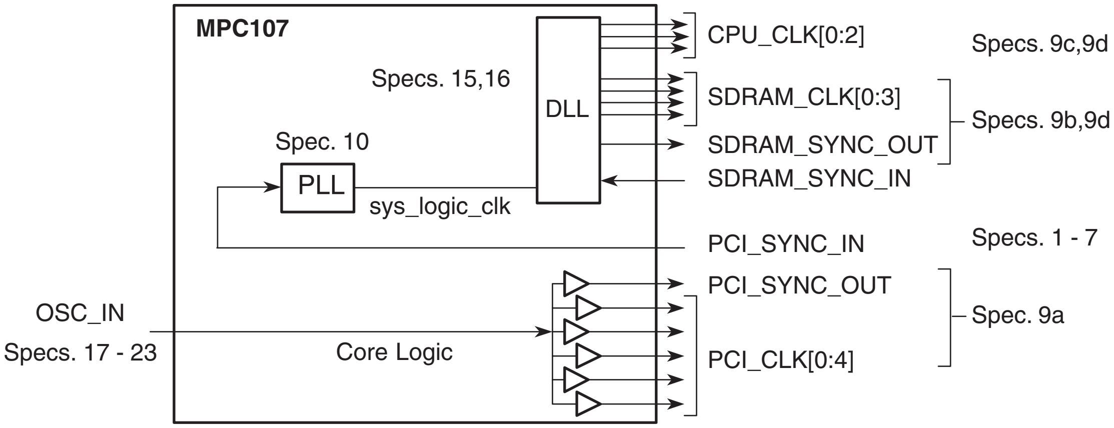


Figure 7-2. Clock Subsystem Block Diagram



Note: Specification numbers are from Table 7-3.

Figure 7-3. DLL Locking Range Loop Delay (DLL_Standard = 0)

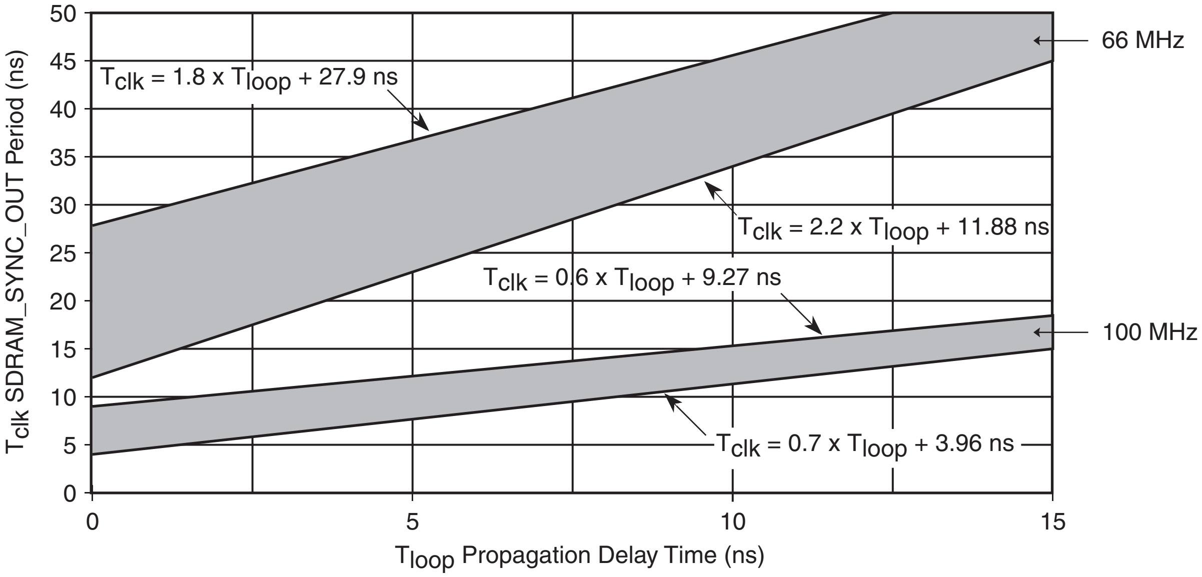
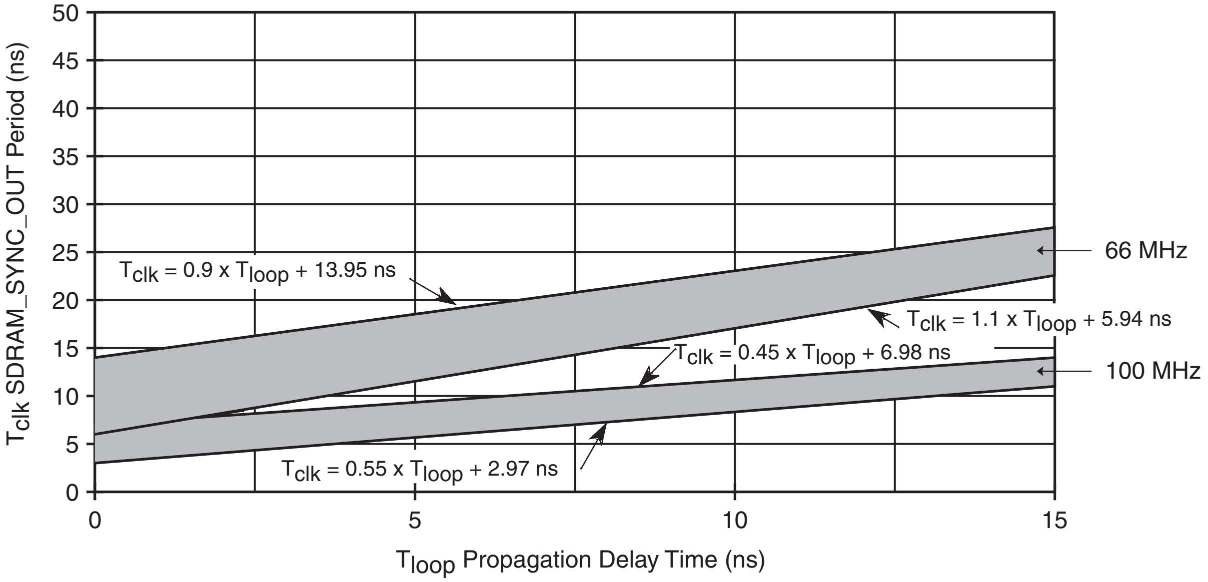


Figure 7-4. DLL Locking Range Loop Delay (DLL_Standard = 1)



7.2.2 Operating Frequency

This section provides the AC electrical characteristics for the PC107A. After fabrication, functional parts are sorted by maximum core frequency as shown in Figure 7-4 and “Clock AC Specifications” on page 22 and tested for conformance to the AC specifications for that frequency. The core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0–3] signals. Parts are sold by maximum processor core frequency; see “Ordering Information” on page 44.

Table 7-4 provides the operating frequency information for the PC107A.

At recommended operating conditions (see Table 5-2 on page 12) with $LV_{DD} = 3.3 \pm 0.3V$.

Table 7-4. Operating Frequency

Characteristic[1]	**66 MHz**		**100 MHz**		**Unit**
	Min	**Max**	**Min**	**Max**	
Core (memory bus/processor bus) frequency	25	66	25	100	MHz
PCI input frequency (PCI_SYNC_IN)	12.5 – 66				MHz

Note: 1. Caution: The PCI_SYNC_IN frequency and PLL_CFG[0–3] settings must be chosen such that the resulting peripheral logic/memory bus frequency, CPU (core) frequency, and PLL (VCO) frequencies do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0–3] signal description in “System Design Information” on page 41 for valid PLL_CFG[0–3] settings and PCI_SYNC_IN frequencies.

7.2.3 Input AC Timing Specifications

Table 7-5 provides the input AC timing specifications. See Figure 7-5 on page 26 and Figure 7-6 on page 26.

At recommended operating conditions (see Table 5-2 on page 12) with GV_{DD} = 3.3V ±5% and LV_{DD} = 3.3 ±0.3V

Table 7-5. Input AC Timing Specifications

Num	Characteristics	Min	Max	Unit	Notes
10a	PCI Input Signals Valid to PCI_SYNC_IN (Input Setup)	3.0	–	ns	(2)(3)
10b	Memory Interface Signals Valid to SDRAM_SYNC_IN (Input Setup)	2.0	–	ns	(1)(3)
10c	Epic, Misc. Debug Input Signals Valid to SDRAM_SYNC_IN (Input Setup)	2.0	–	ns	(1)(3)
10d	Two-wire interface Input Signals Valid to SDRAM_SYNC_IN (Input Setup)	2.0	–	ns	(1)(3)
10e	Mode select Inputs Valid to $\overline{\text{HRESET}}$ (Input Setup)	$9*t_{CLK}$	–	ns	(1)(3)(5)
10f	60x Processor Interface Signals Valid to SDRAM_SYNC_IN (Input Setup)	2.0	–	ns	(1)(3)
11a1	PCI_SYNC_IN (SDRAM_SYNC_IN) to Inputs Invalid (Input Hold)	1.0	–	ns	(2)(3)
11a2	Memory Interface Signals SDRAM_SYNC_IN to Inputs Invalid (Input Hold)	0.5	–	ns	(1)(3)
11a3	60x Processor Interface Signals SDRAM_SYNC_IN to Inputs Invalid (Input Hold)	0	–	ns	(1)(3)
11b	$\overline{\text{HRESET}}$ to Mode select Inputs Invalid (Input Hold)	0	–	ns	(1)(3)(5)

Notes:
1. All memory, processor and related interface input signal specifications are measured from the TTL level (0.8 or 2.0V) of the signal in question to the V_M = 1.4V of the rising edge of the memory bus clock, SDRAM_SYNC_IN. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 7-5.
2. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4*OV_{DD}$ of the signal in question for 3.3 V PCI signaling levels. See Figure 7-6.
3. Input timings are measured at the pin.
4. t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.
5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0V) of the signal in question to the V_M = 1.4V of the rising edge of the $\overline{\text{HRESET}}$ signal. See Figure 7-7 on page 26.

Figure 7-5. Input – Output Timing Diagram Referenced to SDRAM_SYNC_IN

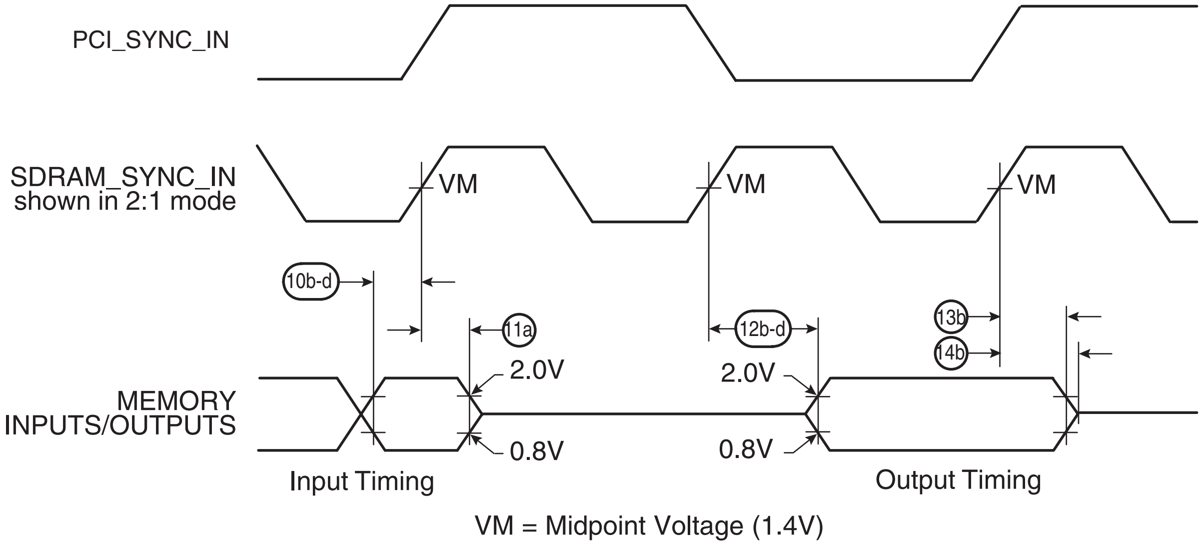


Figure 7-6. Input – Output Timing Diagram Referenced to PCI_SYNC_IN

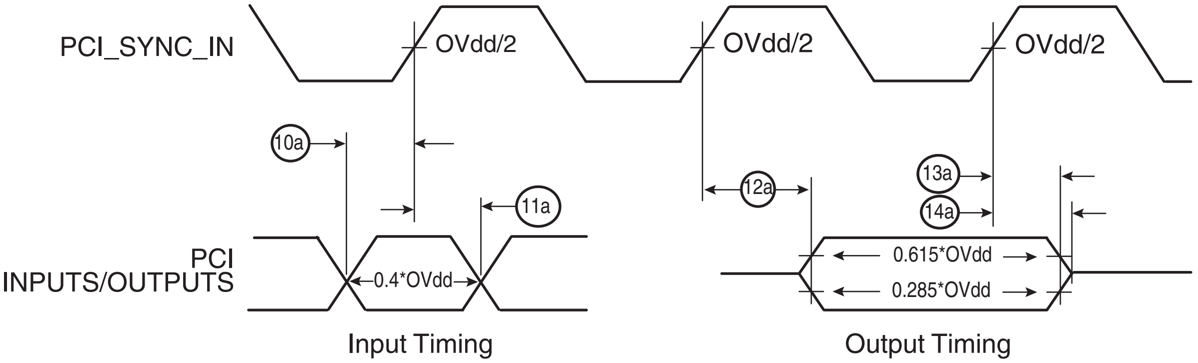
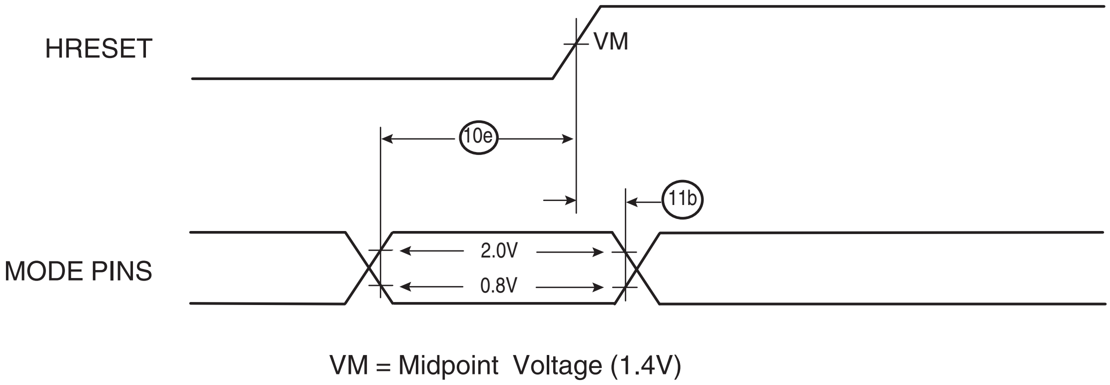


Figure 7-7. Input Timing Diagram for Mode Select Signals



7.2.4 Output AC Timing Specification

Table 7-6 provides the processor bus AC timing specifications for the PC107A. See Figure 7-5 on page 26 and Figure 7-6 on page 26.

At recommended operating conditions (see Table 5-2 on page 12) with LV_{DD} = 3.3 ±0.3V

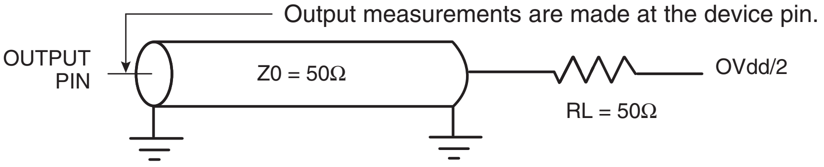
Table 7-6. Output AC Timing Specifications

Num	Characteristics(3)(6)	Min	Max	Unit	Notes
12a	PCI_SYNC_IN to Output Valid, 66 MHz PCI, with SDMA4 pulled-down to logic 0 state. See Figure 7-9.	–	6.0	ns	(2)(4)
	PCI_SYNC_IN to Output Valid, 33 MHz PCI, with SDMA4 in the default logic 1 state. See Figure 7-9.	–	11.0	ns	(2)(4)
12b	Memory Interface Signals, SDRAM_SYNC_IN to Output Valid	–	5.5	ns	(1)
12b1	Memory Interface Signal: CKE (100 MHz Device), SDRAM_SYNC_IN to Output Valid	–	5.5	ns	(1)
12b2	Memory Interface Signal: CKE (66 MHz Device), SDRAM_SYNC_IN to Output Valid	–	6.0	ns	(1)
12c	Epic, Misc. Debug Signals, SDRAM_SYNC_IN to Output Valid	–	9.0	ns	(1)
12d	Two-wire interface, SDRAM_SYNC_IN to Output Valid	–	5.0	ns	(1)
12e	60x Processor Interface Signals, SDRAM_SYNC_IN to Output Valid	–	5.5	ns	(1)
13a	Output Hold, 66 MHz PCI, with SDMA4 and SDMA3 pulled-down to logic 0 states. See Table 7-7.	1.0	–	ns	(2)(4)(5)
	Output Hold, 33 MHz PCI, with SDMA4 in the default logic 1 state and SDMA3 pulled-down to logic 0 state. See Table 7-7.	2.0	–	ns	(2)(4)(5)
13b	Output Hold (For All Others)	1		ns	(1)
14a	PCI_SYNC_IN to Output High Impedance (T_{off} for PCI)	–	14.0	ns	(2)(4)
14b	SDRAM_SYNC_IN to Output High Impedance (For All Others)	–	4.0	ns	(1)

Notes:

1. All memory and related interface output signal specifications are specified from the V_M = 1.4V of the rising edge of the memory bus clock, SDRAM_SYNC_IN to the TTL level (0.8 or 2.0V) of the signal in question. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 7-5 on page 26.
2. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.285{*}OV_{DD}$ or $0.615{*}OV_{DD}$ of the signal in question for 3.3V PCI signaling levels. See Figure 7-6 on page 26.
3. All output timings assume a purely resistive 50Ω load (See Figure 7-8 on page 27). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
4. PCI Bussed signals are composed of the following signals: $\overline{\text{LOCK}}$, $\overline{\text{IRDY}}$, $\overline{\text{C/BE}}$[0–3], PAR, $\overline{\text{TRDY}}$, $\overline{\text{FRAME}}$, $\overline{\text{STOP}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, AD[0–31], $\overline{\text{REQ}}$[4–0], $\overline{\text{GNT}}$[4–0], $\overline{\text{IDSEL}}$, $\overline{\text{INTA}}$.
5. PCI hold times can be varied, see "PCI Signal Output Hold Timing" on page 28 for information on programmable PCI output hold times. The values shown for item 13a are for PCI compliance.
6. These specifications are for the default driver strengths indicated in Table 7-2 on page 21.

Figure 7-8. AC Test Load for the PC107A



7.2.5 PCI Signal Output Hold Timing

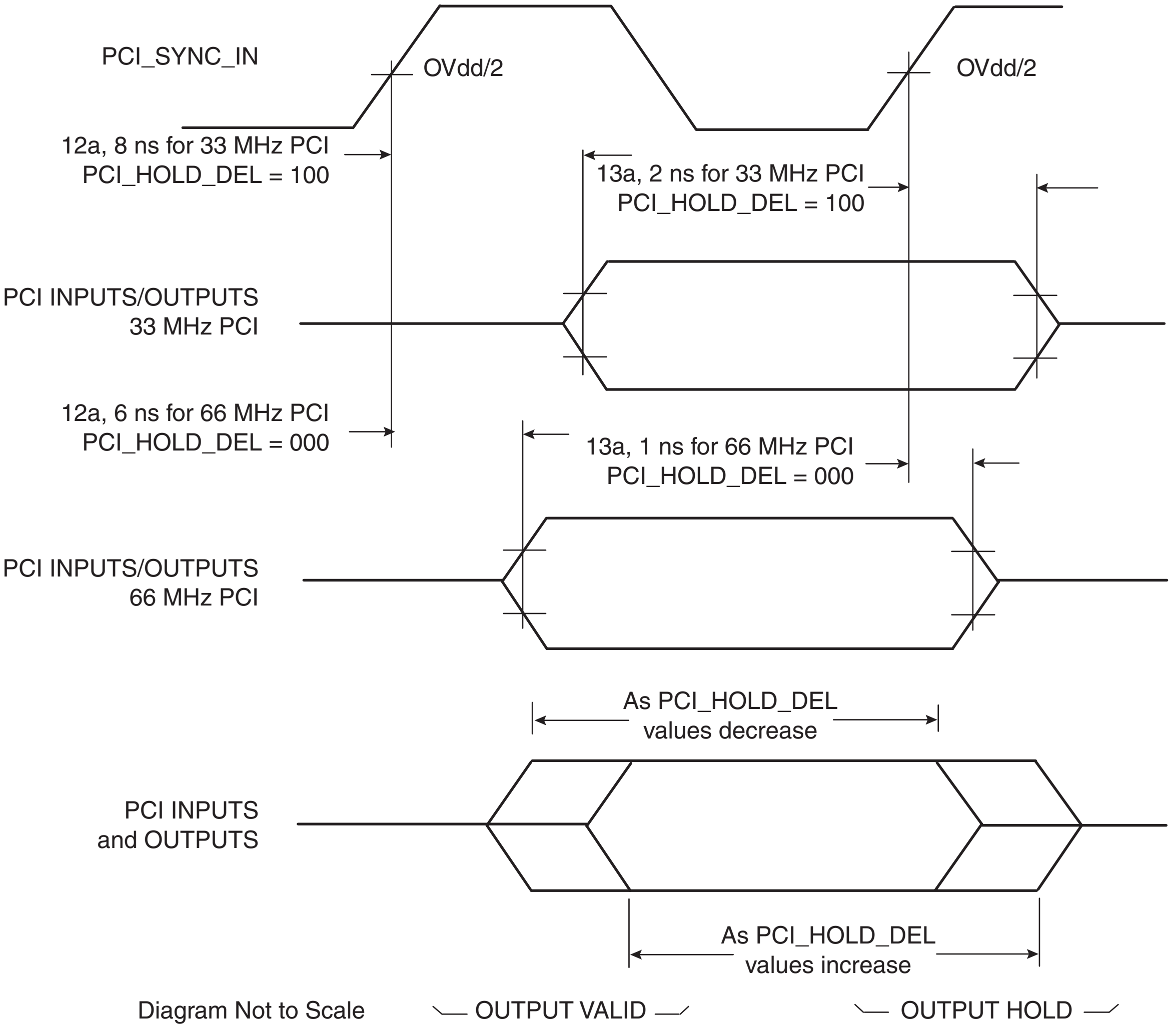
In order to meet minimum output hold specifications relative to PCI_SYNC_IN for both 33 MHz and 66 MHz PCI systems, the PC107A has a programmable output hold delay for PCI signals. The initial value of the output hold delay is determined by the values on the SDMA4 and SDMA3 reset configuration signals. Further output hold delay values are available by programming the PCI_HOLD_DEL value of the PMCR2 configuration register.

Table 7-7 describes the bit values for the PCI_HOLD_DEL values in PMCR2.

Table 7-7. Power Management Configuration Register 2-0x72

Bit	Name	Reset value	Description
6 – 4	PCI_HOLD_DEL	xx0	PCI output hold delay values relative to PCI_SYNC_IN. The initial values of bits 6 and 5 are determined by the reset configuration pins SDMA4 and SDMA3, respectively. As these two pins have internal pull-up resistors, the default value after reset is 0b110. While the minimum hold times are guaranteed at shown values, changes in the actual hold time can be made by incrementing or decrementing the value in these bit fields of this register via software or hardware configuration. The increment is in approximately 400 picosecond steps. Lowering the value in the three bit field decreases the amount of output hold available. 000 66 MHz PCI. Pull-down SDMA4 configuration pin with a 2 kΩ or less value resistor. This setting guarantees the minimum output hold, item 13a, and the maximum output valid, item 12a, times as specified in Figure 7-6 are met for a 66 MHz PCI system. See Figure 7-9 on page 29. 001 010 011 100 33 MHz PCI. This setting guarantees the minimum output hold, item 13a, and the maximum output valid, item 12a, times as specified in Figure 7-6 are met for a 33 MHz PCI system. See Figure 7-9 on page 29. 101 110 (Default if reset configuration pins left unconnected) 111

Figure 7-9. PCI_HOLD_DEL Effect on Output Valid and Hold Time



7.2.6 Two-wire Interface AC Timing Specifications

Table 7-8 provides the two-wire interface input AC timing specifications for the PC107A.

At recommended operating conditions (see Table 5-2 on page 12) with LV_{DD} = 3.3 ±0.3V

Table 7-8. Two-wire Interface Input AC Timing Specifications

Num	Characteristics	Min	Max	Unit	Notes
1	Start condition hold time	4.0	–	CLKs	(1)(2)
2	Clock low period (The time before the PC107A will drive SCL low as a transmitting slave after detecting SCL low as driven by an external master)	8.0 + (16 × $2^{FDR[4:2]}$) × (5 - 4({FDR[5],FDR[1]} == b'10) - 3({FDR[5],FDR[1]} == b'11) - 2({FDR[5],FDR[1]} == b'00) - 1({FDR[5],FDR[1]} == b'01))	–	CLKs	(1)(2)(4)(5)
3	SCL/SDA rise time (from 0.5V to 2.4V)	–	1	ms	
4	Data hold time	0	–	ns	(2)
5	SCL/SDA fall time (from 2.4V to 0.5V)	–	1	mS	
6	Clock high period (Time needed to either receive a data bit or generate a START or STOP)	5.0	–	CLKs	(1)(2)(5)
7	Data setup time	3.0	–	ns	(3)
8	Start condition setup time (for repeated start condition only)	4.0	–	CLKs	(1)(2)
9	Stop condition setup time	4.0	–	CLKs	(1)(2)

Notes:
1. Units for these specifications are in SDRAM_CLK/CPU_CLK units.
2. The actual values depend on the setting of the Digital Filter Frequency Sampling Rate (DFFSR) bits in the Frequency Divider Register two-wire interface FDR. Therefore, the noted timings in the above table are all relative to qualified signals. The qualified SCL and SDA are delayed signals from what is seen in real time on the two-wire interface bus. The qualified SCL, SDA signals are delayed by the SDRAM_CLK/CPU_CLK clock times DFFSR times 2 plus 1 SDRAM_CLK/CPU_CLK clock. The resulting delay value is added to the value in the table (where this note is referenced). See Figure 7-11 on page 33.
3. Timing is relative to the Sampling Clock (not SCL).
4. FDR[x] refers to the Frequency Divider Register I2CFDR bit x.
5. Input clock low and high periods in combination with the FDR value in the Frequency Divider Register (I2CFDR) determine the maximum two-wire interface input frequency. See Figure 7-11 on page 33.

Table 7-9 provides the two-wire interface Frequency Divider Register (I2CFDR) information for the PC107A.

At recommended operating conditions (see Table 5-2 on page 12) with LV_{DD} = 3.3V ± 5%

Table 7-9. PC8240 Maximum Two-wire Interface Input Frequency

FDR Hex(2)	**Divider (Dec)**(2)	**Max Two-wire Interface Input Frequency**(1)			
		SDRAM_CLK/ CPU_CLK at 25 MHz	**SDRAM_CLK/ CPU_CLK at 33 MHz**	**SDRAM_CLK/ CPU_CLK at 50 MHz**	**SDRAM_CLK/ CPU_CLK at 100 MHz**
20, 21	160, 192	862	1.13 MHz	1.72 MHz	3.44 MHz
22, 23, 24, 25	224, 256, 320, 384	555	733	1.11 MHz	2.22 MHz
0, 1	288, 320	409	540	819	1.63 MHz
2, 3, 26, 27, 28, 29	384, 448, 480, 512, 640, 768	324	428	649	1.29 MHz
4, 5	576, 640	229	302	458	917
6, 7, 2A, 2B, 2C, 2D	768, 896, 960, 1024, 1280, 1536	177	234	354	709
8, 9	1152, 1280	121	160	243	487
A, B, 2E, 2F, 30, 31	1536, 1792, 1920, 2048, 2560, 3072	92	122	185	371
C, D	2304, 2560	62	83	125	251
E, F, 32, 33, 34, 35	3072, 3584, 3840, 4096, 5120, 6144	47	62	95	190
10, 11	4608, 5120	32	42	64	128
12, 13, 36, 37, 38, 39	6144, 7168, 7680, 8192, 10240, 12288	24	31	48	96
14, 15	9216, 10240	16	21	32	64
16, 17, 3A, 3B, 3C, 3D	12288, 14336, 15360, 16384, 20480, 24576	12	16	24	48
18, 19	18432, 20480	8	10	16	32
1A, 1B, 3E, 3F	24576, 28672, 30720, 32768	6	8	12	24
1C, 1D	36864, 40960	4	5	8	16
1E, 1F	49152, 61440	3	4	6	12

Notes:
1. Values are in kHz unless otherwise specified.
2. FDR Hex and Divider (Dec) values are listed in corresponding order.
3. Multiple Divider (Dec) values will generate the same input frequency but each Divider (Dec) value will generate a unique output frequency as shown in Table 7-10 on page 32.

Table 7-10 provides the two-wire interface output AC timing specifications for the PC107A.

At recommended operating conditions (see Table 5-2 on page 12) with GV_{DD} = 3.3V ± 5% and LV_{DD} = 3.3 ±0.3V

Table 7-10. Two-wire Interface Output AC Timing Specifications

Num	Characteristics	Min	Max	Unit	Notes
1	Start condition hold time	(FDR[5] == 0) × (D_{FDR}/16) / 2N + (FDR[5] == 1) × (D_{FDR}/16) / 2M	–	CLKs	(1)(2)(5)
2	Clock low period	D_{FDR} / 2	–	CLKs	(1)(2)(5)
3	SCL/SDA rise time (from 0.5V to 2.4V)	–	–	mS	(3)
4	Data hold time	8.0 + (16 × $2^{FDR[4:2]}$) × (5 - 4({FDR[5],FDR[1]} == b'10) - 3({FDR[5],FDR[1]} == b'11) - 2({FDR[5],FDR[1]} == b'00) - 1({FDR[5],FDR[1]} == b'01))	–	CLKs	(1)(2)(5)
5	SCL/SDA fall time (from 2.4V to 0.5V)	–	< 5	ns	(4)
6	Clock high time	D_{FDR} / 2	–	CLKs	(1)(2)(5)
7	Data setup time (PC107A as a master only)	(D_{FDR} / 2) - (Output data hold time)	–	CLKs	(1)(5)
8	Start condition setup time (for repeated start condition only)	D_{FDR} + (Output start condition hold time)	–	CLKs	(1)(2)(5)
9	Stop condition setup time	4.0	–	CLKs	(1)(2)

Notes:
1. Units for these specifications are in SDRAM_CLK/CPU_CLK units.
2. The actual values depend on the setting of the Digital Filter Frequency Sampling Rate (DFFSR) bits in the Frequency Divider Register I2CFDR. Therefore, the noted timings in the above table are all relative to qualified signals. The qualified SCL and SDA are delayed signals from what is seen in real time on the two-wire interface bus. The qualified SCL, SDA signals are delayed by the SDRAM_CLK/CPU_CLK clock times DFFSR times 2 plus 1 SDRAM_CLK/CPU_CLK clock. The resulting delay value is added to the value in the table (where this note is referenced). See Figure 7-11 on page 33.
3. Since SCL and SDA are open-drain type outputs, which the PC107A can only drive low, the time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values.
4. Specified at a nominal 50 pF load.
5. D_{FDR} is the decimal divider number indexed by FDR[5:0] value. Refer to the two-wire Interface chapter's Serial Bit Clock Frequency Divider Selections table. FDR[x] refers to the Frequency Divider Register I2CFDR bit x. N is equal to a variable number that would make the result of the divide (Data Hold Time value) equal to a number less than 16. M is equal to a variable number that would make the result of the divide (Data Hold Time value) equal to a number less than 9.

Figure 7-10. Two-wire Interface Timing Diagram II

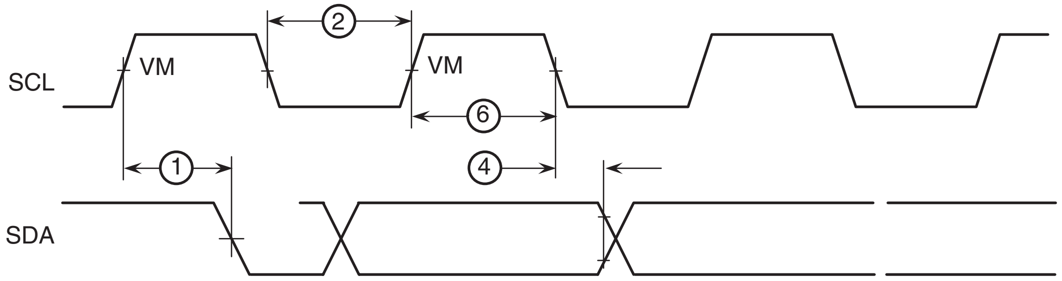


Figure 7-11. Two-wire Interface Timing Diagram II

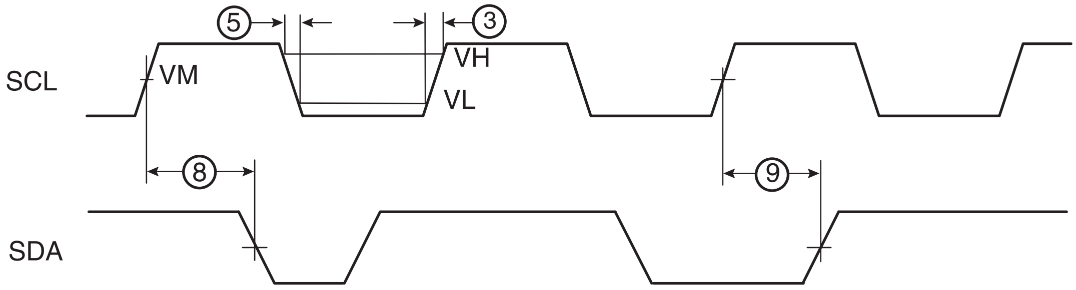
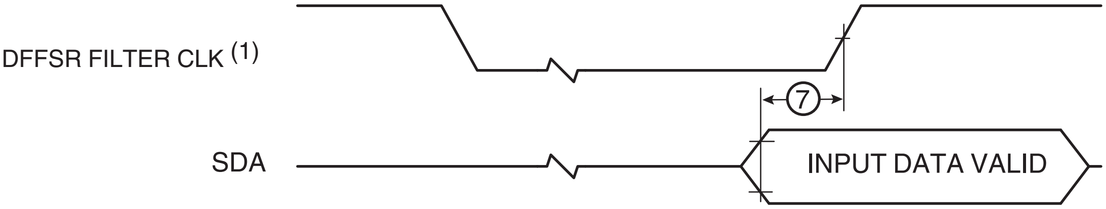
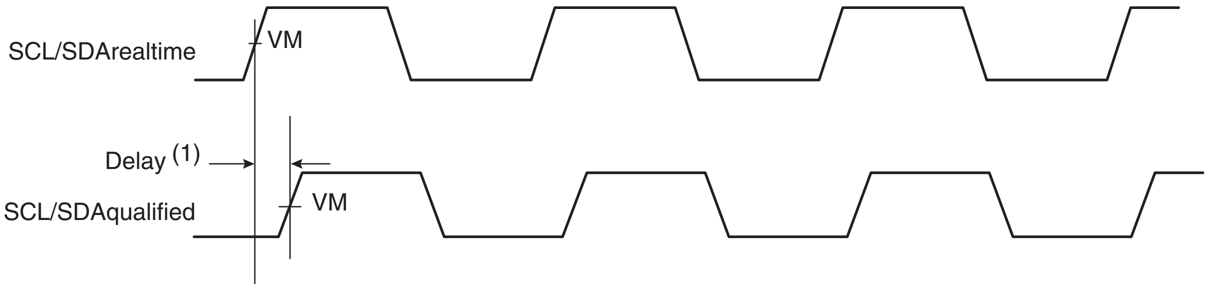


Figure 7-12. Two-wire Interface Timing Diagram III



Note: DFFSR Filter Clock is the SDRAM_CLK clock times DFFSR value.

Figure 7-13. Two-wire Interface Timing Diagram IV (Qualified Signal)



Note: The delay is the Local Memory clock times DFFSR times 2 plus 1 Local Memory clock.

7.2.7 EPIC Serial Interrupt Mode AC Timing Specifications

Table 7-11 provides the EPIC serial interrupt mode AC timing specifications for the PC107A.

At recommended operating conditions (see Table 5-2 on page 12) with LV_{DD} = 3.3 ±0.3V

Table 7-11. EPIC Serial Interrupt Mode AC Timing Specifications

Num	Characteristics	Min	Max	Unit	Notes
1	S_CLK Frequency	1/14 SDRAM_SYNC_IN	1/2 SDRAM_SYNC_IN	MHz	(1)
2	S_CLK Duty Cycle	40	60	%	
3	S_CLK Output Valid Time	–	6	nS	
4	Output Hold Time	0	–	nS	
5	$\overline{\text{S\_FRAME}}$, S_RST Output Valid Time	–	1 sys_logic_clk period + 6	nS	(2)
6	S_INT Input Setup Time to S_CLK	1 sys_logic_clk period + 2	–	nS	(2)
7	S_INT Inputs Invalid (Hold Time) to S_CLK	–	0	nS	(2)

Notes:
1. See the PC107A User's Manual for a description of the EPIC Interrupt Control Register (EICR) describing S_CLK frequency programming.
2. S_RST, $\overline{\text{S\_FRAME}}$, and S_INT shown in Figure 7-14 and Figure 7-15 depict timing relationships to sys_logic_clk and S_CLK and do not describe functional relationships between S_RST, $\overline{\text{S\_FRAME}}$, and S_INT. See the PC107A User's Manual for a complete description of the functional relationships between these signals.
3. The sys_logic_clk waveform is the clocking signal of the internal peripheral logic from the output of the peripheral logic PLL; sys_logic_clk is the same as SDRAM_SYNC_IN when the SDRAM_SYNC_OUT to SDRAM_SYNC_IN feedback loop is implemented and the DLL is locked. See the PC107A User's Manual for a complete clocking description.

Figure 7-14. EPIC Serial Interrupt Mode Output Timing Diagram

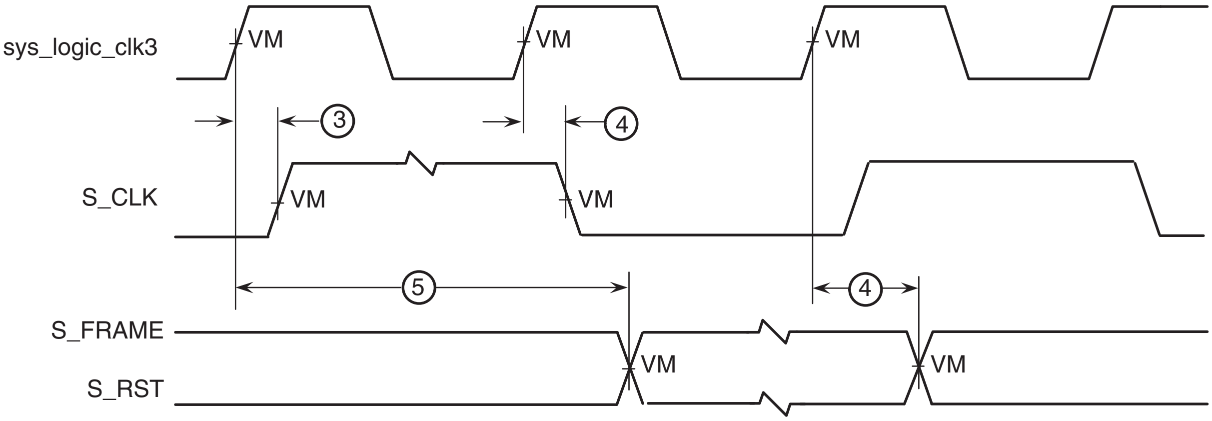
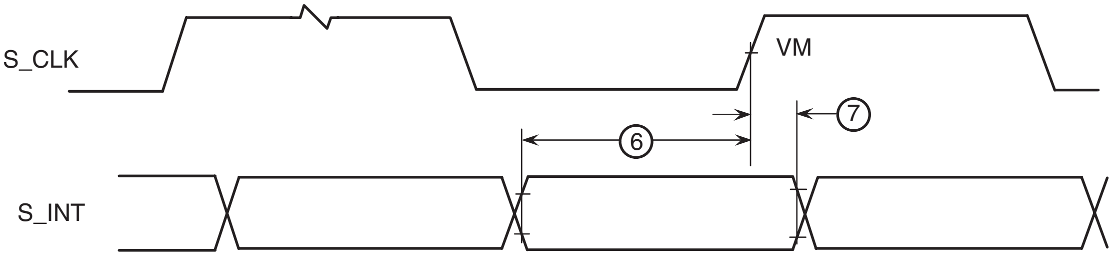


Figure 7-15. EPIC Serial Interrupt Mode Input Timing Diagram



7.2.8 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 7-12 provides the JTAG AC timing specifications for the PC107A while in the JTAG operating mode.

At recommended operating conditions (see Table 5-2 on page 12) with LV_{DD} = 3.3 ±0.3V

Table 7-12. JTAG AC Timing Specifications (Independent of PCI_SYNC_IN)

Num	Characteristics(4)	Min	Max	Unit	Notes
	TCK Frequency of Operation	0	25	MHz	
1	TCK Cycle Time	40	–	ns	
2	TCK Clock Pulse Width Measured at 1.5V	20	–	ns	
3	TCK Rise and Fall Times	0	3	ns	
4	TRST_ Setup Time to TCK Falling Edge	10	–	ns	(1)
5	TRST_ Assert Time	10	–	ns	
6	Boundary Scan Input Data Setup Time	5	–	ns	(2)
7	Boundary Scan Input Data Hold Time	15	–	ns	(2)
8	TCK to Output Data Valid	0	30	ns	(3)
9	TCK to Output High Impedance	0	30	ns	(3)
10	TMS, TDI Data Setup Time	5	–	ns	
11	TMS, TDI Data Hold Time	15	–	ns	
12	TCK to TDO Data Valid	0	15	ns	
13	TCK to TDO High Impedance	0	15	ns	

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test (other than TDI and TMS) signal input timing with respect to TCK.
3. Non-test (other than TDO) signal output timing with respect to TCK.
4. Timings are independent of the system clock (PCI_SYNC_IN).

Figure 7-16. JTAG Clock Input Timing Diagram

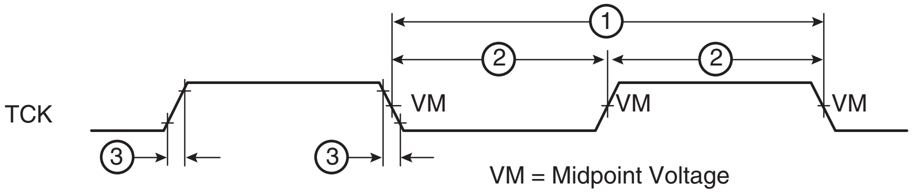


Figure 7-17. JTAG TRST Timing Diagram

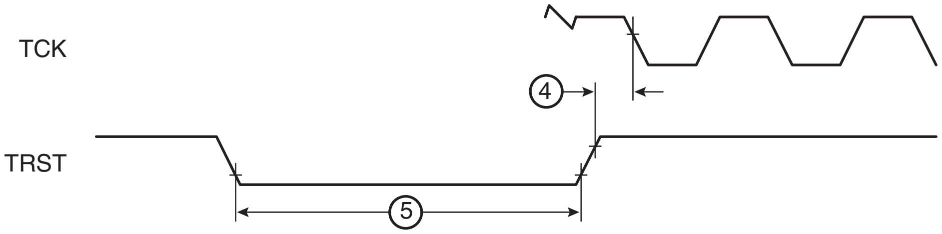


Figure 7-18. JTAG Boundary Scan Timing Diagram

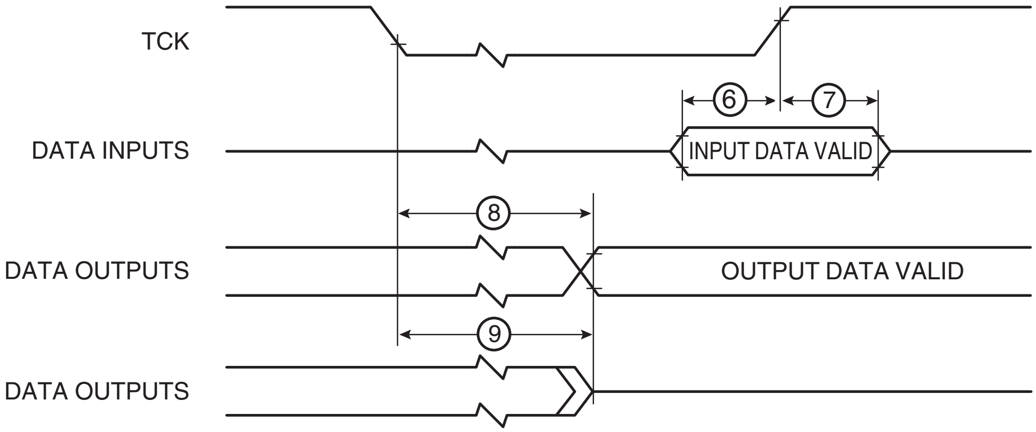
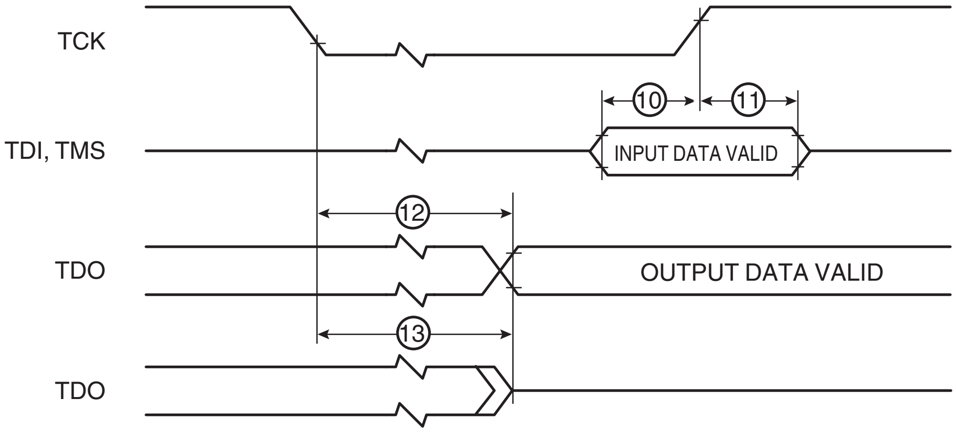


Figure 7-19. Test Access Port Timing Diagram



8. Preparation for Delivery

8.1 Packaging

Microcircuits are prepared for delivery in accordance with internal standards.

8.2 Certificate of Compliance

e2v offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with internal specifications and guaranteeing the parameters not tested at temperature extremes for the entire temperature range.

8.3 Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

- Devices should be handled on benches with conductive and grounded surfaces
- Ground test equipment, tools and operator
- Do not handle devices by the leads
- Store devices in conductive foam or carriers
- Avoid use of plastic, rubber or silk in MOS areas
- Maintain relative humidity above 50% if practical

8.4 Choice of Clock Relationships

The PC107A's internal PLL is configured by the PLL_CFG[0–3] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set the Core/Memory/Processor PLL (VCO) frequency of operation for the PCI-to-Core/Memory/Processor frequency multiplying, if any. All valid PLL configurations for the PC107A are shown in Table 8-1.

Table 8-1. PC107A Microprocessor PLL Configuration

Ref	PLL_CFG [0–3](2)	66 MHz Part		100 MHz Part		PCI: Core Ratio	VCO Multiplier
		PCI_SYNC_IN Range (MHz)	Core/Mem/CPU Range (MHz)	PCI_SYNC_IN Range (MHz)	Core/Mem/CPU Range (MHz)		
1	0001	25(5) – 33	25 – 33	25(5) – 50(4)	25 – 50	1	4
2	0010	13(5) – 16(4)	26 – 34	13(5) – 25(4)	26 – 50	2	4
3	0011	Bypass		Bypass		Bypass	Bypass
5	0101	25(5) – 33	50 – 66	25(5) – 50	50 – 100	2	2
8	1000	17(5) – 22	51 – 66	17(5) – 33	50 – 100	3	2
9	1001	34(5) – 44	51 – 66	33(5) – 66	50 – 100	1.5	2
A	1010	13(4)–16(7)	52–64	13(4)–25(7)	52–100	4	2
C	1100	20(5) – 26	50 – 65	20(5) – 40	50 – 100	2.5	2
D	1101	50(5) – 66	50 – 66	50(5) – 66	50 – 66	1	2
F	1111	Clock off(3)	Not Usable	Clock off (3)	Not Usable	Off	Off

Notes:
1. PLL_CFG[0–3] settings not listed (00000100, 0110, 0111, 1010, 1011, and 1110) are reserved.
2. In PLL Bypass mode, the PCI_SYNC_IN input signal clocks the internal core directly, the PLL is disabled, and the PCI: core mode is set for 1:1 mode operation. The AC timing specifications given in this document do not apply in PLL Bypass mode.
3. In Clock Off mode, no clocking occurs inside the PC107A regardless of the PCI_SYNC_IN input.
4. Limited due to maximum memory VCO = 200 MHz.
5. Limited due to minimum VCO = 100 MHz.
6. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
7. Limited by maximum memory bus speed.

9. Package Mechanical Data

9.1 Package Parameters

The PC107A uses a 33 mm × 33 mm, 503 pin Plastic Ball Grid Array (PBGA) or HiTCE "Ceramic Ball Grid Array (CBGA)" package. The plastic package parameters are as provided in the following list.

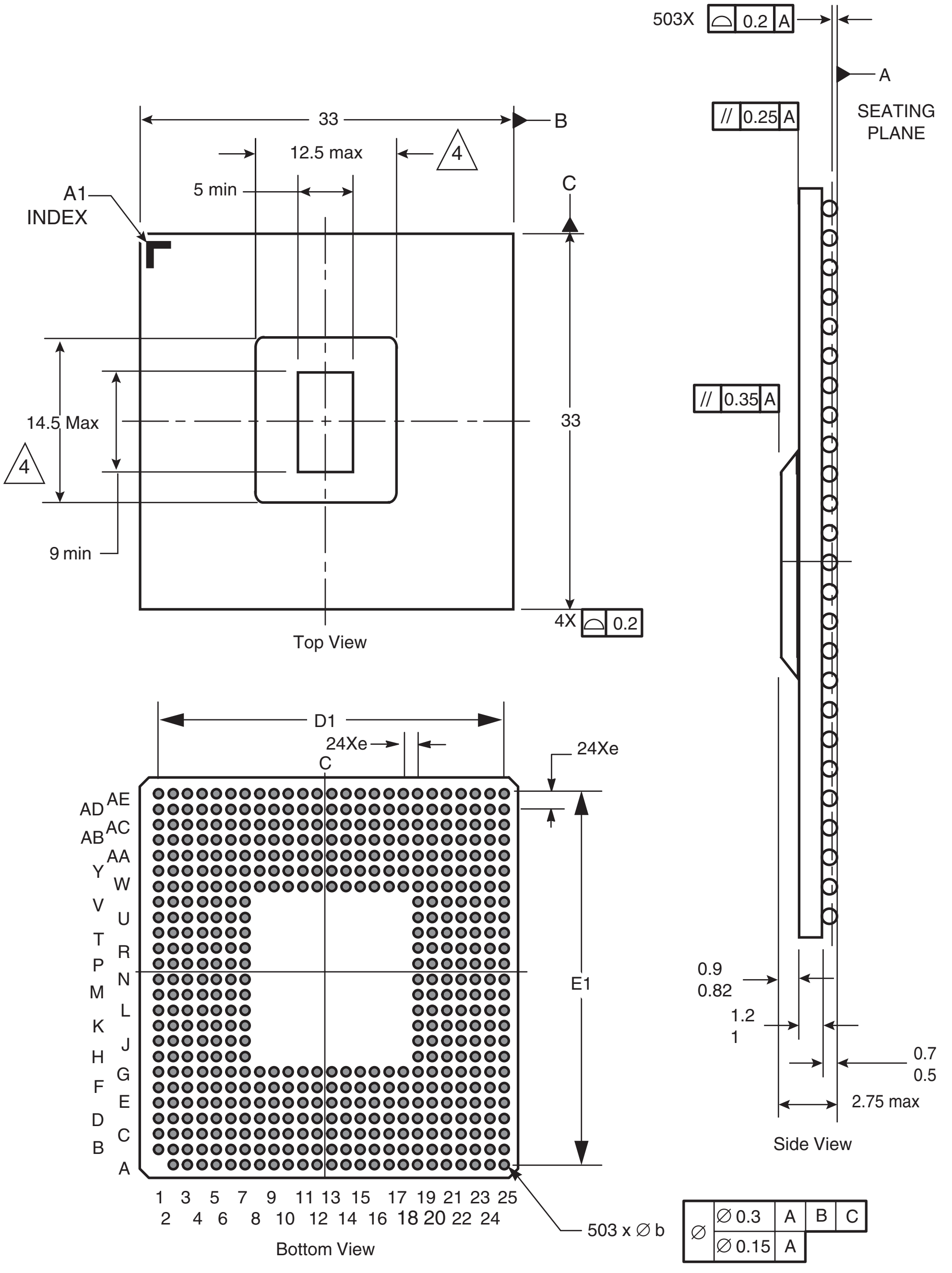
Table 9-1. Package Parameters

Parameter	**HiTCE-CBGA**	**FC-PBGA**
Package Outline	33 mm × 33 mm	33 mm × 33 mm
Interconnects	503	503
Pitch	1.27 mm	1.27 mm
Solder Attach	10 Sn/90 Pb	62 Sn/36 Pb/2 Ag
Solder Balls	10 Sn/90 Pb	62 Sn/36 Pb/2 Ag
Solder Balls Diameter	0.60 mm – 0.90 mm	0.60 mm – 0.90 mm
Maximum Module Height	3.20	2.75 mm
Co-planarity Specification	0.20 mm	0.20 mm
Maximum Force	6.0 lbs. total, uniformly distributed over package (5.4 grams/ball)	6.0 pbs. total, uniformly distributed over package (5.4 grams/ball)

9.2 Mechanical Dimensions

Figure 9-1 shows the top surface, side profile, and pinout of the PC107A, 503 PBGA package.

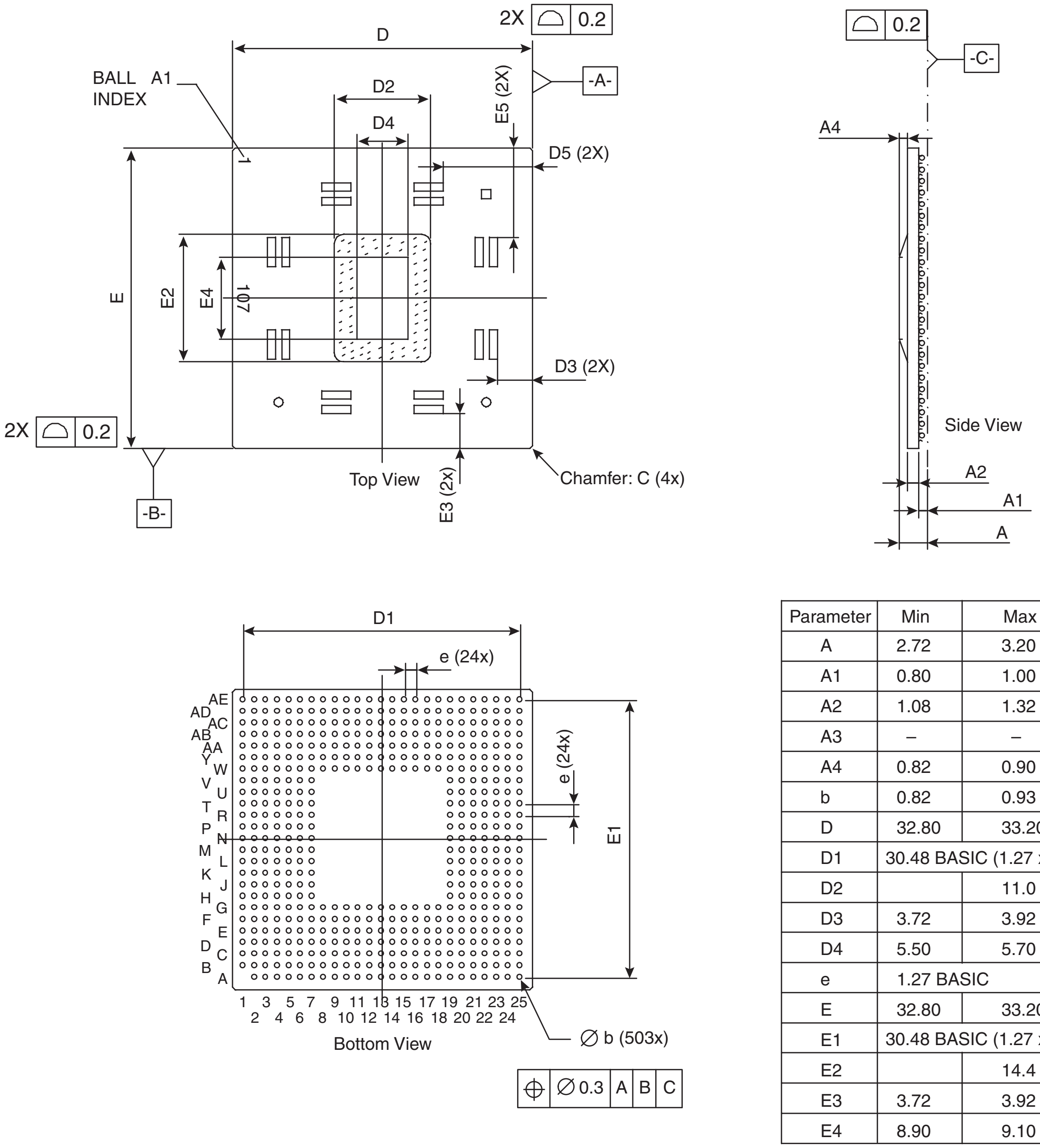
Figure 9-1. PC107A Package Dimensions and Pinout Assignments



	Millimeters	
DIM	Min	Max
A		2.75
A1	0.50	0.70
A2	1.00	1.20
A3		0.80
A4	0.82	0.90
b	0.60	0.90
C	33 BSC	
D1	30.48 BSC	
D2		12.50
D3	3.43	
D4	5.00	
e	1.27 BSC	
E	33 BSC	
E1	30.48 BSC	
E2		14.50
E3	3.43	
E4	9.00	

Notes:
1. Dimensioning and tolerancing per A.
2. Dimensions in millimeters.
3. Dimension b is the maximum solder ball diameter measured parallel to datum A.
4. D2 and E2 define the area occupied on the die and underfill actual size of this area may be smaller than shown. D3 and E3 are the minimum clearance from the package edge to the chip capacitors.
5. Capacitors may not be present on all devices.
6. Caution must be taken not to short expose metal capacitor pads on package top.

Figure 9-2. Mechanical Dimensions and Bottom Surface Nomenclature of the 503-ball HiTCE CBGA Package



Parameter	Min	Max
A	2.72	3.20
A1	0.80	1.00
A2	1.08	1.32
A3	–	–
A4	0.82	0.90
b	0.82	0.93
D	32.80	33.20
D1	30.48 BASIC (1.27 x 24)	
D2		11.0
D3	3.72	3.92
D4	5.50	5.70
e	1.27 BASIC	
E	32.80	33.20
E1	30.48 BASIC (1.27 x 24)	
E2		14.4
E3	3.72	3.92
E4	8.90	9.10

All dimension in mm

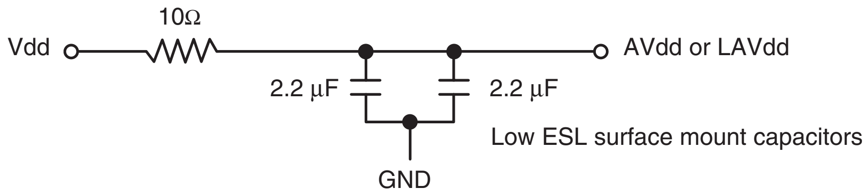
10. System Design Information

10.1 PLL Power Supply Filtering

The AV_{DD} and LAV_{DD} power signals are provided on the PC107A to provide power to the peripheral logic/memory bus PLL and the SDRAM clock delay-locked loop (DLL), respectively. To ensure stability of the internal clocks, the power supplied to the AV_{DD} and LAV_{DD} input signals should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLLs. A separate circuit similar to the one shown in Figure 10-1 using surface mount capacitors with minimum effective series inductance (ESL) is recommended for each of the AV_{DD} and LAV_{DD} power signal pins. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over using multiple values.

The circuits should be placed as close as possible to the respective input signal pins to minimize noise coupled from nearby circuits. Routing directly as possible from the capacitors to the input signal pins with minimal inductance of vias is important but proportionately less critical for the LAV_{DD} pin.

Figure 10-1. PLL Power Supply Filter Circuit

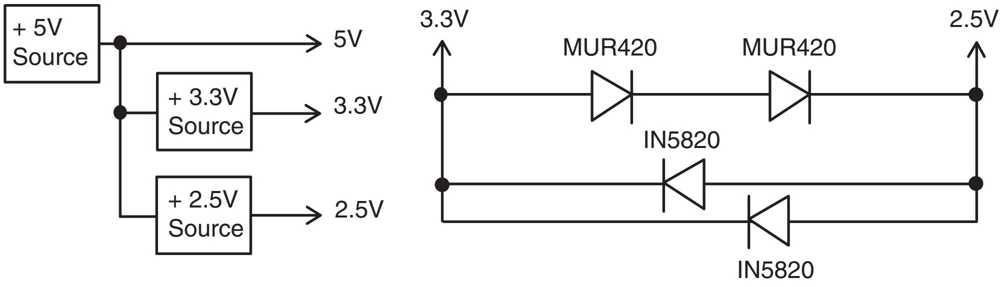


10.2 Power Supply Voltage Sequencing

The notes in Table 5-2 on page 12 contain cautions illustrated in Figure 5-1 on page 13 about the sequencing of the external bus voltages and internal voltages of the PC107A. These cautions are necessary for the long term reliability of the part. If they are violated, the electrostatic discharge (ESD) protection diodes will be forward biased and excessive current can flow through these diodes. Figure 5-1 shows a typical ramping voltage sequence where the DC power sources (voltage regulators and/or power supplies) are connected as shown in Figure 10-2. The voltage regulator delay shown in Figure 5-1 can be zero if the various DC voltage levels are all applied to the target board at the same time. The ramping voltage sequence shows a scenario in which the $V_{DD}/AV_{DD}/LAV_{DD}$ power plane is not loaded as much as the OV_{DD}/GV_{DD} power plane and thus $V_{DD}/AV_{DD}/LAV_{DD}$ ramps at a faster rate than OV_{DD}/GV_{DD}.

If the system power supply design does not control the voltage sequencing, the circuit of Figure 10-2 can be added to meet these requirements. The MUR420 diodes of Figure 10-2 control the maximum potential difference between the 3.3 bus and internal voltages on power-up and the 1N5820 Schottky diodes regulate the maximum potential difference on power-down.

Figure 10-2. Example Voltage Sequencing Circuits



10.3 Decoupling Recommendations

Due to the PC107A's dynamic power management feature, large address and data buses, and high operating frequencies, the PC107A can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PC107A system, and the PC107A itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the PC107A. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603, oriented such that connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, BV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors-100 – 330 µF (AVX TPS tantalum or Sanyo OSCON).

10.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, BV_{DD}, and GND pins of the PC107A.

The PCI_SYNC_OUT signal is intended to be routed halfway out to the PCI devices and then returned to the PCI_SYNC_IN input of the PC107A.

The SDRAM_SYNC_OUT signal is intended to be routed halfway out to the SDRAM devices and then returned to the SDRAM_SYNC_IN input of the PC107A. The trace length may be used to skew or adjust the timing window as needed. See Freescale™ application note "AN1794/D" for more information on this topic.

The $\overline{\text{TRST}}$ signal must be asserted during reset to ensure proper initialization and operation of the PC107A. It is recommended that the $\overline{\text{TRST}}$ signal be connected to the system $\overline{\text{HRESET}}$ signal or pulled down with a 100Ω - 1 kΩ resistor.

10.5 Pull-up/Pull-down Resistor Requirements

The data bus input receivers are normally turned off when no read operation is in progress; therefore, they do not require pull-up resistors on the bus. The processor data bus signals are: DH[0–31], DL[0–31], and PAR[0–7]. The memory data bus signals are: MDH[0–31], MDL[0–31], and PAR/AR[0–7].

If the 32-bit data bus mode is selected, the input receivers of the unused data and parity bits (DL[0–31], DP[4–7], MDL[0–31], and PAR[4–7]) will be disabled, and their outputs will drive logic zeros when they would otherwise normally be driven. For this mode, these pins do not require pull-up resistors, and should be left unconnected by the system to minimize possible output switching.

It is recommended that $\overline{\text{ARTRY}}$, $\overline{\text{TA}}$, and $\overline{\text{TS}}$ have weak pull-up resistors (2 kΩ – 10 kΩ) connected to BV_{DD}.

It is recommended that MTP[1–2] and $\overline{\text{TEST2}}$ have weak pull-up resistor (2 kΩ – 10 kΩ) connected to GV_{DD}.

It is recommended that the following signals be pulled up to OV_{DD} with weak pull-up resistors (2 kΩ – 10 kΩ): SDA, SCL, $\overline{\text{TEST1}}$, and FTP[3–3].

It is recommended that the following PCI control signals be pulled up to LV_{DD} with weak pull-up resistors (2 kΩ – 10 kΩ): $\overline{\text{DEVSEL}}$, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{LOCK}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{STOP}}$, $\overline{\text{TRDY}}$ and $\overline{\text{INTA}}$. The resistor values may need to be adjusted stronger to reduce induced noise on specific board designs.

The following pins have internal pull-up resistors enabled at all times: $\overline{\text{REQ}}$[06–4], TCK, TDI, TMS, and $\overline{\text{TRST}}$, $\overline{\text{BR1}}$, $\overline{\text{HRESET\_CPU}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$, $\overline{\text{SRESET}}$, $\overline{\text{TEST}}$ and $\overline{\text{TRIG\_OUT}}$. See Table 2-1, "PC107A Pinout Listing," on page 5 for more information.

The following pins have internal pull-up resistors enabled only while device is in the reset state: MDL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, CKE, SDBAO, and SDMA[10–1]. See Table 2-1, "PC107A Pinout Listing," on page 5 for more information.

The following pins are reset configuration pins: MDL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, SDBAO, SDMA[10–1], and PLL_CFG[0–3]. These pins are sampled during reset to configure the device.

Any other unused active low input pins should be tied to a logic one level via weak pull-up resistors (2 kΩ – 10 kΩ) to the appropriate power supply listed in Table 5-2 on page 12. Unused active high input pins should be tied to GND via weak pull-down resistors (2 kΩ– 10 kΩ).

11. Definitions

11.1 Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify e2v for any damages resulting from such improper use or sale.

12. Ordering Information

Product Code [1]	Part Identifier	Temperature Range: T_J [1]	Package [1]	Screening Level	Operating Frequency	Bus Divider	Revision Level [1]
PC(X) [2]	107A	M: -55˚C, +125˚C V: -40˚C, +110˚C	ZF: FC-PBGA [2] GH: HiTCE - CBGA	U: Upscreening Test Blank: Standard	100: 100 MHz	L: 2.5 ± 125 mV	C = 1.3 D = 1.4

Notes:
1. For availability of the different versions, contact your local e2v sales office.
2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

13. Document Revision History

Table 13-1 provides a revision history for this hardware specification.

Table 13-1. Document Revision History

Revision Number	Date	Substantive Change(s)
E	04/2007	Name from Atmel to e2v Ordering information update
D	09/2004	Final specification after qualification product Motorola changed to Freescale
C	06/2006	Add HiTCE Package with Thermal characteristics (see Table 6-2 on page 16)
		Ordering Information (See “Ordering Information” on page 44.)

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