Effective October 2015 Supersedes March 2007

HC2LP Low profile, high current power inductors



Product description

- · Compact footprint
- Designed for high density, high current/low voltage applications
- Foil technology that adds higher reliability factor over the traditional magnet wire used for higher frequency circuit designs
- Frequency Range up to 1MHz
- · Ferrite core material

Applications

- Distributed power systems DC-DC converters
- General-purpose low voltage supplies
- Computer systems
- Servers
- Point of Load (POL) converters
- Industrial Equipment
- Networking/Telecom power supplies

Environmental data

- Storage temperature range (component): -40°C to +125°C
- Operating temperature range: -40°C to +125°C (ambient + self-temperature rise).
- Solder reflow temperature: J-STD-020D compliant.





Product specifications

OCL1 (µH) ±20%	l _{rms} ² amps (approx.)	l _{sat} ³ amps (approx.)	DCR⁴ (Ω) maximum @ 20°C	Volt-µsec⁵ (V-µs)
.52	52.9	63.75	.0006	6.87
.63	52.9	50.00	.0006	6.87
1.15	33.0	42.50	.0013	10.31
2.00	24.3	31.90	.0023	13.75
4.55	17.0	21.25	.0046	20.62
6.00	17.0	16.50	.0046	20.62
	.52 .63 1.15 2.00 4.55	.52 52.9 .63 52.9 1.15 33.0 2.00 24.3 4.55 17.0	.52 52.9 63.75 .63 52.9 50.00 1.15 33.0 42.50 2.00 24.3 31.90 4.55 17.0 21.25	.52 52.9 63.75 .0006 .63 52.9 50.00 .0006 1.15 33.0 42.50 .0013 2.00 24.3 31.90 .0023 4.55 17.0 21.25 .0046

4. Values @ 20°C

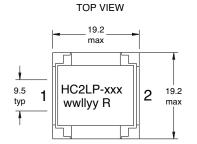
1. Open Circuit Inductance Test Parameters: 300kHz, 0.250 Vrms, 0.0 Adc

2. DC current for an approximate temperature change of 40°C without core loss. Derating is necessary for AC currents. PCB layout, trace thickness and width, air-flow and proximity of other heat generating components will affect the temperature rise. It is recommended that the temperature

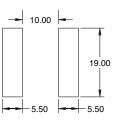
of the part not exceed 125°C under worst case operating conditions verified in the end application.

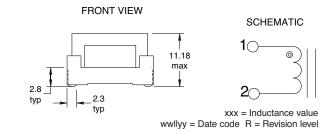
3. Peak current for approximately 30% rolloff.

Dimensions-mm



RECOMMENDED PCB PAD LAYOUT



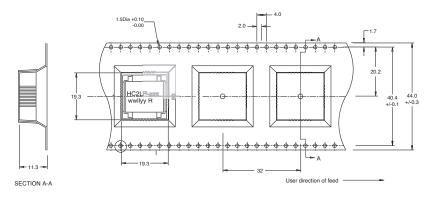


5. Applied Volt-Time product (V-µs) across the inductor. This value represents the applied V-µs at

300KHz neccessary to generate a core loss equal to 10% of the total losses for 40°C temperature rise.

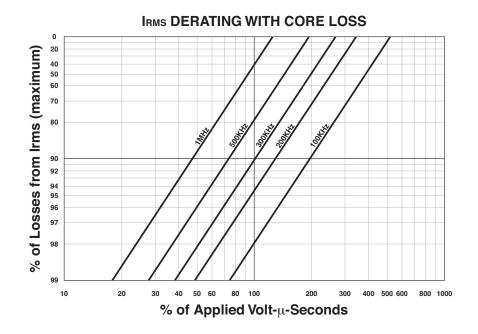
Packaging information (mm)

Supplied in tape and reel packaging, 130 parts per 13" reel.

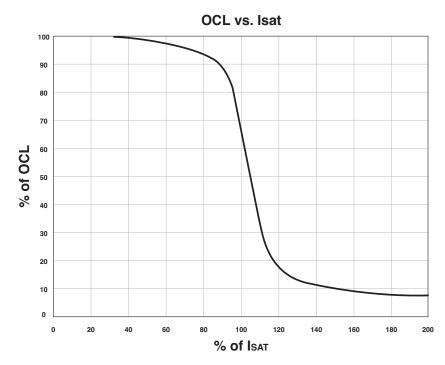


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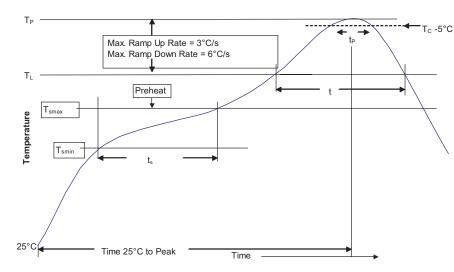
Core loss



Inductance Characteristics



Solder reflow profile



$-_{T_c - 5^{\circ}C}$ Table 1 - Standard SnPb Solder (T_c)

Package Thickness	Volume mm3 <350	Volume mm3 ≥350
<2.5mm)	235°C	220°C
≥2.5mm	220°C	220°C

Table 2 - Lead (Pb) Free Solder (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
<1.6mm	260°C	260°C	260°C
1.6 – 2.5mm	260°C	250°C	245°C
>2.5mm	250°C	245°C	245°C

Reference JDEC J-STD-020D

Profile Feature	Standard SnPb Solder	Lead (Pb) Free Solder	
Preheat and Soak • Temperature min. (T _{smin})	100°C	150°C	
• Temperature max. (T _{smax})	150°C	200°C	
• Time (T _{smin} to T _{smax}) (t _s)	60-120 Seconds	60-120 Seconds	
Average ramp up rate T _{smax} to T _p	3°C/ Second Max.	3°C/ Second Max.	
Liquidous temperature (TL) Time at liquidous (tL)	183°C 60-150 Seconds	217°C 60-150 Seconds	
Peak package body temperature (Tp)*	Table 1	Table 2	
Time $(t_p)^{**}$ within 5 °C of the specified classification temperature (T_c)	20 Seconds**	30 Seconds**	
Average ramp-down rate (T _p to T _{smax})	6°C/ Second Max.	6°C/ Second Max.	
Time 25°C to Peak Temperature	6 Minutes Max.	8 Minutes Max.	

* Tolerance for peak profile temperature (T_n) is defined as a supplier minimum and a user maximum.

** Tolerance for time at peak profile temperature (tp) is defined as a supplier minimum and a user maximum.

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