

# EMS41HJC-24.545454M

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## REGULATORY COMPLIANCE (Data Sheet downloaded on Dec 20, 2018)


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## ITEM DESCRIPTION

Spread Spectrum MEMS Clock Oscillators LVCMOS (CMOS) 1.8Vdc 4 Pad 2.0mm x 2.5mm Plastic Surface Mount (SMD) 24.545454MHz  $\pm 50$ ppm Maximum over  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  Power Down (Disabled Output Logic Low)  $\pm 1.00\%$  Center Spread

## ELECTRICAL SPECIFICATIONS

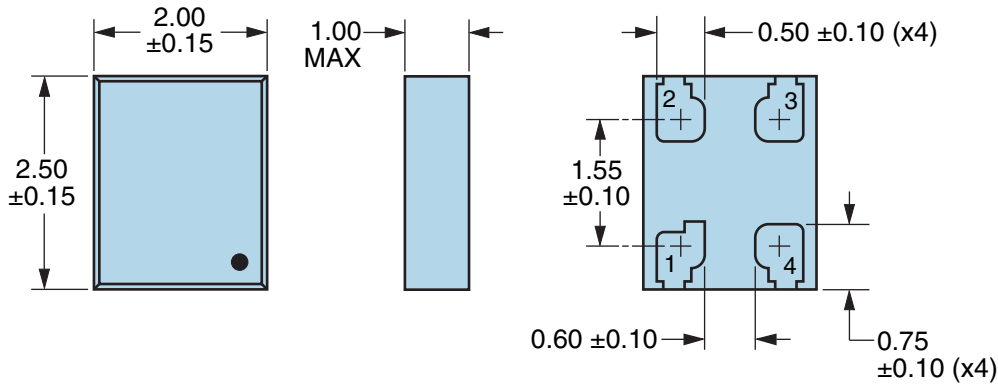
Nominal Frequency	24.545454MHz
Frequency Tolerance/Stability	$\pm 50$ ppm Maximum over $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Inclusive of all conditions: Calibration Tolerance at $25^{\circ}\text{C}$ , Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at $25^{\circ}\text{C}$ , $260^{\circ}\text{C}$ Reflow, Shock, and Vibration)
Aging at $25^{\circ}\text{C}$	$\pm 1$ ppm Maximum First Year
Supply Voltage	1.8Vdc $\pm 5\%$
Maximum Supply Voltage	$-0.5$ Vdc to $+1.98$ Vdc
Input Current	25mA Maximum (Unloaded; Nominal Vdd)
Output Voltage Logic High (Voh)	90% of Vdd Minimum (IOH= $-8$ mA)
Output Voltage Logic Low (Vol)	10% of Vdd Maximum (IOL= $+8$ mA)
Rise/Fall Time	2nSec Maximum (Measured from 20% to 80% of waveform)
Duty Cycle	50 $\pm 5$ (%) (Measured at 50% of waveform)
Load Drive Capability	15pF Maximum
Output Logic Type	CMOS
Output Control Function	Power Down (Disabled Output Logic Low)
Power Down Input Voltage (Vih and Vil)	70% of Vdd Minimum or No Connection to Enable Output, 30% of Vdd Maximum to Disable Output
Standby Current	50 $\mu$ A Maximum (Disabled Output: Logic Low) (Pad 1=Ground)
Spread Spectrum	$\pm 1.00\%$ Center Spread
Modulation Frequency	30kHz Minimum, 32kHz Typical, 35kHz Maximum
Period Jitter	90pSec Maximum (Cycle to Cycle; Spread Spectrum-On; Fo=133.333M, Vdd=1.8Vdc)
Start Up Time	10mSec Maximum
Storage Temperature Range	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

## ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

ESD Susceptibility	MIL-STD-883, Method 3015, Class 2, HBM 2000V
Flammability	UL94-V0
Mechanical Shock	MIL-STD-883, Method 2002, Condition G, 30,000G
Moisture Resistance	MIL-STD-883, Method 1004
Moisture Sensitivity Level	J-STD-020, MSL 1
Resistance to Soldering Heat	MIL-STD-202, Method 210, Condition K
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-883, Method 2003 (Pads on Bottom of Package Only)
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Thermal Shock	MIL-STD-883, Method 1011, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A, 20G

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### MECHANICAL DIMENSIONS (all dimensions in millimeters)

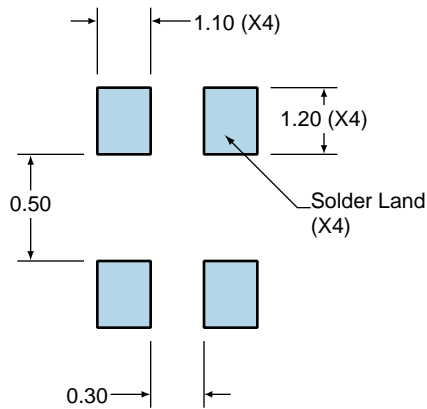


PIN	CONNECTION
1	Power Down (Logic Low)
2	Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	XXXX or XXXXX XXXX or XXXXX=Ecliptek Manufacturing Identifier

### Suggested Solder Pad Layout

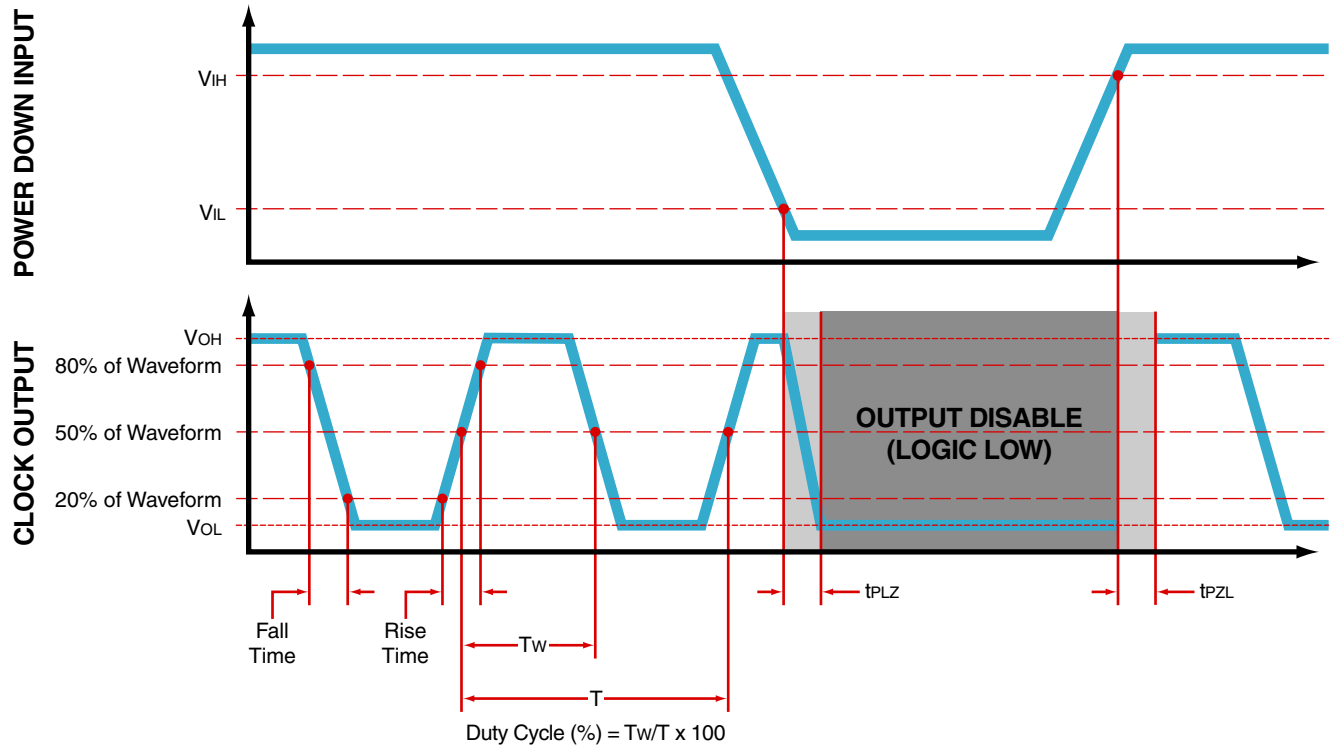
All Dimensions in Millimeters



All Tolerances are ±0.1

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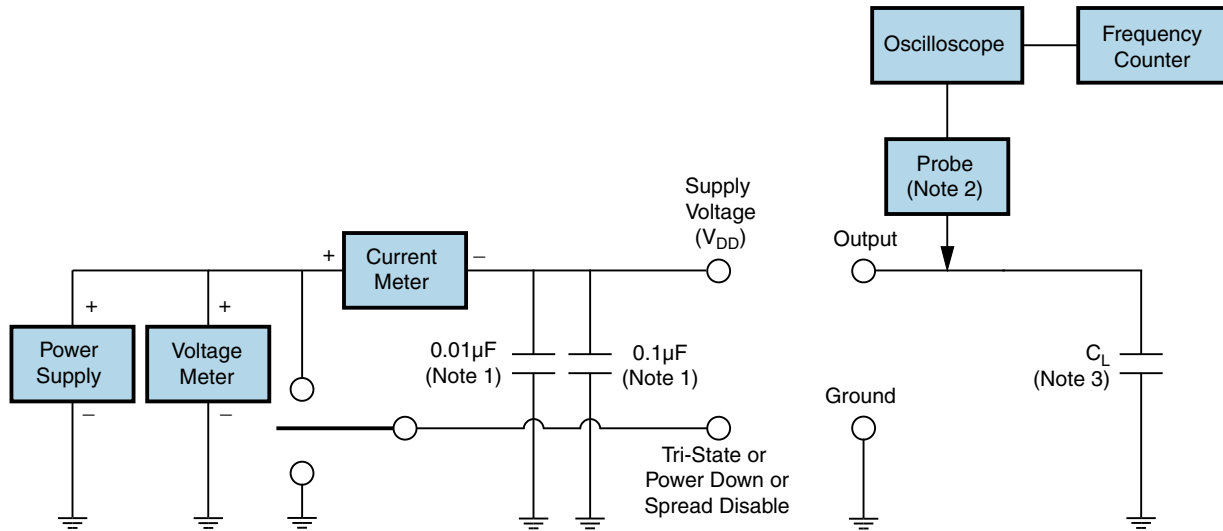
**OUTPUT WAVEFORM & TIMING DIAGRAM**



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## Test Circuit for CMOS Output



Note 1: An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

Note 3: Capacitance value C<sub>L</sub> includes sum of all probe and fixture capacitance.

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