

# EC5720TS-24.576M

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## REGULATORY COMPLIANCE (Data Sheet downloaded on Dec 5, 2018)


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## ITEM DESCRIPTION

Quartz Crystal Clock Oscillators XO (SPXO) LVCMOS (CMOS) 2.5Vdc 4 Pad 2.0mm x 2.5mm Ceramic Surface Mount (SMD) 24.576MHz  $\pm 20$ ppm -10°C to +70°C

## ELECTRICAL SPECIFICATIONS

|                                       |  |
|---------------------------------------|--|
| Nominal Frequency                     | 24.576MHz  |
| Frequency Tolerance/Stability         | $\pm 20$ ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, First Year Aging at 25°C, Shock, and Vibration) |
| Operating Temperature Range           | -10°C to +70°C   |
| Supply Voltage                        | 2.5Vdc $\pm 5\%$   |
| Input Current                         | 5.5mA Maximum  |
| Output Voltage Logic High (Voh)       | 90% of Vdd Minimum (IOH= -4mA)   |
| Output Voltage Logic Low (Vol)        | 10% of Vdd Maximum (IOL= +4mA)   |
| Rise/Fall Time                        | 10nSec Maximum (Measured at 20% to 80% of waveform)  |
| Duty Cycle                            | 50 $\pm 10$ (%) (Measured at 50% of waveform)  |
| Load Drive Capability                 | 15pF Maximum   |
| Output Logic Type                     | CMOS   |
| Pin 1 Connection                      | Tri-State (High Impedance)   |
| Tri-State Input Voltage (Vih and Vil) | 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)   |
| Standby Current                       | 10 $\mu$ A Maximum (Disabled Output: High Impedance)   |
| RMS Phase Jitter                      | 1pSec Maximum (12kHz to 20MHz offset frequency)  |
| Start Up Time                         | 10mSec Maximum   |
| Storage Temperature Range             | -55°C to +125°C  |

## ENVIRONMENTAL & MECHANICAL SPECIFICATIONS

|                              |   |
|------------------------------|---|
| ESD Susceptibility           | MIL-STD-883, Method 3015, Class 1, HBM: 1500V |
| Fine Leak Test               | MIL-STD-883, Method 1014, Condition A         |
| Flammability                 | UL94-V0                                       |
| Gross Leak Test              | MIL-STD-883, Method 1014, Condition C         |
| Mechanical Shock             | MIL-STD-883, Method 2002, Condition B         |
| Moisture Resistance          | MIL-STD-883, Method 1004                      |
| Moisture Sensitivity         | J-STD-020, MSL 1                              |
| Resistance to Soldering Heat | MIL-STD-202, Method 210, Condition K          |
| Resistance to Solvents       | MIL-STD-202, Method 215                       |
| Solderability                | MIL-STD-883, Method 2003                      |
| Temperature Cycling          | MIL-STD-883, Method 1010, Condition B         |
| Vibration                    | MIL-STD-883, Method 2007, Condition A         |

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### MECHANICAL DIMENSIONS (all dimensions in millimeters)



| PIN | CONNECTION     |
|-----|----------------|
| 1   | Tri-State      |
| 2   | Case/Ground    |
| 3   | Output         |
| 4   | Supply Voltage |

| LINE | MARKING   |
|------|---|
| 1    | <b>E24.5</b><br>E=Ecliptek Designator                   |
| 2    | <b>XXXXX</b><br>XXXXX=Ecliptek Manufacturing Identifier |

### Suggested Solder Pad Layout

All Dimensions in Millimeters



All Tolerances are  $\pm 0.1$

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**OUTPUT WAVEFORM & TIMING DIAGRAM**



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## Test Circuit for CMOS Output



Note 1: An external 0.01µF ceramic bypass capacitor in parallel with a 0.1µF high frequency ceramic bypass capacitor close (less than 2mm) to the package ground and supply voltage pin is required.

Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

Note 3: Capacitance value  $C_L$  includes sum of all probe and fixture capacitance.

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