T4 Data Sheet

Contents

Introduction

The T4 FPGA features the high-density, low-power Efinix® Quantum™ architecture wrapped with an I/O interface in a small footprint package for easy integration. T4 FPGAs support mobile, consumer, and IoT edge markets that need low power, low cost, and a small form factor. With ultra-low power T4 FPGAs, designers can build products that are always on, providing enhanced capabilities for applications such as embedded vision, voice and gesture recognition, intelligent sensor hubs, and power management.

Features

- High-density, low-power Quantum™ architecture
- Built on SMIC 40 nm process
- Less than 150 μA typical core leakage current at 1.1 V
- Ultra-small footprint package options
- FPGA interface blocks
  - GPIO
  - PLL
  - Oscillator
- Programmable high-performance I/O
  - Supports 1.8, 2.5, and 3.3 V single-ended I/O standards and interfaces
- Flexible on-chip clocking
  - 12 low-skew global clock signals can be driven from off-chip external clock signals or PLL synthesized clock signals
  - PLL support
- Flexible device configuration
  - Standard SPI interface (active, passive, and daisy chain)
  - JTAG interface
  - Optional Mask Programmable Memory (MPM) capability
- Fully supported by the Efinity® software, an RTL-to-bitstream compiler

Table 1: T4 FPGA Resources

LEs[1]	Global Clock Networks	Global Control Networks	Embedded Memory (kbits)	Embedded Memory Blocks (5 Kbits)	Embedded Multipliers
3,888	Up to 16	Up to 8	76.8	15	4

---

[1] Logic capacity in equivalent LE counts.

Table 2: T4 FPGA Package-Dependent Resources

Resource	BGA49	BGA81
Available GPIO	33	55
Global clock pins (available as GPIO)	12	12
PLL (simple)	1	1
Oscillator	1	1
MPM	1 (optional)	1 (optional)

Available Package Options

Table 3: Available Packages

Package	Dimensions (mm x mm)	Pitch (mm)
49-ball FBGA[2]	3 x 3	0.4
81-ball FBGA	5 x 5	0.5

Device Core Functional Description

T4 FPGAs feature an eXchangeable Logic and Routing (XLR) cell that Efinix has optimized for a variety of applications. Trion® FPGAs contain three building blocks constructed from XLR cells: LEs, embedded memory blocks, and multipliers. Each FPGA in the Trion® family has a custom number of building blocks to fit specific application needs. As shown in the following figure, the FPGA includes I/O ports on all four sides, as well as columns of LEs, memory, and multipliers. A control block within the FPGA handles configuration.

Figure 1: T4 FPGA Block Diagram

Quantum Fabric

I/O Ports from Core to Device Interface

Logic Elements and Routing

Each Device Contains Unique Interface Blocks such as GPIO and PLL

Note: The number and locations of rows and columns are shown for illustration purposes only. The actual number and position depends on the core.
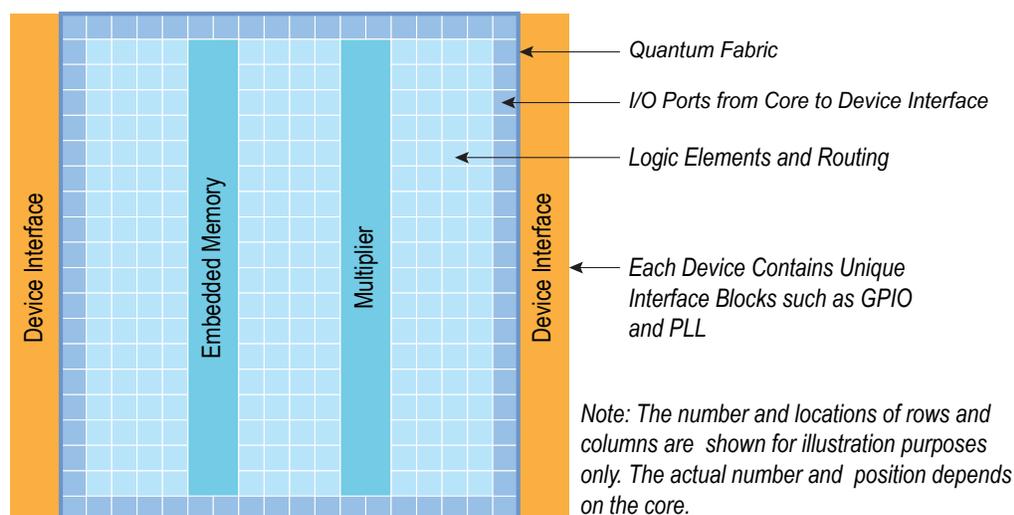
[2] This package does not have dedicated JTAG pins (TDI, TDO, TCK, TMS).

XLR Cell

The eXchangeable Logic and Routing (XLR) cell is the basic building block of the Quantum™ architecture. The Efinix XLR cell combines logic and routing and supports both functions interchangeably. This unique innovation greatly enhances the transistor flexibility and utilization rate, thereby reducing transistor counts and silicon area significantly.

Logic Cell

The LE comprises a 4-input LUT or a full adder plus a register (flipflop). You can program each LUT as any combinational logic function with four inputs. You can configure multiple LEs to implement arithmetic functions such as adders, subtractors, and counters.

Figure 2: Logic Element Block Diagram
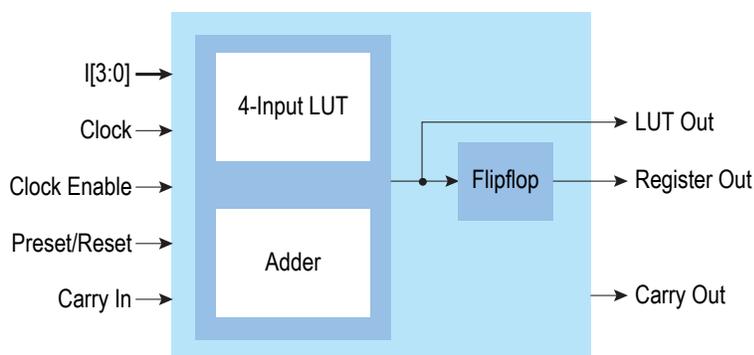
Embedded Memory

The core has 5-kbit high-speed, synchronous, embedded SRAM memory blocks. Memory blocks can operate as single-port RAM, simple dual-port RAM, true dual-port RAM, FIFOs, or ROM. You can initialize the memory content during configuration. The Efinity® software includes a memory cascading feature to connect multiple blocks automatically to form a larger array. This feature enables you to instantiate deeper or wider memory modules.

The memory read and write ports have the following modes for addressing the memory (depth x width):

256 x 16	1024 x 4	4096 x 1	512 x 10
512 x 8	2048 x 2	256 x 20	1024 x 5

The read and write ports support independently configured data widths.

Figure 3: Embedded Memory Block Diagram (True Dual-Port Mode)
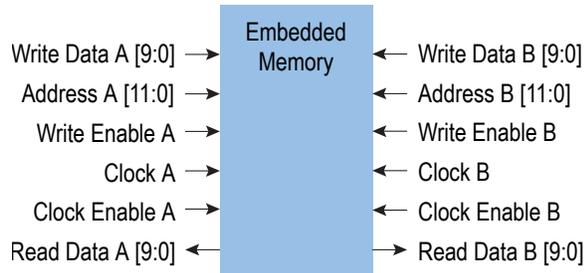
Multipliers

The FPGA has high-performance multipliers that support 18 x 18 fixed-point multiplication. Each multiplier takes two signed 18-bit input operands and generates a signed 36-bit output product. The multiplier has optional registers on the input and output ports.

Figure 4: Multiplier Block Diagram
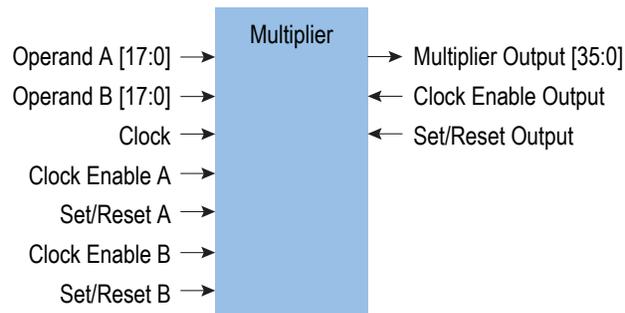
Global Clock Network

The Quantum™ core fabric supports up to 16 global clock (GCLK) signals feeding 16 pre-built global clock networks. Global clock pins (GPIO), PLL outputs, oscillator output, and core-generated clocks can drive the global clock network.

The global clock networks are balanced clock trees that feed all FPGA modules. Each network has dedicated clock-enable logic to save power by disabling the clock tree at the root. The logic dynamically enables/disables the network and guarantees no glitches at the output.

Figure 5: Global Clock Network
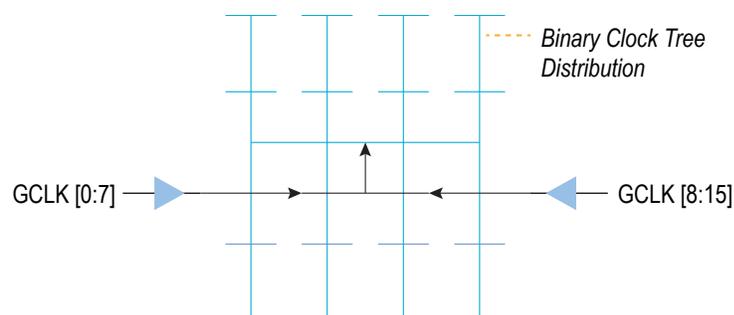
Device Interface Functional Description

The device interface wraps the core and routes signals between the core and the device I/O pads through a signal interface. Because they use the flexible Quantum™ architecture, devices in the Trion® family support a variety of interfaces to meet the needs of different applications.

Interface Block Connectivity

The FPGA core fabric connects to the interface blocks through a signal interface. The interface blocks then connect to the package pins. The core connects to the interface blocks using three types of signals:

- *Input*—Input data or clock to the FPGA core
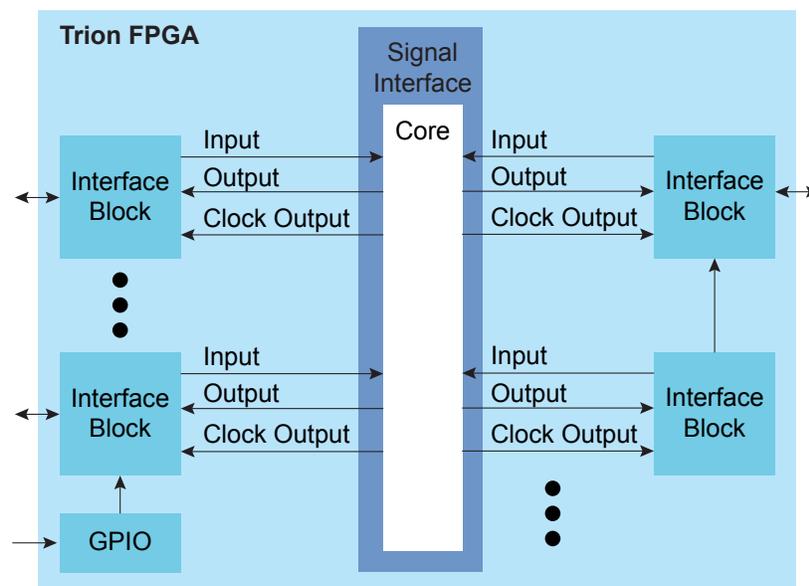- *Output*—Output from the FPGA core
- *Clock output*—Clock signal from the core clock tree

Figure 6: Interface Block and Core Connectivity

GPIO blocks are a special case because they can operate in several modes. For example, in alternate mode the GPIO signal can bypass the signal interface and directly feed another interface block. So a GPIO configured as an alternate input can be used as a PLL reference clock without going through the signal interface to the core.

When designing for Trion® FPGAs, you create an RTL design for the core and also configure the interface blocks. From the perspective of the core, outputs from the core are inputs to the interface block and inputs to the core are outputs from the interface block. The Efinity netlist always shows signals from the perspective of the core, so some signals do not appear in the netlist:

- GPIO used as reference clocks are not present in the RTL design, they are only visible in the interface block configuration.
- The FPGA clock tree is connected to the interface blocks directly. Therefore, clock outputs from the core to the interface are not present in the RTL design, they are only part of the interface configuration (this includes GPIO configured as output clocks).

The following sections describe the T4 interface blocks. Signals and block diagrams are shown from the perspective of the interface, not the core.

General-Purpose I/O Logic and Buffer

The GPIO support the 3.3 V LVTTL and 1.8 V, 2.5 V, and 3.3 V LVCMOS I/O standards. The GPIOs are grouped into banks. Each bank has its own VCCIO that sets the bank voltage for the I/O standard.

Each GPIO consists of I/O logic and an I/O buffer. I/O logic connects the core logic to the I/O buffers. I/O buffers are located at the periphery of the device.

The I/O logic comprises three register types:
- *Input*—Capture interface signals from the I/O before being transferred to the core logic
- *Output*—Register signals from the core logic before being transferred to the I/O buffers
- *Output enable*—Enable and disable the I/O buffers when I/O used as output

Table 4: GPIO Modes

GPIO Mode	Description
Input	Only the input path is enabled; optionally registered. If registered, the input path uses the input clock to control the registers (positively or negatively triggered). Select the alternate input path to drive the alternate function of the GPIO. The alternate path cannot be registered.
Output	Only the output path is enabled; optionally registered. If registered, the output path uses the output clock to control the registers (positively or negatively triggered). The output register can be inverted.
Bidirectional	The input, output, and OE paths are enabled; optionally registered. If registered, the input clock controls the input register, the output clock controls the output and OE registers. All registers can be positively or negatively triggered. Additionally, the input and output paths can be registered independently. The output register can be inverted.
Clock output	Clock output path is enabled.

The T4 I/O buffer supports weak pull-up mode, weak pull-down mode, and the input I/O buffer supports a Schmitt trigger mode. The output I/O buffer has four settings for programmable drive strength as well as an option to enable or disable the slew rate. Turn on the **Enable Slew Rate** option in the Efinity® Interface Designer for a slow slew rate; turn the option off for a fast slew rate. When the I/O buffer is disabled, the output value is tristated.

Note: Refer to Table 17: Single-Ended I/O Buffer Drive Strength Characteristics on page 15 for more information.

During configuration, all GPIO pins are tristated and configured in weak pull-up mode.

By default, unused GPIO pins are tristated and configured in weak pull-up mode. You can change the default mode to weak pull-down in the Interface Designer.

Simple I/O Buffer

Figure 7: /I/O Interface Block
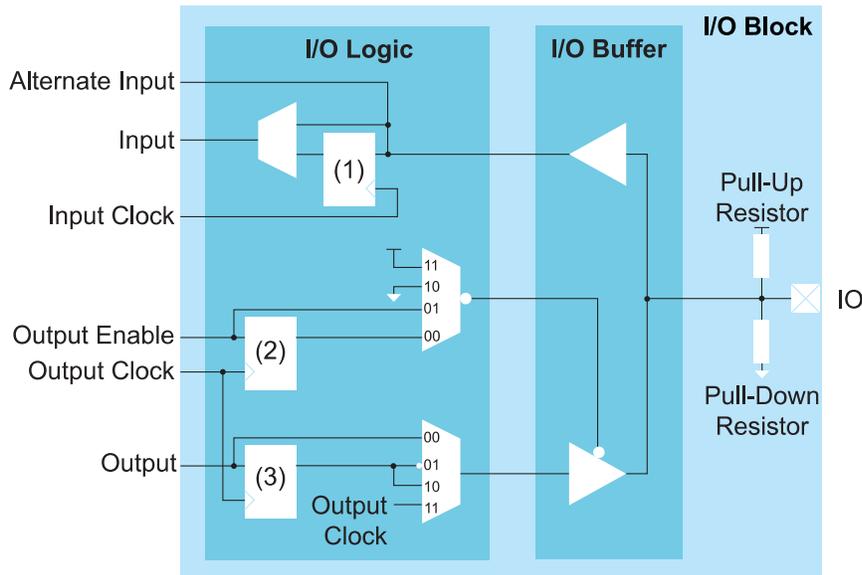
Notes:
1. Input Register
2. Output Enable Register
3. Output Register

Table 5: GPIO Signals

Signal	Direction	Description
IN	Output	Input data from the GPIO pad to the core fabric.
ALT	Output	Alternative input connection (in the Interface Designer, the input **Register Option** is **none**). Alternative connections are GCLK, GCTRL, and PLLCLK.
OUT	Input	Output data to GPIO pad from the core fabric.
OE	Input	Output enable from core fabric to the I/O block. Can be registered.
OUTCLK	Input	Core clock that controls the output and OE register. This clock is not visible in the user netlist.
INCLK	Input	Core clock that controls the input register. This clock is not visible in the user netlist.

Table 6: GPIO Pads

Signal	Direction	Description
IO	Bidirectional	GPIO pad.

I/O Banks

Trion FPGAs have input/output (I/O) banks for general-purpose usage. Each I/O bank has independent power pins. The number and voltages supported vary by FPGA and package.

Table 7: I/O Banks by Package

Package	I/O Banks	Voltage (V)	Banks with DDIO Support	Merged Banks
BGA49, BGA81	1A - 1C, 2A, 2B	1.8, 2.5, 3.3	–	–

Learn more: Refer to the T4 Pinout for information on the I/O bank assignments.

PLL

The T4 has 1 PLL to synthesize clock frequencies. The PLL's reference clock input comes from a dedicated GPIO's alternate input pin. The PLL consists of a pre-divider counter (N counter), a feedback multiplier counter (M counter), post-divider counter (O counter), and an output divider per clock output.

Figure 8: T4 PLL Block Diagram
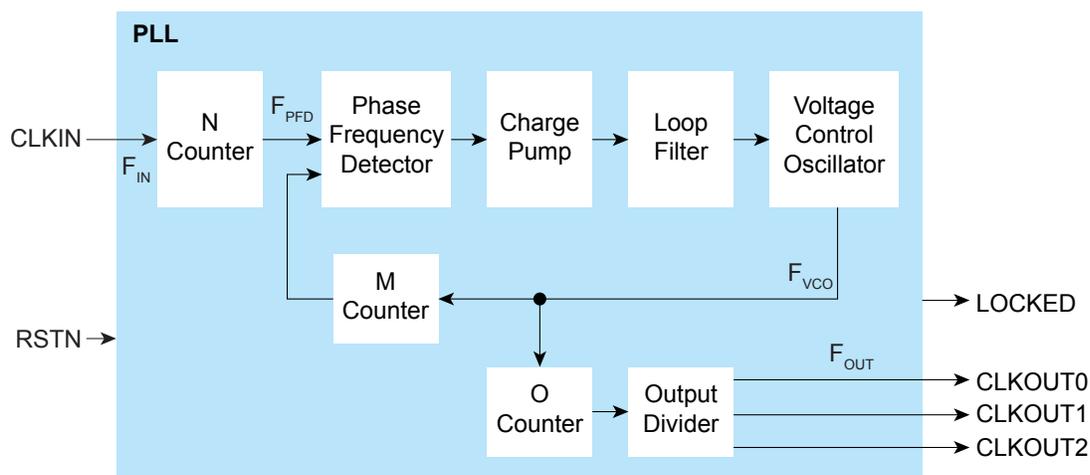
The counter settings define the PLL output frequency:	where:
$F_{PFD} = F_{IN} / N$ $F_{VCO} = F_{PFD} \times M$ $F_{OUT} = F_{VCO} / (O \times \text{Output divider})$	F_{VCO} is the voltage control oscillator frequency F_{OUT} is the output clock frequency F_{IN} is the reference clock frequency F_{PFD} is the phase frequency detector input frequency

Note: The reference clock must be between 10 and 50 MHz.
The PFD input must be between 10 and 50 MHz.
The VCO frequency must be between 500 and 1,500 MHz.

Table 8: PLL Pins

Port	Direction	Description
CLKIN	Input	Reference clock. This port is also a GPIO pin; the GPIO pins' alternate function is configured as a reference clock.
RSTN	Input	Active-low PLL reset signal. When asserted, this signal resets the PLL; when de-asserted, it enables the PLL. Connect this signal in your design to power up or reset the PLL. Assert the RSTN pin for a minimum pulse of 10 ns to reset the PLL.
CLKOUT0 CLKOUT1 CLKOUT2	Output	PLL output. The designer can route these signals as input clocks to the core's GCLK network.
LOCKED	Output	Goes high when PLL achieves lock; goes low when a loss of lock is detected. Connect this signal in your design to monitor the lock status. This signal is analog asynchronous.

Table 9: PLL Settings

Configure these settings in the Efinity® Interface Designer.

Setting	Allowed Values	Notes
N counter	1 - 15 (integer)	Pre-divider
M counter	1 - 255 (integer)	Multiplier
O counter	1, 2, 4, 8	Post-divider
Output divider	2, 4, 8, 16, 32, 64, 128, 256	Output divider per output

Clock and Control Distribution Network

The global clock network is distributed through the device to provide clocking for the core's LEs, memory, multipliers, and I/O blocks. Designers can access the T4 global clock network using the global clock GPIO pins, PLL outputs, oscillator output, and core-generated clocks. Similarly, the T4 has GPIO pins (the number varies by package) that the designer can configure as control inputs to access the high-fanout network connected to the LE's set, reset, and clock enable signals.

Learn more: Refer to the T4 pinout for information on the location and names of these pins.

Oscillator

The T4 has 1 low-frequency oscillator tailored for low-power operation. The oscillator runs at nominal frequency of 10 kHz. Designers can use the oscillator to perform always-on functions with the lowest power possible. Its output clock is available to the GCLK network.
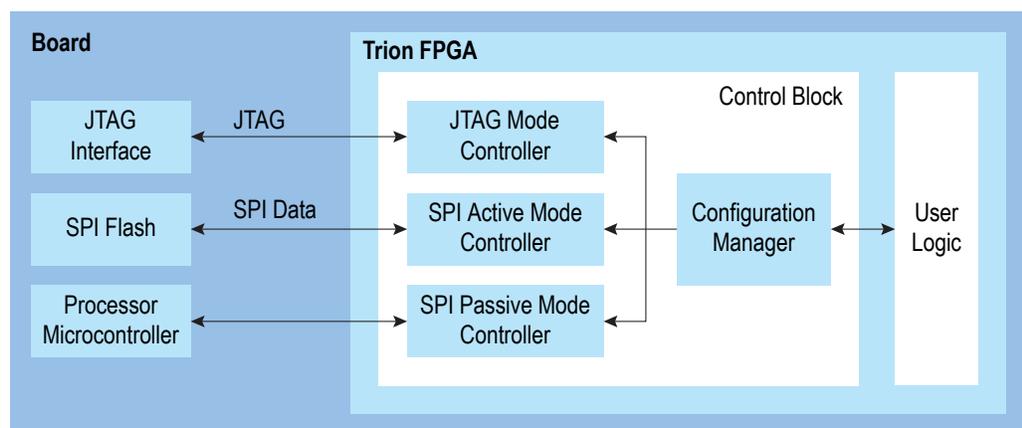
Configuration

The T4 FPGA contains volatile Configuration RAM (CRAM). The user must configure the CRAM for the desired logic function upon power-up and before the FPGA enters normal operation. The FPGA's control block manages the configuration process and uses a bitstream to program the CRAM. The Efinity® software generates the bitstream, which is design dependent. You can configure the T4 FPGA(s) in active, passive, or JTAG mode.

Learn more: Refer to AN 006: Configuring Trion FPGAs for details on the dedicated configuration pins and how to configure FPGA(s).

Figure 9: High-Level Configuration Options

In active mode, the FPGA controls the configuration process. An oscillator circuit within the FPGA provides the configuration clock. The bitstream is typically stored in an external serial flash device, which provides the bitstream when the FPGA requests it.

The control block sends out the instruction and address to read the configuration data. First, it issues a release from power-down instruction to wake up the external SPI flash. Then, it waits for at least 30 μs before issuing a fast read command to read the content of SPI flash from address 24h'000000.

In passive mode, the FPGA is the slave and relies on an external master to provide the control, bitstream, and clock for configuration. Typically the master is a microcontroller or another FPGA in active mode.

In JTAG mode, you configure the FPGA via the JTAG interface.

Supported Configuration Modes

Table 10: T4 Configuration Modes by Package

Configuration Mode	Width	BGA49	BGA81
Active	X1	✓	✓
	X2	✓	✓
	X4	✓	✓
Passive	X1	✓	✓
	X2	✓	✓
	X4	✓	✓
	X8	✓	✓
JTAG	X1		✓

Mask-Programmable Memory Option

The T4 FPGA is equipped with one-time programmable MPM. With this feature, you use on-chip MPM instead of an external serial flash device to configure the FPGA. This option is for systems that require an ultra-small factor and the lowest cost structure such that an external serial flash device is undesirable and/or not required at volume production. MPM is a one-time factory programmable option that requires a Non-Recurring Engineering (NRE) payment. To enable MPM, submit your design to our factory; our Applications Engineers (AEs) convert your design into a single configuration mask to be specially fabricated.

DC and Switching Characteristics

Table 11: Absolute Maximum Ratings [3]

Conditions beyond those listed may cause permanent damage to the device. Device operation at the absolute maximum ratings for extended periods of time has adverse effects on the device.

Symbol	Description	Min	Max	Units
VCC	Core power supply	-0.5	1.42	V
VCCIO	I/O bank power supply	-0.5	4.6	V
VCCA_PLL	PLL analog power supply	-0.5	1.42	V
T_J	Operating junction temperature	-40	125	°C

Table 12: Recommended Operating Conditions [3]

Symbol	Description	Min	Typ	Max	Units
VCC	Core power supply	1.05	1.1	1.15	V
VCCIO	1.8 V I/O bank power supply	1.71	1.8	1.89	V
	2.5 V I/O bank power supply	2.38	2.5	2.63	V
	3.3 V I/O bank power supply	3.14	3.3	3.47	V
VCCA_PLL	PLL analog power supply	1.05	1.1	1.15	V
T_{JCOM}	Operating junction temperature, commercial	0	–	85	°C

Table 13: Power Supply Ramp Rates

Symbol	Description	Min	Max	Units
t_{RAMP}	Power supply ramp rate for all supplies.	0.01	10	V/ms

Table 14: Static Supply Current

Symbol	Parameter	Typ	Units
I_{CC}	Typical standby (Low Power [LP] option)[4]	150	μA
I_{CC}	Typical standby	500	μA

Table 15: Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2	VCCIO + 0.3	0.2	VCCIO - 0.2
3.3 V LVTTL	-0.3	0.8	2	VCCIO + 0.3	0.4	2.4

---

[3] Supply voltage specification applied to the voltage taken at the device pins with respect to ground, not at the power supply.
[4] This specification is for the commercial grade -1 speed grade device only.

I/O Standard	V$_{IL}$ (V)		V$_{IH}$ (V)		V$_{OL}$ (V)	V$_{OH}$ (V)
	Min	Max	Min	Max	Max	Min
2.5 V LVCMOS	-0.3	0.7	1.7	VCCIO + 0.3	0.5	1.8
1.8 V LVCMOS	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO + 0.3	0.45	VCCIO - 0.45

Table 16: Single-Ended I/O DC Electrical Characteristics

Voltage	VT+ (V) Schmitt Trigger Low-to-High Threshold	VT- (V) Schmitt Trigger High-to-Low Threshold	Input Leakage Current (µA)	Tristate Output Leakage Current (µA)
3.3	1.73	1.32	±10	±10
2.5	1.37	1.01	±10	±10
1.8	1.05	0.71	±10	±10

Table 17: Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at T$_J$ = 25 °C, power supply at nominal voltage, device in nominal process (TT).

I/O Standard	3.3 V		2.5 V		1.8 V	
Drive Strength	I$_{OH}$ (mA)	I$_{OL}$ (mA)	I$_{OH}$ (mA)	I$_{OL}$ (mA)	I$_{OH}$ (mA)	I$_{OL}$ (mA)
1	14.4	8.0	9.1	8.0	4.4	5.1
2	19.1	10.5	12.2	10.5	5.8	6.8
3	23.9	13.3	15.2	13.4	7.3	8.6
4	28.7	15.8	18.2	15.9	8.6	10.3

ESD Performance

Refer to the Trion Reliability Report for ESD performance data.

Timing Specifications

Configuration Timing

The T4 FPGA has the following configuration timing specifications. Refer to AN 006: Configuring Trion FPGAs for detailed configuration information.

Timing Waveforms
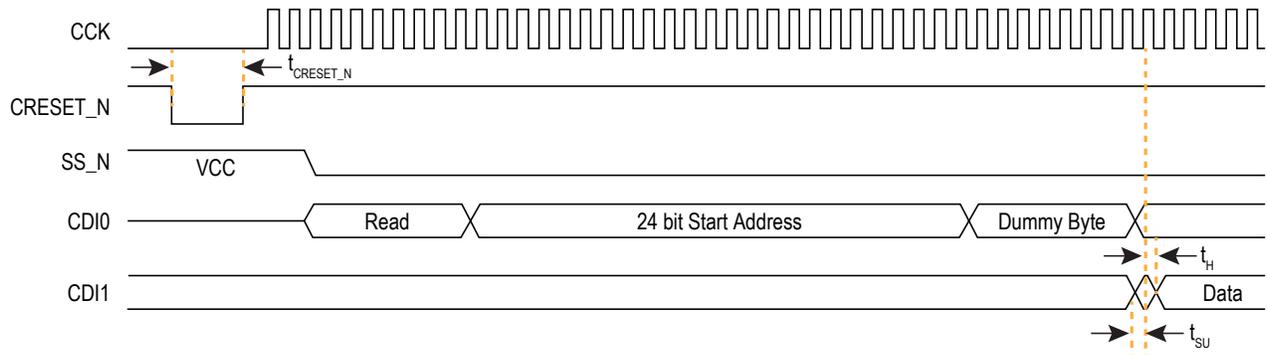
Figure 10: SPI Active Mode (x1) Timing Sequence

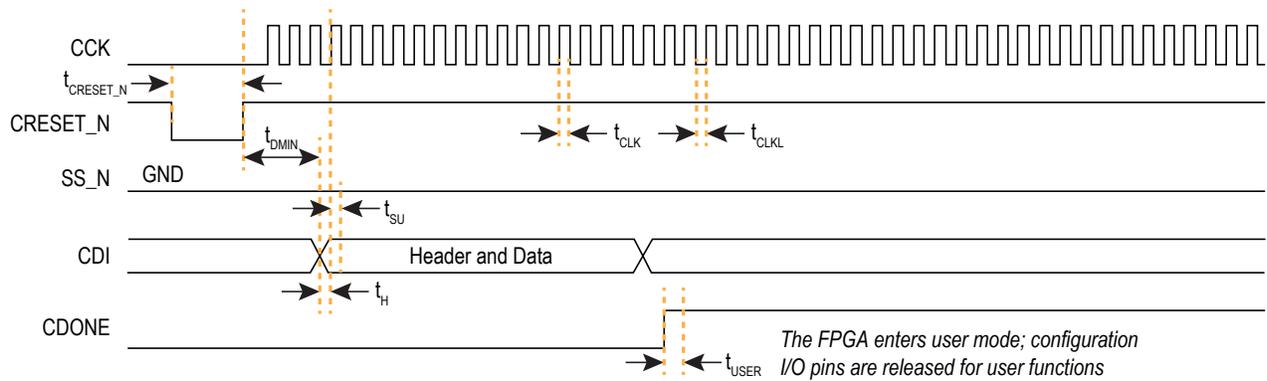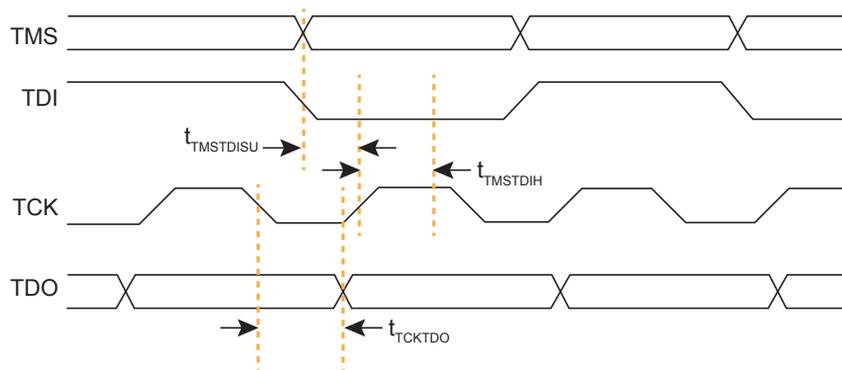
Figure 11: SPI Passive Mode (x1) Timing Sequence

Figure 12: Boundary Scan Timing Waveform

Timing Parameters

Table 18: All Modes

Symbol	Parameter	Min	Typ	Max	Units
t_{CRESET_N}	Minimum creset_n low pulse width required to trigger re-configuration.	320	–	–	ns
t_{USER}	Minimum configuration duration after CDONE goes high before entering user mode.[5]	8	–	–	µs

Table 19: Active Mode

Symbol	Parameter	Frequency	Min	Typ	Max	Units
f_{MAX_M}	Active mode configuration clock frequency.	DIV4	14	20	26	MHz
		DIV8	7	10	13	MHz

Table 20: Passive Mode

Symbol	Parameter	Min	Typ	Max	Units
f_{MAX_S}	Passive mode configuration clock frequency.	–	–	100	MHz
t_{CLKH}	Configuration clock pulse width high.	4.8	–	–	ns
t_{CLKL}	Configuration clock pulse width low.	4.8	–	–	ns
t_{SU}	Setup time.	4	–	–	ns
t_{H}	Hold time.	1	–	–	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to first valid configuration data.	1.2	–	–	µs

Table 21: JTAG Mode

Symbol	Parameter	Min	Typ	Max	Units
f_{TCK}	TCK frequency.	–	–	33	MHz
t_{TDISU}	TDI setup time.	3.5	–	–	ns
t_{TDIH}	TDI hold time.	1			ns
t_{TMSSU}	TMS setup time.	3			ns
t_{TMSH}	TMS hold time.	1			ns
t_{TCKTDO}	TCK falling edge to TDO output.	–	–	10.5[6]	ns

---

[5] The FPGA may go into user mode before t_{USER} has elapsed. However, Efinix recommends that you keep the system interface to the FPGA in reset until t_{USER} has elapsed.

[6] 0 pf output loading.

PLL Timing and AC Characteristics

The following tables describe the PLL timing and AC characteristics.

Table 22: PLL Timing

Symbol	Parameter	Min	Typ	Max	Units
F_{PFD}	Phase frequency detector input frequency.	10	–	50	MHz
F_{OUT}	Output clock frequency.	0.25 [7]	–	400 [7]	MHz
F_{VCO}	PLL VCO frequency.	500 [7]	–	1500 [7]	MHz

Table 23: PLL AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{DT}	Output clock duty cycle.	45 [7]	50	55 [7]	%
t_{OPJIT} (PK - PK)	Output clock period jitter (PK-PK).	–	100 [7]	–	ps
t_{LOCK}	PLL pull in plus lock-in time.	–	–	0.5	ms

Internal Oscillator

The internal oscillator has the following specifications.

Table 24: Internal Oscillator Specifications

Symbol	Parameter	Min	Typ	Max	Units
F_{CLKOSC}	Oscillator clock frequency.	–	10	–	kHz
D_{CHOSC}	Duty cycle.	45	50	55	%

---

[7] Pending hardware characterization.

Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

Table 25: General Pinouts

Function	Group	Direction	Description
VCC	Power	–	Core power supply.
VCCIO	Power	–	I/O pin power supply.
VCCA_PLL	Power	–	PLL analog power supply.
GND	Ground	–	Ground.
GNDA_PLL	Ground	–	PLL ground pin.
CLKn	Alternate	Input	Global clock network input. n is the number. The number of inputs is package dependent.
CTRLn	Alternate	Input	Global network input used for high fanout and global reset. n is the number. The number of inputs is package dependent.
PLLIN	Alternate	Input	PLL reference clock.
GPIOx_n	GPIO	I/O	General-purpose I/O for user function. User I/O pins are single ended. x: Indicates the bank (L or R) n: Indicates the GPIO number.
GPIOx_n_yyy GPIOx_n_yyy_zzz GPIOx_$zzzn$	GPIO Multi-Function	I/O	Multi-function, general-purpose I/O. These pins are single ended. If these pins are not used for their alternate function, you can use them as user I/O pins. x: Indicates the bank; left (L) or right (R). n: Indicates the GPIO number. yyy, yyy_zzz: Indicates the alternate function.

Table 26: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

Pins	Direction	Description	Use External Weak Pull-Up
CDONE	Output	Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, configuration is complete. If you hold CDONE low, the device will not enter user mode. CDONE is an open-drain output.	✓
CRESET_N	Input	Configuration reset pin (active low). Pulse CRESET_N low for t_{creset} time to reset the FPGA.	✓
TCK	Input	JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.	✓
TMS	Input	JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation . The signal value typically changes on the falling edge of TCK. TMS is typically a weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1.	✓
TDI	Input	JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI is typically a weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1.	✓
TDO	Output	JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or from a test data register depending on the sequence previously applied at TMS. During shifting, data applied at TDI appears at TDO after a number of cycles of TCK determined by the length of the register included in the serial path. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance).	✓

Table 27: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.

Pins	Direction	Description	Use External Weak Pull-Up
CBUS[2:0]	Input	Configuration bus width select. Connect to weak pull-up resistors if using default mode (x1).	✓
CBSEL[1:0]	Input	Optional multi-image selection input (if multi-image configuration mode is enabled).	N/A
CCK	I/O	Passive SPI input configuration clock or active SPI output configuration clock (active low). Includes an internal weak pull-up.	N/A
CDI*n*	I/O	*n* is a number from 0 to 31 depending on the SPI configuration. 0: Passive serial data input or active serial output. 1: Passive serial data output or active serial input. *n*: Parallel I/O.	N/A
CSI	Input	Chip select. 0: The FPGA is not selected or enabled and will not be configured. 1: Selects the FPGA for configuration.	✓

| Pins	Direction	Description	Use External Weak Pull-Up
CSO	Output	Chip select output. Selects the next device for cascading configuration.	N/A
NSTATUS	Output	Status (active low). Indicates a configuration error. This pin is active when there is a synchronization pattern mismatch or not found. When the FPGA drives this pin low, it indicates an ID mismatch, the bitstream CRC check has failed, or remote update has failed.	N/A
SS_N	Input	SPI slave select (active low). Includes an internal weak pull-up resistor to VCCIO during configuration. During configuration, the logic level samples on this pin determine the configuration mode. This pin is an input when sampled at the start of configuration (SS is low); an output in active SPI flash configuration mode. The FPGA senses the value of SS_N when it comes out of reset (pulse CRESET_N low to high). 0: Passive mode 1: Active mode	✓
TEST_N	Input	Active-low test mode enable signal. Set to 1 to disable test mode. During configuration, rely on the external weak pull-up or drive this pin high.	✓
RESERVED_OUT	Output	Reserved pin during user configuration. This pin drives high during user configuration. BGA49 and BGA81 packages only.	N/A

Efinity Software Support

The Efinity® software provides a complete tool flow from RTL design to bitstream generation, including synthesis, place-and-route, and timing analysis. The software has a graphical user interface (GUI) that provides a visual way to set up projects, run the tool flow, and view results. The software also has a command-line flow and Tcl command console. The software-generated bitstream file configures the T4 FPGA. The software supports the Verilog HDL and VHDL languages.

T4 Interface Floorplan

> **Note:** The numbers in the floorplan figures indicate the GPIO and LVDS number ranges. Some packages may not have all GPIO or LVDS pins in the range bonded out. Refer to the T4 pinout for information on which pins are available in each package.

Figure 13: Floorplan Diagram for BGA49 and BGA81 Packages
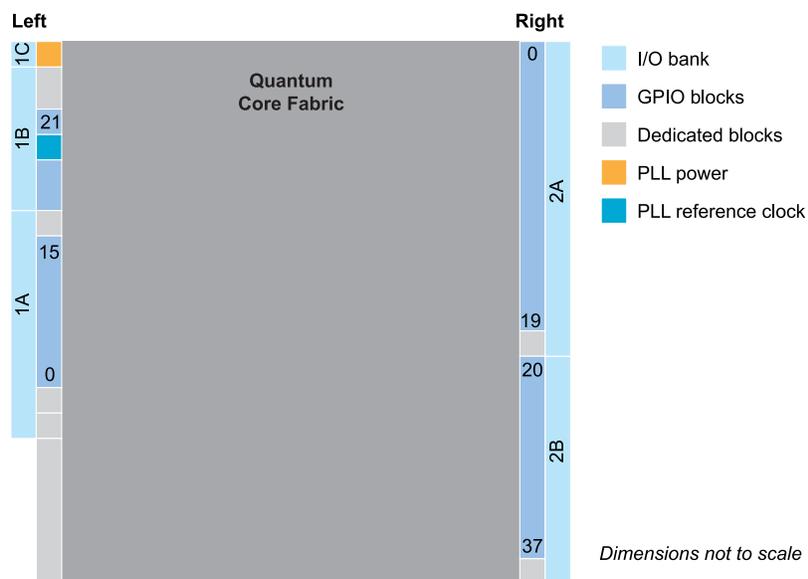
Ordering Codes

Refer to the Trion Selector Guide for the full listing of T4 ordering codes.

Revision History

Table 28: Revision History

Date	Version	Description
December 2019	1.9	Removed DIV1 and DIV2 active mode configuration frequencies; they are not supported.
October 2019	1.8	Added waveforms for configuration timing.
August 2019	1.7	Removed ESD table and added link to Trion Reliability Report. Minor formatting changes.
February 2019	1.6	Removed incorrect footnote about LVDS under Available Package Options.
November 2018	1.5	Updated PLL interface description. Added floorplan information. Updated configuraiton timing and PLL timing information.
August 2018	1.4	Updated configuration pin table. Renamed RST PLL pin as RSTN.
August 2018	1.3	Updated standby current specifications. Updated ordering codes.
July 2018	1.2	• Updated the PLL timing specification to add F_{PFD}. • Clarified the slew rate description.
May 2018	1.1	Added ordering code information.
April 2018	1.0	Initial release.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for efinix *manufacturer:*

Other Similar products are found below :

T8F81C2 T20F169C4 T4F81C2 T20F256C4 T13F256C4