T8 Data Sheet

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Contents

Introduction

The T8 FPGA features the high-density, low-power Efinix® Quantum™ architecture wrapped with an I/O interface in a small footprint package for easy integration. T8 FPGAs support mobile, consumer, and IoT edge markets that need low power, low cost, and a small form factor. With ultra-low power T8 FPGAs, designers can build products that are always on, providing enhanced capabilities for applications such as embedded vision, voice and gesture recognition, intelligent sensor hubs, and power management.

Features

- High-density, low-power Quantum™ architecture
- Built on SMIC 40 nm process
- Less than 150 µA typical core leakage current at 1.1 V(1)
- Ultra-small footprint package options
- FPGA interface blocks
  - GPIO
  - PLL
  - LVDS 600 Mbps per lane with up to 6 TX pairs and 6 RX pairs(2)
  - Oscillator
- Programmable high-performance I/O
  - Supports 1.8, 2.5, and 3.3 V single-ended I/O standards and interfaces(3)
- Flexible on-chip clocking
  - 12 low-skew global clock signals can be driven from off-chip external clock signals or PLL synthesized clock signals
  - PLL support
- Flexible device configuration
  - Standard SPI interface (active, passive, and daisy chain)
  - JTAG interface
  - Optional Mask Programmable Memory (MPM) capability
- Fully supported by the Efinity® software, an RTL-to-bitstream compiler

Table 1: T8 FPGA Resources

LEs(4)	Dedicated Global Clocks	Dedicated Global Controls	Embedded Memory (kbits)	Embedded Memory Blocks (5 Kbits)	Embedded Multipliers
7,384	Up to 16	Up to 8	122.88	24	8

(1) BGA49 and BGA81 packages only.
(2) LVDS pins are only available in QFP144 packages.
(3) LVDS pins used as GPIO only support 3.3 V.
(4) Logic capacity in equivalent LE counts.

Table 2: T8 FPGA Package-Dependent Resources

Resource	BGA49	BGA81	QFP144
Available GPIO	33	55	97
Global clock pins (available as GPIO)	4	8	6
PLL (simple)	1	1	–
PLL (advanced)	–	–	5
Oscillator	1	1	–
MPM	1 (optional)	1 (optional)	1 (optional)
LVDS[5]	–	–	6 TX pairs 6 RX pairs

Available Package Options

Table 3: Available Packages

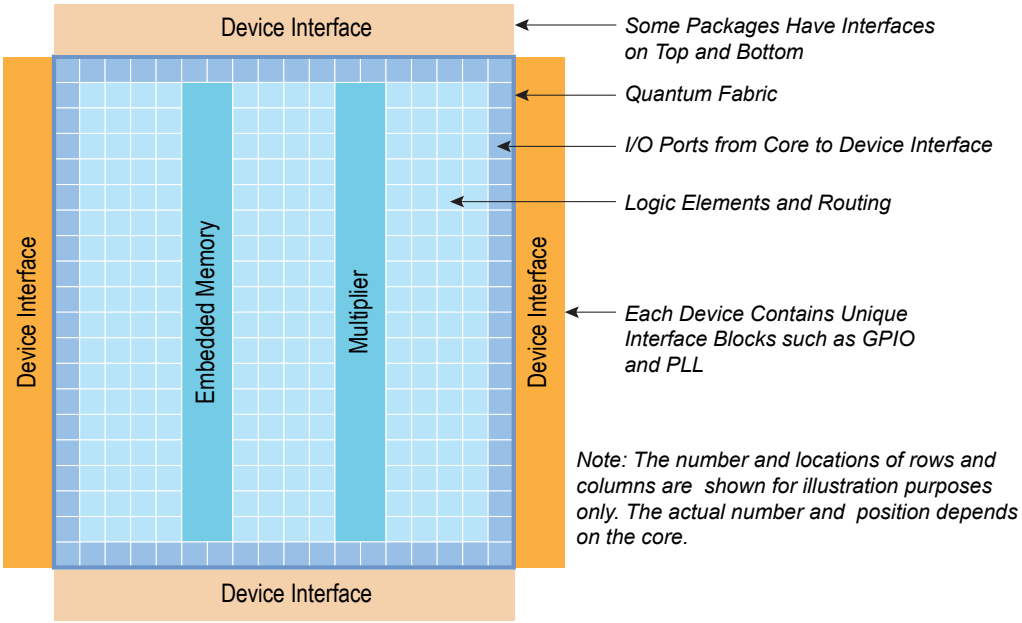
Package	Dimensions (mm x mm)	Pitch (mm)
49-ball FBGA[6]	3 x 3	0.4
81-ball FBGA	5 x 5	0.5
144-pin QFP	20 x 20	0.5

Device Core Functional Description

T8 FPGAs feature an eXchangeable Logic and Routing (XLR) cell that Efinix has optimized for a variety of applications. Trion® FPGAs contain three building blocks constructed from XLR cells: LEs, embedded memory blocks, and multipliers. Each FPGA in the Trion® family has a custom number of building blocks to fit specific application needs. As shown in the following figure, the FPGA includes I/O ports on all four sides, as well as columns of LEs, memory, and multipliers. A control block within the FPGA handles configuration.

[5] The LVDS I/O pins are dual-purpose. The full number of GPIO are available when all LVDS I/O pins are in GPIO mode.
[6] This package does not have dedicated JTAG pins (TDI, TDO, TCK, TMS).

Figure 1: T8 FPGA Block Diagram



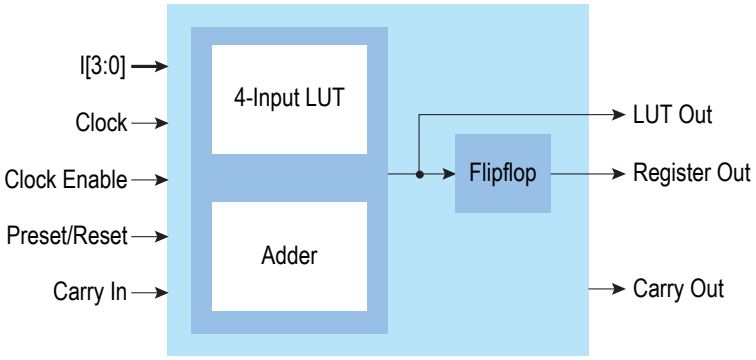
XLR Cell

The eXchangeable Logic and Routing (XLR) cell is the basic building block of the Quantum™ architecture. The Efinix XLR cell combines logic and routing and supports both functions interchangeably. This unique innovation greatly enhances the transistor flexibility and utilization rate, thereby reducing transistor counts and silicon area significantly.

Logic Cell

The LE comprises a 4-input LUT or a full adder plus a register (flipflop). You can program each LUT as any combinational logic function with four inputs. You can configure multiple LEs to implement arithmetic functions such as adders, subtractors, and counters.

Figure 2: Logic Element Block Diagram



Embedded Memory

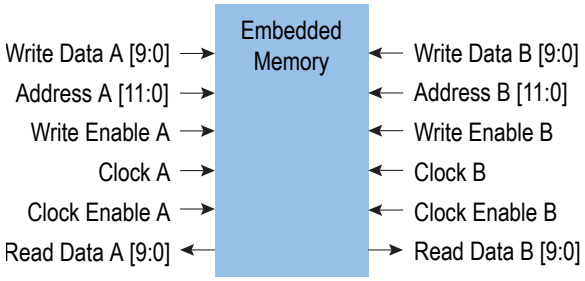
The core has 5-kbit high-speed, synchronous, embedded SRAM memory blocks. Memory blocks can operate as single-port RAM, simple dual-port RAM, true dual-port RAM, FIFOs, or ROM. You can initialize the memory content during configuration. The Efinity® software includes a memory cascading feature to connect multiple blocks automatically to form a larger array. This feature enables you to instantiate deeper or wider memory modules.

The memory read and write ports have the following modes for addressing the memory (depth x width):

256 x 16	1024 x 4	4096 x 1	512 x 10
512 x 8	2048 x 2	256 x 20	1024 x 5

The read and write ports support independently configured data widths.

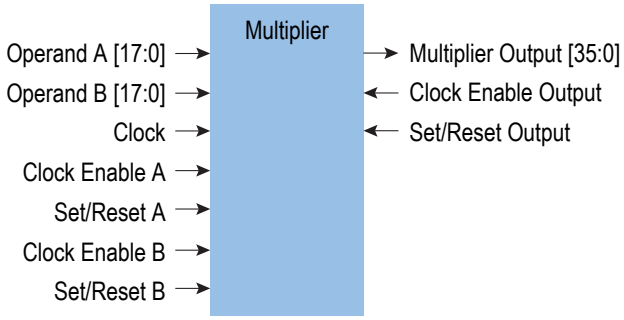
Figure 3: Embedded Memory Block Diagram (True Dual-Port Mode)



Multipliers

The FPGA has high-performance multipliers that support 18 x 18 fixed-point multiplication. Each multiplier takes two signed 18-bit input operands and generates a signed 36-bit output product. The multiplier has optional registers on the input and output ports.

Figure 4: Multiplier Block Diagram

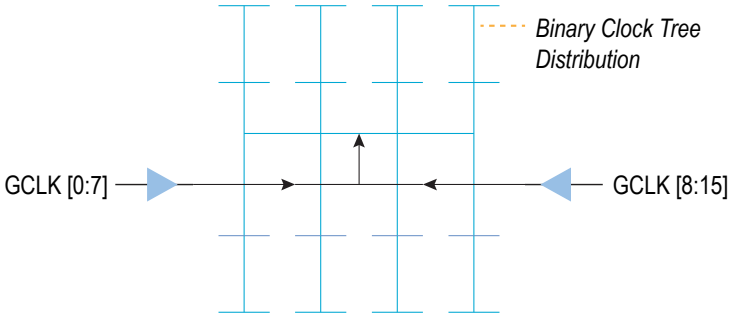


Global Clock Network

The Quantum™ core fabric supports up to 16 global clock (GCLK) signals feeding 16 pre-built global clock networks. Global clock pins (GPIO), PLL outputs, oscillator output, and core-generated clocks can drive the global clock network.

The global clock networks are balanced clock trees that feed all FPGA modules. Each network has dedicated clock-enable logic to save power by disabling the clock tree at the root. The logic dynamically enables/disables the network and guarantees no glitches at the output.

Figure 5: Global Clock Network



Device Interface Functional Description

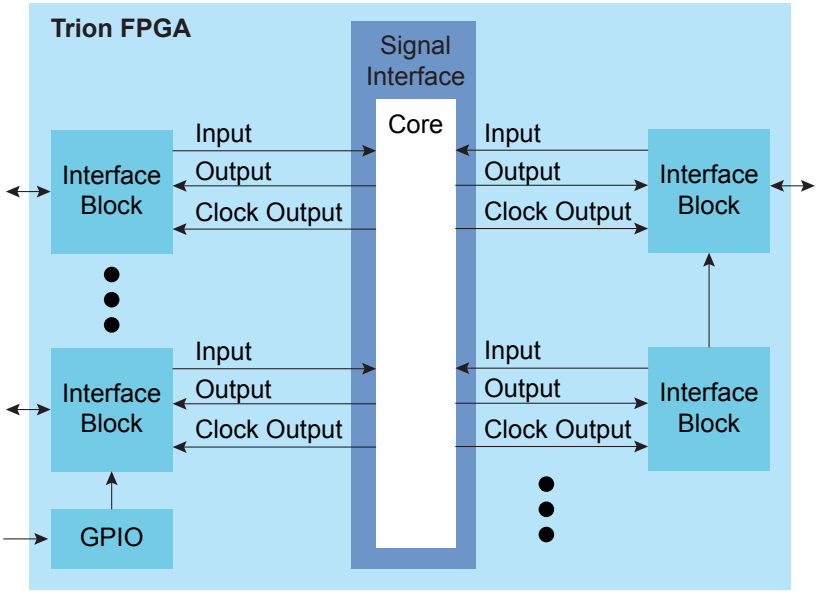
The device interface wraps the core and routes signals between the core and the device I/O pads through a signal interface. Because they use the flexible Quantum™ architecture, devices in the Trion® family support a variety of interfaces to meet the needs of different applications.

Interface Block Connectivity

The FPGA core fabric connects to the interface blocks through a signal interface. The interface blocks then connect to the package pins. The core connects to the interface blocks using three types of signals:

- *Input*—Input data or clock to the FPGA core
- *Output*—Output from the FPGA core
- *Clock output*—Clock signal from the core clock tree

Figure 6: Interface Block and Core Connectivity



GPIO blocks are a special case because they can operate in several modes. For example, in alternate mode the GPIO signal can bypass the signal interface and directly feed another interface block. So a GPIO configured as an alternate input can be used as a PLL reference clock without going through the signal interface to the core.

When designing for Trion® FPGAs, you create an RTL design for the core and also configure the interface blocks. From the perspective of the core, outputs from the core are inputs to the interface block and inputs to the core are outputs from the interface block. The Efinity netlist always shows signals from the perspective of the core, so some signals do not appear in the netlist:

- GPIO used as reference clocks are not present in the RTL design, they are only visible in the interface block configuration.
- The FPGA clock tree is connected to the interface blocks directly. Therefore, clock outputs from the core to the interface are not present in the RTL design, they are only part of the interface configuration (this includes GPIO configured as output clocks).

The following sections describe the T8 interface blocks. Signals and block diagrams are shown from the perspective of the interface, not the core.

Clock and Control Distribution Network

The global clock network is distributed through the device to provide clocking for the core's LEs, memory, multipliers, and I/O blocks. Designers can access the T8 global clock network using the global clock GPIO pins, PLL outputs, oscillator output, and core-generated clocks. Similarly, the T8 has GPIO pins (the number varies by package) that the designer can configure as control inputs to access the high-fanout network connected to the LE's set, reset, and clock enable signals.

Learn more: Refer to the T8 pinout for information on the location and names of these pins.

General-Purpose I/O Logic and Buffer

The GPIO support the 3.3 V LVTTL and 1.8 V, 2.5 V, and 3.3 V LVCMOS I/O standards. The GPIOs are grouped into banks. Each bank has its own VCCIO that sets the bank voltage for the I/O standard.

Each GPIO consists of I/O logic and an I/O buffer. I/O logic connects the core logic to the I/O buffers. I/O buffers are located at the periphery of the device.

The I/O logic comprises three register types:

- *Input*—Capture interface signals from the I/O before being transferred to the core logic
- *Output*—Register signals from the core logic before being transferred to the I/O buffers
- *Output enable*—Enable and disable the I/O buffers when I/O used as output

Table 4: GPIO Modes

GPIO Mode	Description
Input	Only the input path is enabled; optionally registered. If registered, the input path uses the input clock to control the registers (positively or negatively triggered). Select the alternate input path to drive the alternate function of the GPIO. The alternate path cannot be registered. **QFP144 packages:** In DDIO mode, two registers sample the data on the positive and negative edges of the input clock, creating two data streams.
Output	Only the output path is enabled; optionally registered. If registered, the output path uses the output clock to control the registers (positively or negatively triggered). The output register can be inverted. **QFP144 packages:** In DDIO mode, two registers capture the data on the positive and negative edges of the output clock, multiplexing them into one data stream.
Bidirectional	The input, output, and OE paths are enabled; optionally registered. If registered, the input clock controls the input register, the output clock controls the output and OE registers. All registers can be positively or negatively triggered. Additionally, the input and output paths can be registered independently. The output register can be inverted.
Clock output	Clock output path is enabled.

The T8 I/O buffer supports weak pull-up mode, weak pull-down mode, and the input I/O buffer supports a Schmitt trigger mode. The output I/O buffer has four settings for programmable drive strength[7] as well as an option to enable or disable the slew rate. Turn on the **Enable Slew Rate** option in the Efinity® Interface Designer for a slow slew rate; turn the option off for a fast slew rate. When the I/O buffer is disabled, the output value is tristated.

Note: Refer to Table 29: Single-Ended I/O Buffer Drive Strength Characteristics on page 26 and Table 35: Single-Ended I/O Buffer Drive Strength Characteristics on page 28 for more information.

During configuration, all GPIO pins are tristated and configured in weak pull-up mode.

By default, unused GPIO pins are tristated and configured in weak pull-up mode. You can change the default mode to weak pull-down in the Interface Designer.

[7] QFP144 packages: GPIO pins using LVDS resources do not have programmable drive strength.

I/O Banks

Trion FPGAs have input/output (I/O) banks for general-purpose usage. Each I/O bank has independent power pins. The number and voltages supported vary by FPGA and package.

The number of banks and the voltages they support vary by package.

Some I/O banks are merged at the package level by sharing VCCIO pins. Merged banks have underscores (_) between banks in the name (e.g., 1B_1C means 1B and 1C are connected).

Table 5: I/O Banks by Package

Package	I/O Banks	Voltage (V)	Banks with DDIO Support	Merged Banks
BGA49, BGA81	1A - 1C, 2A, 2B	1.8, 2.5, 3.3	–	–
QFP144	1A - 1E, 3A - 3E	1.8, 2.5, 3.3	1B, 1C, 1D, 3B, 3C, 3D, 3E	1C_1D, 3B_3C
	4A, 4B	3.3	–	–

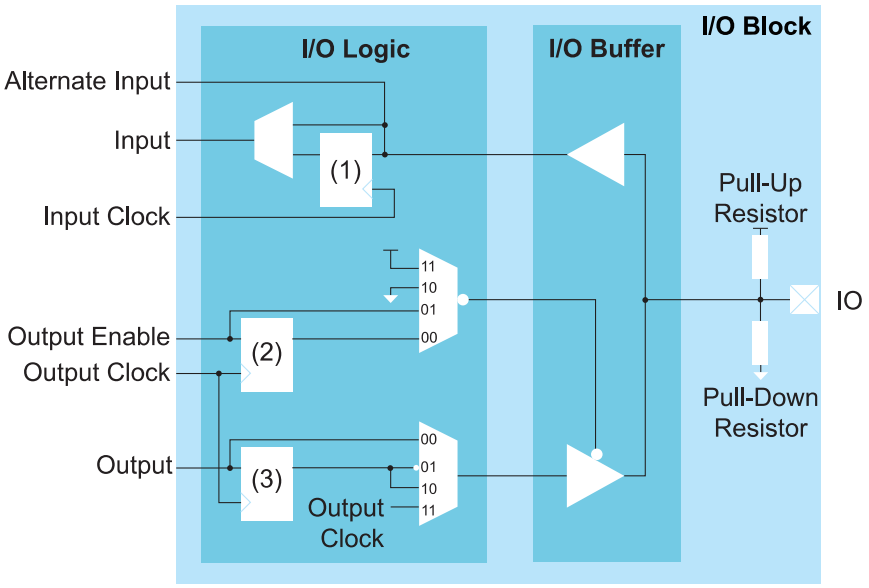
Learn more: Refer to the pinout file for information on the I/O bank assignments.

T8 BGA49 and BGA81 Interface Description

T8 FPGAs in BGA49 and BGA81 packages have simple general-purpose I/O logic and buffers, I/O banks, a simple PLL, and an oscillator.

Simple I/O Buffer

Figure 7: /I/O Interface Block



Notes:
1. Input Register
2. Output Enable Register
3. Output Register

Table 6: GPIO Signals

Signal	Direction	Description
IN	Output	Input data from the GPIO pad to the core fabric.
ALT	Output	Alternative input connection (in the Interface Designer, the input **Register Option** is **none**). Alternative connections are GCLK, GCTRL, and PLLCLK.
OUT	Input	Output data to GPIO pad from the core fabric.
OE	Input	Output enable from core fabric to the I/O block. Can be registered.
OUTCLK	Input	Core clock that controls the output and OE register. This clock is not visible in the user netlist.
INCLK	Input	Core clock that controls the input register. This clock is not visible in the user netlist.

Table 7: GPIO Pads

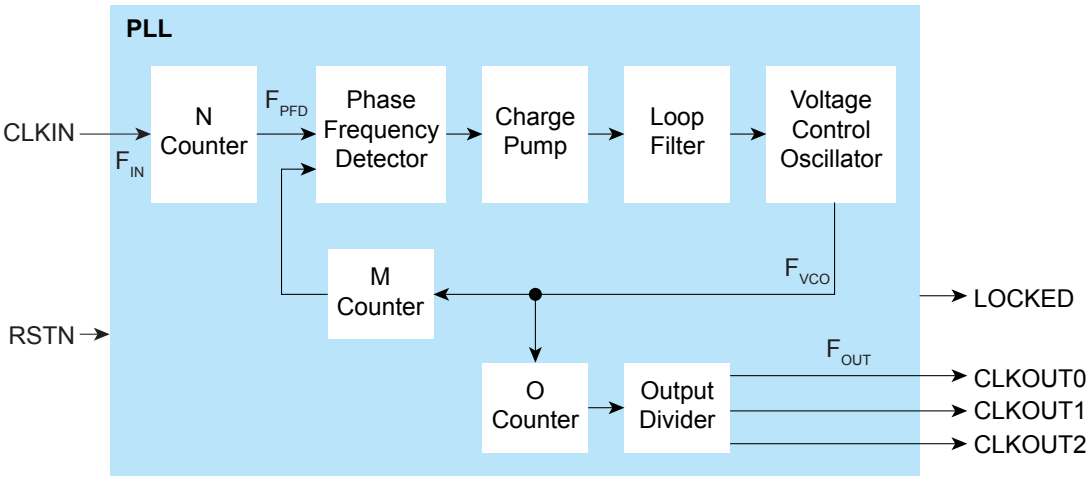
Signal	Direction	Description
IO	Bidirectional	GPIO pad.

Simple PLL

T8 FPGAs in BGA49 and BGA81 packages have a simple PLL.

The T8 has 1 PLL to synthesize clock frequencies. The PLL's reference clock input comes from a dedicated GPIO's alternate input pin. The PLL consists of a pre-divider counter (N counter), a feedback multiplier counter (M counter), post-divider counter (O counter), and an output divider per clock output.

Figure 8: T8 PLL Block Diagram



The counter settings define the PLL output frequency:	where:
$F_{PFD} = F_{IN} / N$ $F_{VCO} = F_{PFD} \times M$ $F_{OUT} = F_{VCO} / (O \times \text{Output divider})$	F_{VCO} is the voltage control oscillator frequency F_{OUT} is the output clock frequency F_{IN} is the reference clock frequency F_{PFD} is the phase frequency detector input frequency

Note: The reference clock must be between 10 and 50 MHz.
The PFD input must be between 10 and 50 MHz.
The VCO frequency must be between 500 and 1,500 MHz.

Table 8: PLL Pins

Port	Direction	Description
CLKIN	Input	Reference clock. This port is also a GPIO pin; the GPIO pins' alternate function is configured as a reference clock.
RSTN	Input	Active-low PLL reset signal. When asserted, this signal resets the PLL; when de-asserted, it enables the PLL. Connect this signal in your design to power up or reset the PLL. Assert the RSTN pin for a minimum pulse of 10 ns to reset the PLL.
CLKOUT0 CLKOUT1 CLKOUT2	Output	PLL output. The designer can route these signals as input clocks to the core's GCLK network.
LOCKED	Output	Goes high when PLL achieves lock; goes low when a loss of lock is detected. Connect this signal in your design to monitor the lock status. This signal is analog asynchronous.

Table 9: PLL Settings

Configure these settings in the Efinity® Interface Designer.

Setting	Allowed Values	Notes
N counter	1 - 15 (integer)	Pre-divider
M counter	1 - 255 (integer)	Multiplier
O counter	1, 2, 4, 8	Post-divider
Output divider	2, 4, 8, 16, 32, 64, 128, 256	Output divider per output

Oscillator

T8 FPGAs in BGA49 and BGA81 packages have an oscillator.

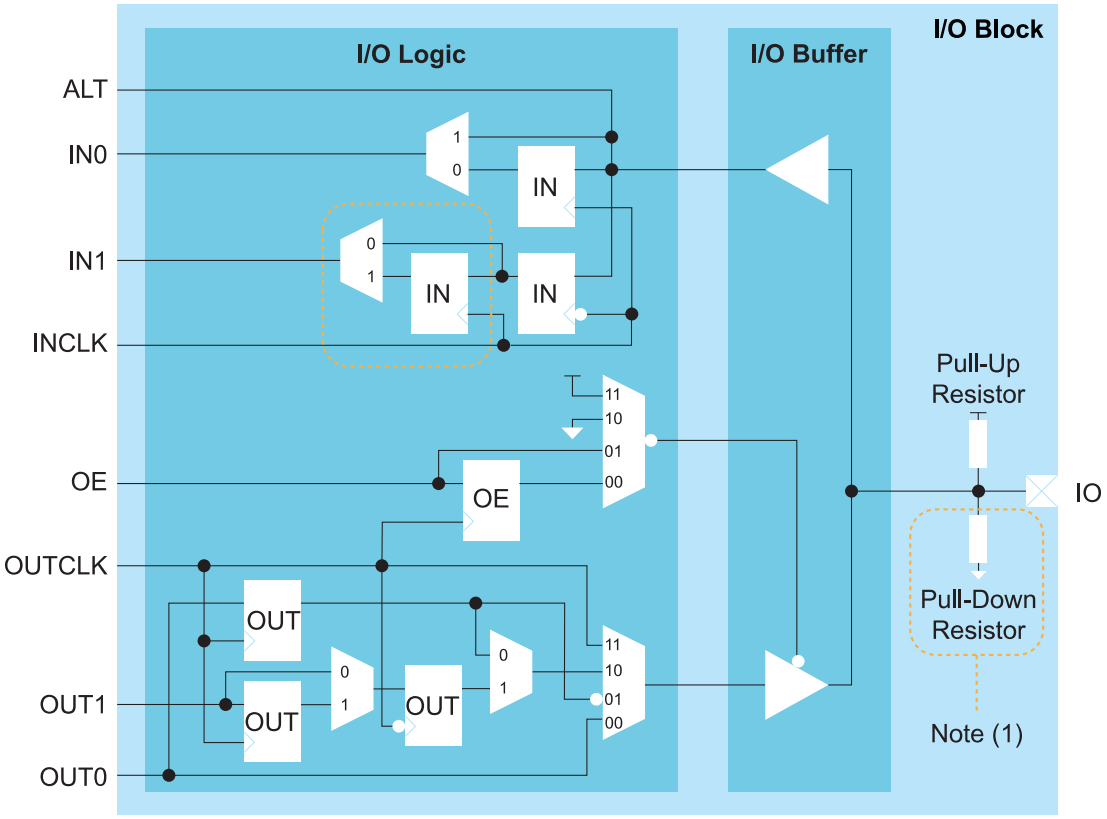
The T8 has 1 low-frequency oscillator tailored for low-power operation. The oscillator runs at nominal frequency of 10 kHz. Designers can use the oscillator to perform always-on functions with the lowest power possible. Its output clock is available to the GCLK network.

T8 QFP144 Interface Description

T8 FPGAs in QFP144 packages have an advanced general-purpose I/O logic and buffers, I/O banks, an advanced PLL, and an LVDS interface.

Complex I/O Buffer

Figure 9: I/O Interface Block



1. GPIO pins using LVDS resources do not have a pull-down resistor.

Note: LVDS pins configured as GPIO do not have double data I/O (DDIO).

Table 10: GPIO Signals

Signal	Direction	Description
IN[1:0]	Output	Input data from the GPIO pad to the core fabric. IN0 is the normal input to the core. In DDIO mode, IN0 is the data captured on the positive clock edge (HI pin name in the Interface Designer) and IN1 is the data captured on the negative clock edge (LO pin name in the Interface Designer).
ALT	Output	Alternative input connection (in the Interface Designer, **Register Option** is **none**). Alternative connections are GCLK, GCTRL, and PLLCLK.
OUT[1:0]	Input	Output data to GPIO pad from the core fabric. OUT0 is the normal output from the core. In DDIO mode, OUT0 is the data captured on the positive clock edge (HI pin name in the Interface Designer) and OUT1 is the data captured on the negative clock edge (LO pin name in the Interface Designer).
OE	Input	Output enable from core fabric to the I/O block. Can be registered.
OUTCLK	Input	Core clock that controls the output and OE registers. This clock is not visible in the user netlist.
INCLK	Input	Core clock that controls the input registers. This clock is not visible in the user netlist.

Table 11: GPIO Pads

Signal	Direction	Description
IO	Bidirectional	GPIO pad.

Double-Data I/O

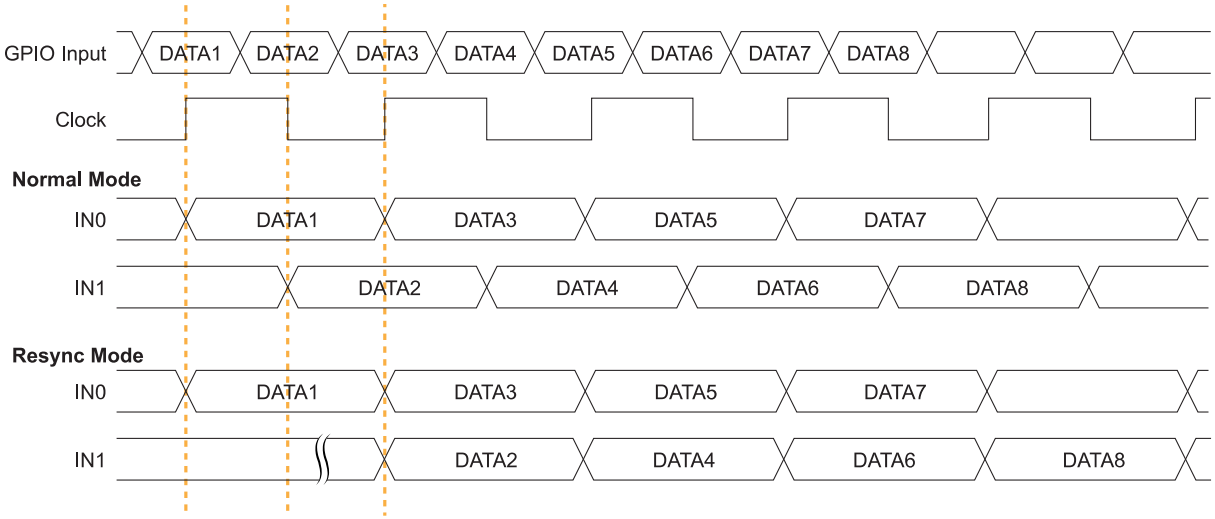
T8 FPGAs support double data I/O (DDIO) on input and output registers. In this mode, the DDIO register captures data on both positive and negative clock edges. The core receives 2 bit wide data from the interface.

In normal mode, the interface receives or sends data directly to or from the core on the positive and negative clock edges. In resync mode, the interface resynchronizes the data to pass both signals on the positive clock edge only.

Not all GPIO support DDIO; additionally, LVDS pins configured as single ended I/O do not support DDIO functionality.

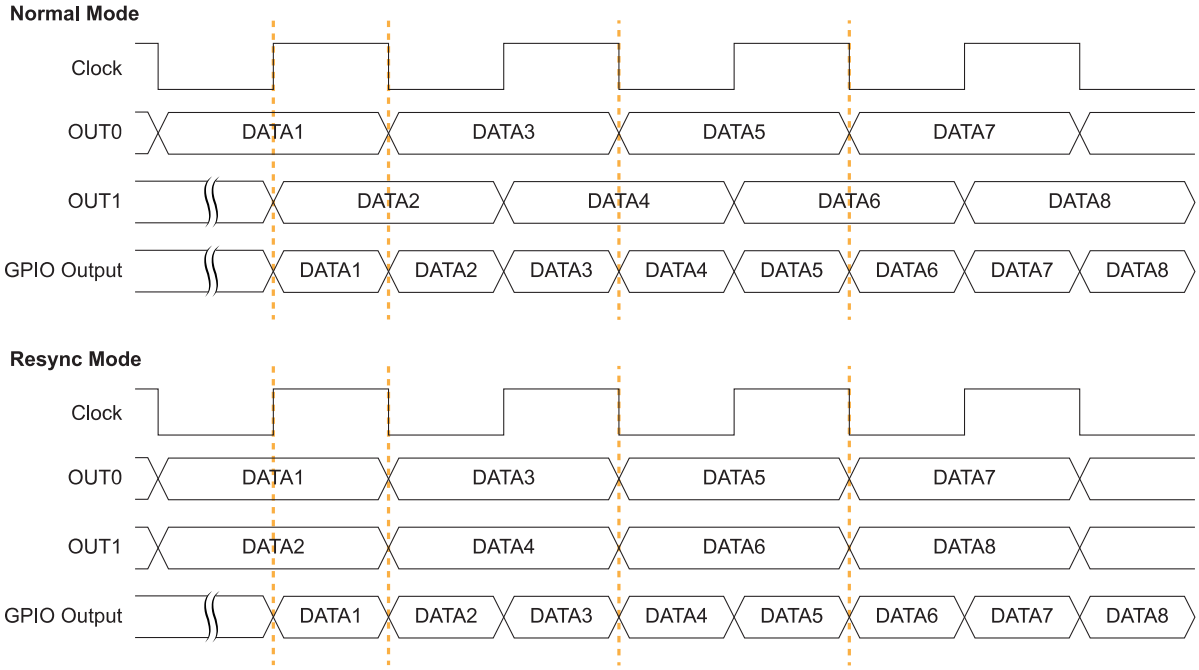
Note: The Resource Assigner in the Efinity® Interface Designer shows which GPIO support DDIO.

Figure 10: DDIO Input Timing Waveform



In resync mode, the IN1 data captured on the falling clock edge is delayed one half clock cycle.
In the Interface Designer, IN0 is the HI pin name and IN1 is the LO pin name.

Figure 11: DDIO Output Timing Waveform



In the Interface Designer, OUT0 is the HI pin name and OUT1 is the LO pin name.

Advanced PLL

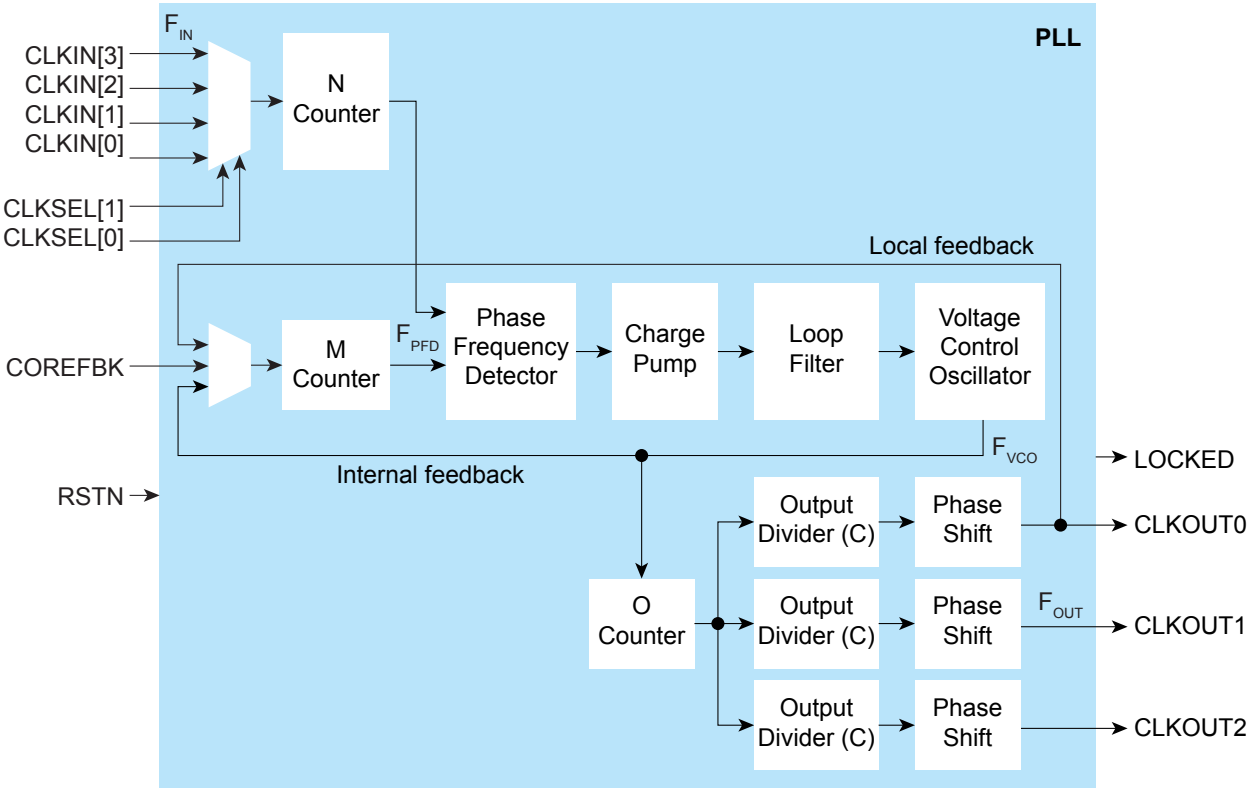
T8 FPGAs in QFP144 packages have an advanced I/O logic block and buffer.

You can use the PLL to compensate for clock skew/delay via external or internal feedback to meet timing requirements in advanced application. The PLL reference clock has up to four sources. You can dynamically select the PLL reference clock with the `CLKSEL` port. (Hold the PLL in reset when dynamically selecting the reference clock source.)

One of the PLLs can use an LVDS RX buffer to input it's reference clock.

The PLL consists of a pre-divider counter (N counter), a feedback multiplier counter (M counter), a post-divider counter (O counter), and output divider.

Figure 12: PLL Block Diagram



The counter settings define the PLL output frequency:

Internal Feedback Mode	Local and Core Feedback Mode	Where:
$F_{PFD} = F_{IN} / N$ $F_{VCO} = F_{PFD} \times M$ $F_{OUT} = (F_{IN} \times M) / (N \times O \times C)$	$F_{PFD} = F_{IN} / N$ $F_{VCO} = (F_{PFD} \times M \times O \times C_{FBK})$ [8] $F_{OUT} = (F_{IN} \times M \times C_{FBK}) / (N \times C)$	F_{VCO} is the voltage control oscillator frequency F_{OUT} is the output clock frequency F_{IN} is the reference clock frequency F_{PFD} is the phase frequency detector input frequency C is the output divider

Note: The reference clock must be between 10 and 200 MHz.
The PFD input must be between 10 and 50 MHz.
The VCO frequency must be between 500 and 1,500 MHz.

[8] $(M \times O \times C_{FBK})$ must be ≤ 255.

Figure 13: PLL Interface Block Diagram

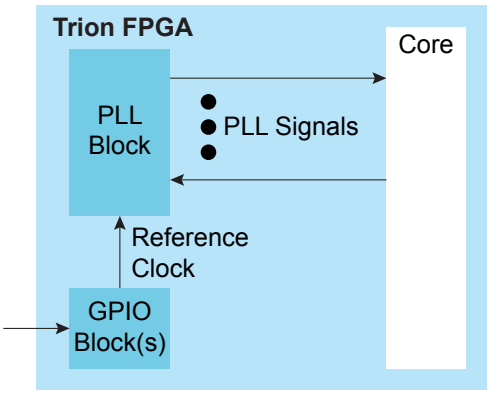


Table 12: PLL Signals (Interface to FPGA Fabric)

Signal	Direction	Description
CLKIN[3:0]	Input	Reference clocks driven by I/O pads or core clock tree.
CLKSEL[1:0]	Input	You can dynamically select the reference clock from one of the clock in pins.
RSTN	Input	Active-low PLL reset signal. When asserted, this signal resets the PLL; when de-asserted, it enables the PLL. Connect this signal in your design to power up or reset the PLL. Assert the RSTN pin for a minimum pulse of 10 ns to reset the PLL. Assert RSTN when dynamically changing the selected PLL reference clock.
COREFBK	Input	Connect to a clock out interface pin when the the PLL feedback mode is set to core.
CLKOUT0 CLKOUT1 CLKOUT2	Output	PLL output. The designer can route these signals as input clocks to the core's GCLK network.
LOCKED	Output	Goes high when PLL achieves lock; goes low when a loss of lock is detected. Connect this signal in your design to monitor the lock status.

Table 13: PLL Interface Designer Settings - Properties Tab

Parameter	Choices	Notes
Instance Name	User defined	
PLL Resource		The resource listing depends on the FPGA you choose.
Clock Source	External	PLL reference clock comes from an external pin.
	Dynamic	PLL reference clock comes from an external pin or the core, and is controlled by the clock select bus.
	Core	PLL reference clock comes from the core.
Automated Clock Calculation		Pressing this button launches the PLL Clock Caclulation window. The calculator helps you define PLL settings in an easy-to-use graphical interface.

Table 14: PLL Interface Designer Settings - Manual Configuration Tab

Parameter	Choices	Notes
Reset Pin Name	User defined	
Locked Pin Name	User defined	

Parameter	Choices	Notes
Feedback Mode	Internal	PLL feedback is internal to the PLL resulting in no known phase relationship between clock in and clock out.
	Local	PLL feedback is local to the PLL. Aligns the clock out phase with clock in.
	Core	PLL feedback is from the core. The feedback clock is defined by the COREFBK connection, and must be one of the three PLL output clocks. Aligns the clock out phase with clock in and removes the core clock delay.
Reference clock Frequency (MHz)	User defined	
Multiplier (M)	1 - 255 (integer)	M counter.
Pre Divider (N)	1 - 15 (integer)	N counter.
Post Divider (O)	1, 2, 4, 8	O counter.
Clock 0, Clock 1, Clock 2	On, off	Use these checkboxes to enable or disable clock 0, 1, and 2.
Pin Name	User defined	Specify the pin name for clock 0, 1, or 2.
Divider (C)	1 to 256	Output divider.
Phase Shift (Degree)	0, 45, 90, 135, 180, or 270	Phase shift CLKOUT by 0, 45, 90, 135, 180, or 270 degrees. 90, 180, and 270 require the C divider to be 2. 45 and 135 require the C divider to be 4. To phase shift 225 degrees, select 45 and invert the clock at the destination. To phase shift 315 degrees, select 135 and invert the clock at the destination.
Use as Feedback	On, off	

Table 15: PLL Reference Clock Resource Assignments (QFP144)

PLL	REFCLK1	REFCLK2
BR_PLL	Differential: GPIOB_CLKP0, GPIOB_CLKN0 Single Ended: GPIOB_CLKP0	GPIOR_157_PLLIN
TR_PLL0	GPIOR_76_PLLIN0	GPIOR_77_PLLIN1
TR_PLL1	GPIOR_76_PLLIN0	GPIOR_77_PLLIN1
TL_PLL0	GPIOL_74_PLLIN0	GPIOL_75_PLLIN1
TL_PLL1	GPIOL_74_PLLIN0	GPIOL_75_PLLIN1

LVDS

T8 FPGAs in QFP144 packages have an LVDS interface.

The LVDS hard IP transmitters and receivers operate independently.

- LVDS TX consists of LVDS transmitter and serializer logic.
- LVDS RX consists of LVDS receiver, on-die termination, and de-serializer logic.

The T8 has one PLL for use with the LVDS receiver.

Note: You can use the LVDS TX and LVDS RX channels as 3.3 V single-ended GPIO pins, which support a weak pull-up but do not support a Schmitt trigger or variable drive strength. When using LVDS as GPIO, make sure to leave at least 2 pairs of unassigned LVDS pins between any GPIO and LVDS pins in the same bank. This separation reduces noise. The Efinity software issues an error if you do not leave this separation.

The LVDS hard IP has these features:

- Dedicated LVDS TX and RX channels (the number of channels is package dependent), and one dedicated LVDS RX clock
- Up to 600 Mbps for LVDS data transmit or receive
- Supported serialization and deserialization factors: 8:1, 7:1, 6:1, 5:1, 4:1, 3:1, and 2:1
- 1:1 mode to bypass the serializer or deserializer
- Source synchronous clock output edge-aligned with data for LVDS transmitter and receiver
- 100 Ω on-die termination resistor for the LVDS receiver

LVDS TX

Figure 14: LVDS TX Interface Block Diagram

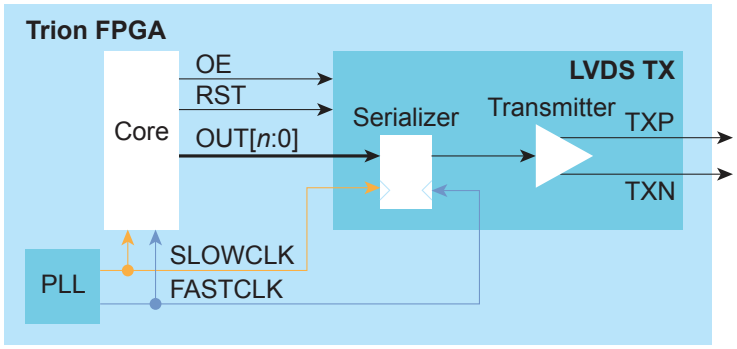


Table 16: LVDS TX Signals (Interface to FPGA Fabric)

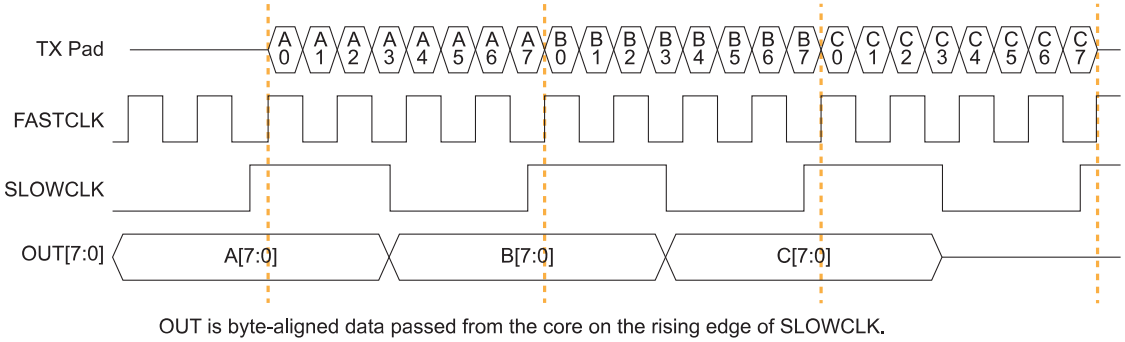
Signal	Direction	Notes
OUT[*n*-1:0]	Input	Parallel output data where *n* is the serialization factor. A width of 1 bypasses the serializer.
OE	Input	LVDS output enable, available in simple buffer (x1) mode. Unused by default.
FASTCLK	Input	Fast clock to serialize the data to the LVDS pads.
SLOWCLK	Input	Slow clock to latch the incoming data from the core.
RST	Input	Reset the serializer. Unused by default.

Table 17: LVDS TX Pads

Pad	Direction	Description
TXP	Output	Differential P pad.
TXN	Output	Differential N pad.

The following waveform shows the relationship between the fast clock, slow clock, TX data going to the pad, and byte-aligned data from the core.

Figure 15: LVDS Timing Example Serialization Width of 8



OUT is byte-aligned data passed from the core on the rising edge of SLOWCLK.

Table 18: LVDS TX Settings in Efinity® Interface Designer

Parameters	Choices	Notes
Mode	**serial data output** or **reference clock output**	**serial data output**—Simple output buffer or serialized output. **reference clock output**—Use the transmitter as a clock output.
Serialization Width	1, 2, 3, 4, 5, 6, 7, or 8	In x1 mode the serializer is bypassed and the LVDS buffer is used as a normal output.
Reduce VOD Swing	True or False	When true, enables reduced output swing (similar to slow slew rate).
Output Load	5, 7 (default), or 10	Output load in pF. Use an output load of 7 pF or higher to achieve the maximum throughput of 600 Mbps.

LVDS RX

Figure 16: LVDS RX Interface Block Diagram

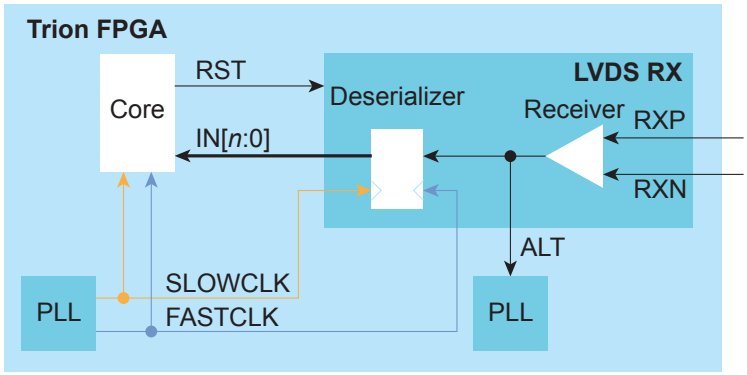


Table 19: LVDS RX Signals (Interface to FPGA Fabric)

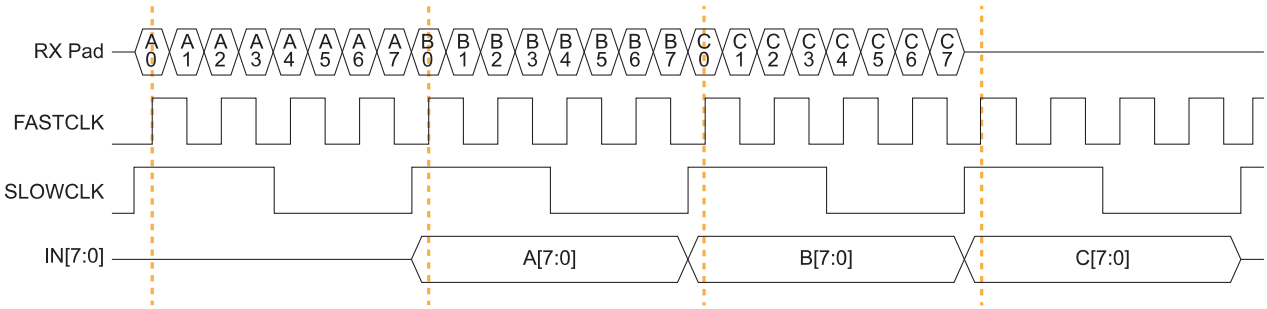
Signal	Direction	Notes
IN[*n*-1:0]	Output	Parallel input data where *n* is the de-serialization factor. A width of 1 bypasses the deserializer.
ALT	Output	Alternative input, only available for an LVDS RX resource in bypass mode (deserialization width is 1; alternate connection type). Alternative connections are PLLCLK and PLLFBK.
FASTCLK	Input	Fast clock to de-serialize the data from the LVDS pads.
SLOWCLK	Input	Slow clock to latch the incoming data to the core.
RST	Input	Reset the de-serializer. Unused by default.

Table 20: LVDS RX Pads

Pad	Direction	Description
RXP	Input	Differential P pad.
RXN	Input	Differential N pad.

The following waveform shows the relationship between the fast clock, slow clock, RX data coming in from the pad, and byte-aligned data to the core.

Figure 17: LVDS RX Timing Example Serialization Width of 8



IN is byte-aligned data passed to the core on the rising edge of SLOWCLK.

Table 21: LVDS RX Settings in Efinity® Interface Designer

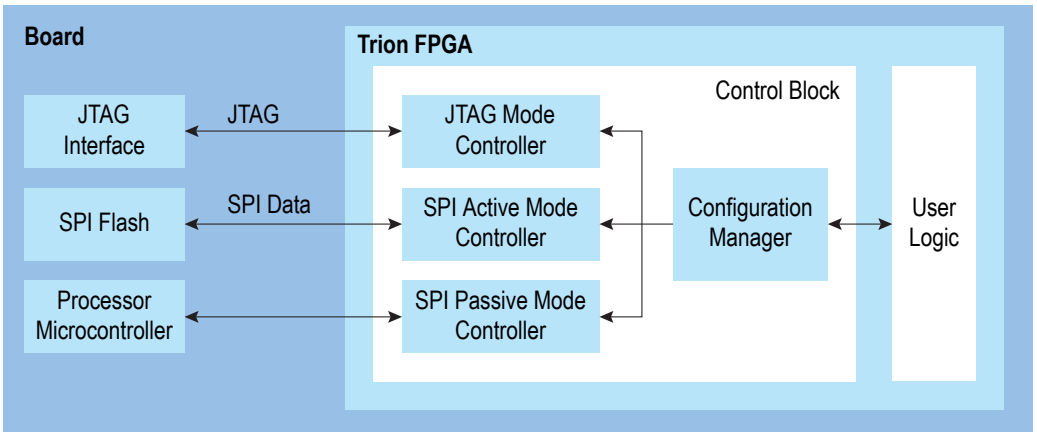
Parameter	Choices	Notes
Connection Type	**normal** or **alternate**	**alternate**—Use the alternate function of the LVDS RX resource (such as a PLL reference clock). Also choose de-serialization width of 1. **normal**—Regular RX function.
Deserialization	1, 2, 3, 4, 5, 6, 7, or 8	In x1 mode the de-serializer is bypassed and the LVDS buffer is used as a normal input.
Enable On-Die Termination	True or False	When true, enables an on-die 100-ohm resistor.

Configuration

The T8 FPGA contains volatile Configuration RAM (CRAM). The user must configure the CRAM for the desired logic function upon power-up and before the FPGA enters normal operation. The FPGA's control block manages the configuration process and uses a bitstream to program the CRAM. The Efinity® software generates the bitstream, which is design dependent. You can configure the T8 FPGA(s) in active, passive, or JTAG mode.

Learn more: Refer to AN 006: Configuring Trion FPGAs for details on the dedicated configuration pins and how to configure FPGA(s).

Figure 18: High-Level Configuration Options



In active mode, the FPGA controls the configuration process. An oscillator circuit within the FPGA provides the configuration clock. The bitstream is typically stored in an external serial flash device, which provides the bitstream when the FPGA requests it.

The control block sends out the instruction and address to read the configuration data. First, it issues a release from power-down instruction to wake up the external SPI flash. Then, it waits for at least 30 μs before issuing a fast read command to read the content of SPI flash from address 24h'000000.

In passive mode, the FPGA is the slave and relies on an external master to provide the control, bitstream, and clock for configuration. Typically the master is a microcontroller or another FPGA in active mode.

In JTAG mode, you configure the FPGA via the JTAG interface.

Supported Configuration Modes

Table 22: T8 Configuration Modes by Package

Configuration Mode	Width	BGA49	BGA81	QFP144
Active	X1	✓	✓	✓
	X2	✓	✓	✓
	X4	✓	✓	✓
Passive	X1	✓	✓	✓
	X2	✓	✓	✓
	X4	✓	✓	✓
	X8	✓	✓	✓
JTAG	X1		✓	✓

Mask-Programmable Memory Option

The T8 FPGA is equipped with one-time programmable MPM. With this feature, you use on-chip MPM instead of an external serial flash device to configure the FPGA. This option is for systems that require an ultra-small factor and the lowest cost structure such that an external serial flash device is undesirable and/or not required at volume production. MPM is a one-time factory programmable option that requires a Non-Recurring Engineering (NRE) payment. To enable MPM, submit your design to our factory; our Applications Engineers (AEs) convert your design into a single configuration mask to be specially fabricated.

DC and Switching Characteristics (BGA49 and BGA81)

T8 FPGAs in BGA49 and BGA81 packages have the following DC and switching characteristics.

Table 23: Absolute Maximum Ratings [9]

Conditions beyond those listed may cause permanent damage to the device. Device operation at the absolute maximum ratings for extended periods of time has adverse effects on the device.

Symbol	Description	Min	Max	Units
VCC	Core power supply	-0.5	1.42	V
VCCIO	I/O bank power supply	-0.5	4.6	V
VCCA_PLL	PLL analog power supply	-0.5	1.42	V
T_J	Operating junction temperature	-40	125	°C

Table 24: Recommended Operating Conditions [9]

Symbol	Description	Min	Typ	Max	Units
VCC	Core power supply	1.05	1.1	1.15	V
VCCIO	1.8 V I/O bank power supply	1.71	1.8	1.89	V
	2.5 V I/O bank power supply	2.38	2.5	2.63	V
	3.3 V I/O bank power supply	3.14	3.3	3.47	V
VCCA_PLL	PLL analog power supply	1.05	1.1	1.15	V
T_{JCOM}	Operating junction temperature, commercial	0	–	85	°C

Table 25: Power Supply Ramp Rates

Symbol	Description	Min	Max	Units
t_{RAMP}	Power supply ramp rate for all supplies.	0.01	10	V/ms

Table 26: Static Supply Current

Symbol	Parameter	Typ	Units
I_{CC}	Typical standby (Low Power [LP] option)[10]	150	µA
I_{CC}	Typical standby	500	µA

[9] Supply voltage specification applied to the voltage taken at the device pins with respect to ground, not at the power supply.
[10] This specification is for the commercial grade -1 speed grade device only.

Table 27: Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2	VCCIO + 0.3	0.2	VCCIO - 0.2
3.3 V LVTTL	-0.3	0.8	2	VCCIO + 0.3	0.4	2.4
2.5 V LVCMOS	-0.3	0.7	1.7	VCCIO + 0.3	0.5	1.8
1.8 V LVCMOS	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO + 0.3	0.45	VCCIO - 0.45

Table 28: Single-Ended I/O DC Electrical Characteristics

Voltage	VT+ (V) Schmitt Trigger Low-to-High Threshold	VT- (V) Schmitt Trigger High-to-Low Threshold	Input Leakage Current (µA)	Tristate Output Leakage Current (µA)
3.3	1.73	1.32	±10	±10
2.5	1.37	1.01	±10	±10
1.8	1.05	0.71	±10	±10

Table 29: Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at T_J = 25 °C, power supply at nominal voltage, device in nominal process (TT).

I/O Standard	3.3 V		2.5 V		1.8 V	
Drive Strength	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)
1	14.4	8.0	9.1	8.0	4.4	5.1
2	19.1	10.5	12.2	10.5	5.8	6.8
3	23.9	13.3	15.2	13.4	7.3	8.6
4	28.7	15.8	18.2	15.9	8.6	10.3

DC and Switching Characteristics (QFP144)

T8 FPGAs in QFP144 packages have the following DC and switching characteristics.

Table 30: Absolute Maximum Ratings

Conditions beyond those listed may cause permanent damage to the device. Device operation at the absolute maximum ratings for extended periods of time has adverse effects on the device.

Symbol	Description	Min	Max	Units
VCC	Core power supply	-0.5	1.42	V
VCCIO	I/O bank power supply	-0.5	4.6	V
VCCA_PLL	PLL analog power supply	-0.5	1.42	V
T_J	Operating junction temperature	-40	125	°C

Table 31: Recommended Operating Conditions [11]

Symbol	Description	Min	Typ	Max	Units
VCC	Core power supply	1.15	1.2	1.25	V
VCCIO	1.8 V I/O bank power supply	1.71	1.8	1.89	V
	2.5 V I/O bank power supply	2.38	2.5	2.63	V
	3.3 V I/O bank power supply	3.14	3.3	3.47	V
VCCA_PLL	PLL analog power supply	1.15	1.2	1.25	V
T_{JCOM}	Operating junction temperature, commercial	0	–	85	°C
T_{JIND}	Operating junction temperature, industrial	-40	–	100	°C

Table 32: Power Supply Ramp Rates

Symbol	Description	Min	Max	Units
t_{RAMP}	Power supply ramp rate for all supplies.	0.01	10	V/ms

Table 33: Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2	VCCIO + 0.3	0.2	VCCIO - 0.2
3.3 V LVTTL	-0.3	0.8	2	VCCIO + 0.3	0.4	2.4
2.5 V LVCMOS	-0.3	0.7	1.7	VCCIO + 0.3	0.5	1.8
1.8 V LVCMOS	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO + 0.3	0.45	VCCIO - 0.45

[11] Supply voltage specification applied to the voltage taken at the device pins with respect to ground, not at the power supply.

Table 34: Single-Ended I/O DC Electrical Characteristics

Voltage (V)	VT+ (V) Schmitt Trigger Low-to-High Threshold	VT- (V) Schmitt Trigger High-to-Low Threshold	Input Leakage Current (µA)	Tristate Output Leakage Current (µA)
3.3	1.73	1.32	±10	±10
2.5	1.37	1.01	±10	±10
1.8	1.05	0.71	±10	±10

Table 35: Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at T_J = 25 °C, power supply at nominal voltage.

I/O Standard	3.3 V		2.5 V		1.8 V	
Drive Strength	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)
1	14.4	8.0	9.1	8.0	4.4	5.1
2	19.1	10.5	12.2	10.5	5.8	6.8
3	23.9	13.3	15.2	13.4	7.3	8.6
4	28.7	15.8	18.2	15.9	8.6	10.3

Table 36: LVDS Pins Configured as Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2	VCCIO + 0.3	0.2	VCCIO - 0.2
3.3 V LVTTL	-0.3	0.8	2	VCCIO + 0.3	0.4	2.4

Table 37: LVDS Pins Configured as Single-Ended I/O DC Electrical Characteristics

Voltage (V)	Input Leakage Current (µA)	Tri-State Output Leakage Current (µA)
3.3	±10	±10

Table 38: LVDS Pins as Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at T_J = 25 °C, power supply at nominal voltage, device in nominal process (TT).

I/O Standard	Drive Strength	
	I_{OH} (mA)	I_{OL} (mA)
3.3 V	37.6	22

LVDS I/O Electrical Specifications (QFP144)

The LVDS pins comply with the EIA/TIA electrical specifications.

Important: All specifications are preliminary and pending hardware characterization.

Table 39: LVDS I/O Electrical Specifications

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{CCIO}	LVDS I/O Supply Voltage	–	2.97	3.3	3.63	V
LVDS TX						
V_{OD}	Output Differential Voltage	–	250	–	450	mV
ΔV_{OD}	Change in V_{OD}	–	–	–	50	mV
V_{OCM}	Output Common Mode Voltage	RT = 100 Ω	1,125	1,250	1,375	mV
ΔV_{OCM}	Change in V_{OCM}	–	–	–	50	mV
V_{OH}	Output High Voltage	RT = 100 Ω	–	–	1475	mV
V_{OL}	Output Low Voltage	RT = 100 Ω	925	–	–	mV
I_{SAB}	Output Short Circuit Current	–	–	–	24	mA
LVDS RX[12]						
V_{ID}	Input Differential Voltage	–	100	–	600	mV
V_{ICM}	Input Common Mode Voltage	–	100	–	2,000	mV
V_{TH}	Differential Input Threshold	–	-100	–	100	mV
I_{IL}	Input Leakage Current	–	–	–	20	µA

ESD Performance

Refer to the Trion Reliability Report for ESD performance data.

[12] The LVDS RX supports the sub-lvds, slvs, HiVcm, RSDS and 3.3 V LVPECL differential I/O standard.

Timing Specifications

Configuration Timing

The T8 FPGA has the following configuration timing specifications. Refer to AN 006: Configuring Trion FPGAs for detailed configuration information.

Timing Waveforms

Figure 19: SPI Active Mode (x1) Timing Sequence

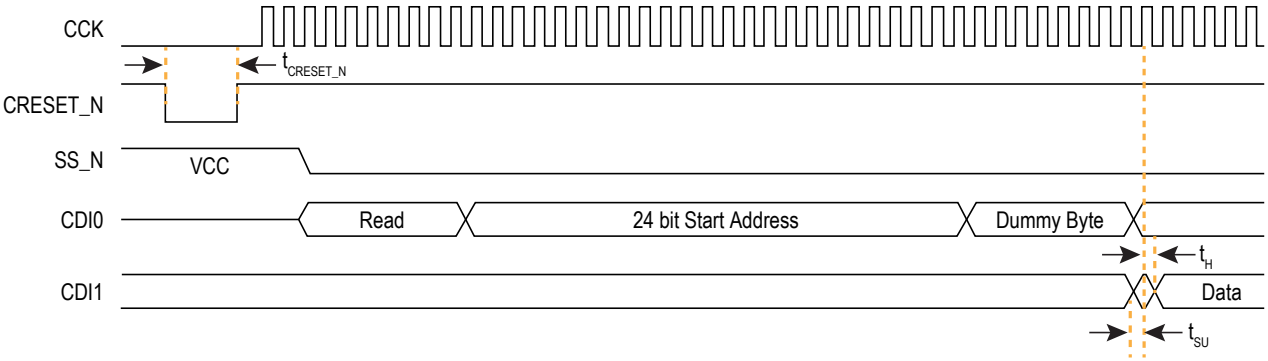


Figure 20: SPI Passive Mode (x1) Timing Sequence

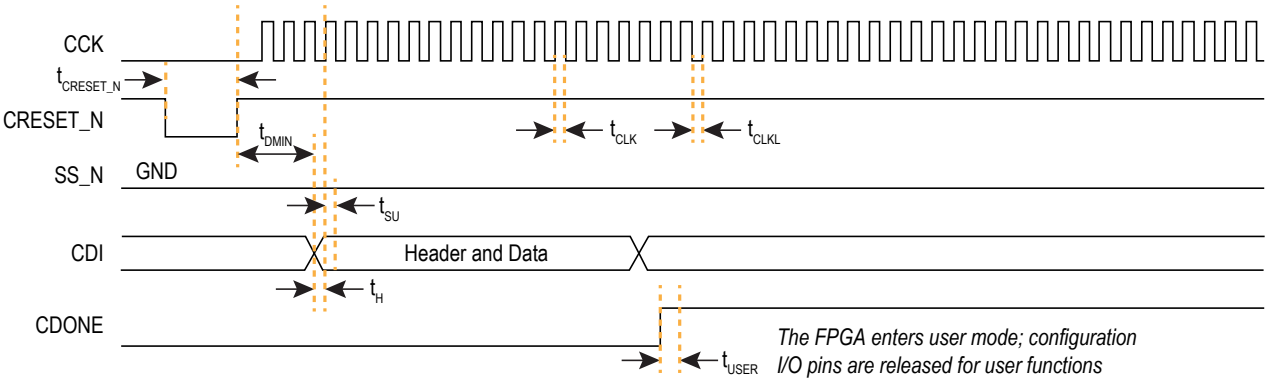
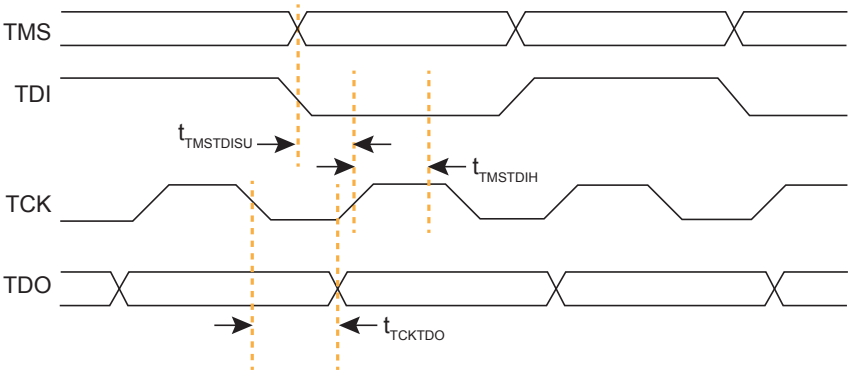


Figure 21: Boundary Scan Timing Waveform



Timing Parameters

Table 40: All Modes

Symbol	Parameter	Min	Typ	Max	Units
t_{CRESET_N}	Minimum creset_n low pulse width required to trigger re-configuration.	320	–	–	ns
t_{USER}	Minimum configuration duration after CDONE goes high before entering user mode.[13]	8	–	–	µs

Table 41: Active Mode

Symbol	Parameter	Frequency	Min	Typ	Max	Units
f_{MAX_M}	Active mode configuration clock frequency.	DIV4	14	20	26	MHz
		DIV8	7	10	13	MHz
t_{SU} [14]	Setup time.	–	7.5	–	–	ns
t_H [14]	Hold time.	–	1	–	–	ns

Table 42: Passive Mode

Symbol	Parameter	Min	Typ	Max	Units
f_{MAX_S}	Passive mode configuration clock frequency.	–	–	100	MHz
t_{CLKH}	Configuration clock pulse width high.	4.8	–	–	ns
t_{CLKL}	Configuration clock pulse width low.	4.8	–	–	ns
t_{SU}	Setup time. (BGA49 and BGA81)	4	–	–	ns
t_{SU}	Setup time. (QFP144 packages)	6	–	–	ns
t_H	Hold time.	1	–	–	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to first valid configuration data.	1.2	–	–	µs

Table 43: JTAG Mode

Symbol	Parameter	Min	Typ	Max	Units
f_{TCK}	TCK frequency.	–	–	33	MHz
t_{TDISU}	TDI setup time.	3.5	–	–	ns
t_{TDIH}	TDI hold time.	1			ns
t_{TMSSU}	TMS setup time.	3			ns
t_{TMSH}	TMS hold time.	1			ns
t_{TCKTDO}	TCK falling edge to TDO output.	–	–	10.5[15]	ns

[13] The FPGA may go into user mode before t_{USER} has elapsed. However, Efinix recommends that you keep the system interface to the FPGA in reset until t_{USER} has elapsed.
[14] Test condition at 3.3 V I/O standard and 0 pF output loading.
[15] 0 pf output loading.

PLL Timing and AC Characteristics (BGA49 and BGA81)

The following tables describe the PLL timing and AC characteristics for the simple PLL in BGA49 and BGA81 packages.

Table 44: PLL Timing

Symbol	Parameter	Min	Typ	Max	Units
F_{PFD}	Phase frequency detector input frequency.	10	–	50	MHz
F_{OUT}	Output clock frequency.	0.25 (16)	–	400 (16)	MHz
F_{VCO}	PLL VCO frequency.	500 (16)	–	1500 (16)	MHz

Table 45: PLL AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{DT}	Output clock duty cycle.	45 (16)	50	55 (16)	%
t_{OPJIT} (PK - PK)	Output clock period jitter (PK-PK).	–	100 (16)	–	ps
t_{LOCK}	PLL pull in plus lock-in time.	–	–	0.5	ms

PLL Timing and AC Characteristics (QFP144)

The following tables describe the PLL timing and AC characteristics for the advanced PLL in QFP144 packages.

Table 46: PLL Timing

Symbol	Parameter	Min	Typ	Max	Units
F_{IN}	Input clock frequency.	10	–	200	MHz
F_{OUT}	Output clock frequency.	0.24	–	500	MHz
F_{VCO}	PLL VCO frequency.	500	–	1,500	MHz
F_{PFD}	Phase frequency detector input frequency.	10	–	50	MHz

Table 47: PLL AC Characteristics[17]

Symbol	Parameter	Min	Typ	Max	Units
t_{DT}	Output clock duty cycle.	45	50	55	%
t_{OPJIT} (PK - PK) (18)	Output clock period jitter (PK-PK).			200	ps
t_{LOCK}	PLL lock-in time.	–	–	0.5	ms

(16) Pending hardware characterization.
(17) Test conditions at 3.3 V and room temperature.
(18) The output jitter specification applies to the PLL jitter when an input jitter of 20 ps is applied.

Internal Oscillator (BGA49 and BGA81)

The internal oscillator has the following specifications.

Table 48: Internal Oscillator Specifications

Symbol	Parameter	Min	Typ	Max	Units
F_{CLKOSC}	Oscillator clock frequency.	–	10	–	kHz
D_{CHOSC}	Duty cycle.	45	50	55	%

Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

Table 49: General Pinouts

Function	Group	Direction	Description
VCC	Power	–	Core power supply.
VCCIO	Power	–	I/O pin power supply.
VCCA_PLL	Power	–	PLL analog power supply.
VCCA_*xx*	Power	–	PLL analog power supply. *xx* indicates location: TL: Top left, TR: Top right, BR: bottom right
VCCIO*xx*	Power	–	I/O pin power supply. *xx* indicates the bank location: 1A: Bank 1A, 3E: Bank 3E 4A: Bank 4A (only for 3.3 V) , 4B: Bank 4B (only for 3.3 V)
VCCIO*xx_yy_zz*	Power	–	Power for I/O banks that are shorted together. *xx*, *yy*, and *zz* are the bank locations. For example: VCCIO1B_1C shorts banks 1B and 1C VCCIO3C_TR_BR shorts banks 3C, TR, and BR
GND	Ground	–	Ground.
GNDA_PLL	Ground	–	PLL ground pin.
CLK*n*	Alternate	Input	Global clock network input. *n* is the number. The number of inputs is package dependent.
CTRL*n*	Alternate	Input	Global network input used for high fanout and global reset. *n* is the number. The number of inputs is package dependent.
PLLIN	Alternate	Input	PLL reference clock resource. There are 5 PLL reference clock resource assignments (depending on the package). Assign the reference clock resource based on the PLL you are using.
GPIO*x_n*	GPIO	I/O	General-purpose I/O for user function. User I/O pins are single ended. *x*: Indicates the bank (L or R) *n*: Indicates the GPIO number.
GPIO*x_n_yyy* GPIO*x_n_yyy_zzz* GPIO*x_zzzn*	GPIO Multi-Function	I/O	Multi-function, general-purpose I/O. These pins are single ended. If these pins are not used for their alternate function, you can use them as user I/O pins. *x*: Indicates the bank; left (L), right (R), or bottom (B). *n*: Indicates the GPIO number. *yyy, yyy_zzz*: Indicates the alternate function. *zzzn*: Indicates LVDS TX or RX and number.
TXN*n*, TXP*n*	LVDS	I/O	LVDS transmitter (TX). *n*: Indicates the number.
RXN*n*, RXP*n*	LVDS	I/O	LVDS receiver (RX). *n*: Indicates the number.
CLKN*n*, CLKP*n*	LVDS	I/O	Dedicated LVDS receiver clock input. *n*: Indicates the number.
RXN*n*_EXTFB*n* RXP*n*_EXTFB*n*	LVDS	I/O	LVDS PLL external feedback. *n*: Indicates the number.
REF_RES	–	–	LVDS reference resistor pin. Connect a 12 kΩ resistor with a tolerance of ±1% to the REF_RES pin with respect to ground.

Table 50: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

Pins	Direction	Description	Use External Weak Pull-Up
CDONE	Output	Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, configuration is complete. If you hold CDONE low, the device will not enter user mode. CDONE is an open-drain output.	✓
CRESET_N	Input	Configuration reset pin (active low). Pulse CRESET_N low for t_{creset} time to reset the FPGA.	✓
TCK	Input	JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.	✓
TMS	Input	JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation . The signal value typically changes on the falling edge of TCK. TMS is typically a weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1.	✓
TDI	Input	JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI is typically a weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1.	✓
TDO	Output	JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or from a test data register depending on the sequence previously applied at TMS. During shifting, data applied at TDI appears at TDO after a number of cycles of TCK determined by the length of the register included in the serial path. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance).	✓

Table 51: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.

Pins	Direction	Description	Use External Weak Pull-Up
CBUS[2:0]	Input	Configuration bus width select. Connect to weak pull-up resistors if using default mode (x1).	✓
CBSEL[1:0]	Input	Optional multi-image selection input (if multi-image configuration mode is enabled).	N/A
CCK	I/O	Passive SPI input configuration clock or active SPI output configuration clock (active low). Includes an internal weak pull-up.	N/A
CDI*n*	I/O	*n* is a number from 0 to 31 depending on the SPI configuration. 0: Passive serial data input or active serial output. 1: Passive serial data output or active serial input. *n*: Parallel I/O.	N/A
CSI	Input	Chip select. 0: The FPGA is not selected or enabled and will not be configured. 1: Selects the FPGA for configuration.	✓

Pins	Direction	Description	Use External Weak Pull-Up
CSO	Output	Chip select output. Selects the next device for cascading configuration.	N/A
NSTATUS	Output	Status (active low). Indicates a configuration error. This pin is active when there is a synchronization pattern mismatch or not found. When the FPGA drives this pin low, it indicates an ID mismatch, the bitstream CRC check has failed, or remote update has failed.	N/A
SS_N	Input	SPI slave select (active low). Includes an internal weak pull-up resistor to VCCIO during configuration. During configuration, the logic level samples on this pin determine the configuration mode. This pin is an input when sampled at the start of configuration (SS is low); an output in active SPI flash configuration mode. The FPGA senses the value of `SS_N` when it comes out of reset (pulse `CRESET_N` low to high). 0: Passive mode 1: Active mode	✓
TEST_N	Input	Active-low test mode enable signal. Set to 1 to disable test mode. During configuration, rely on the external weak pull-up or drive this pin high.	✓
RESERVED_OUT	Output	Reserved pin during user configuration. This pin drives high during user configuration. BGA49 and BGA81 packages only.	N/A

Efinity Software Support

The Efinity® software provides a complete tool flow from RTL design to bitstream generation, including synthesis, place-and-route, and timing analysis. The software has a graphical user interface (GUI) that provides a visual way to set up projects, run the tool flow, and view results. The software also has a command-line flow and Tcl command console. The software-generated bitstream file configures the T8 FPGA. The software supports the Verilog HDL and VHDL languages.

T8 Interface Floorplan

Note: The numbers in the floorplan figures indicate the GPIO and LVDS number ranges. Some packages may not have all GPIO or LVDS pins in the range bonded out. Refer to the T8 pinout for information on which pins are available in each package.

Figure 22: Floorplan Diagram for BGA49 and BGA81 Packages

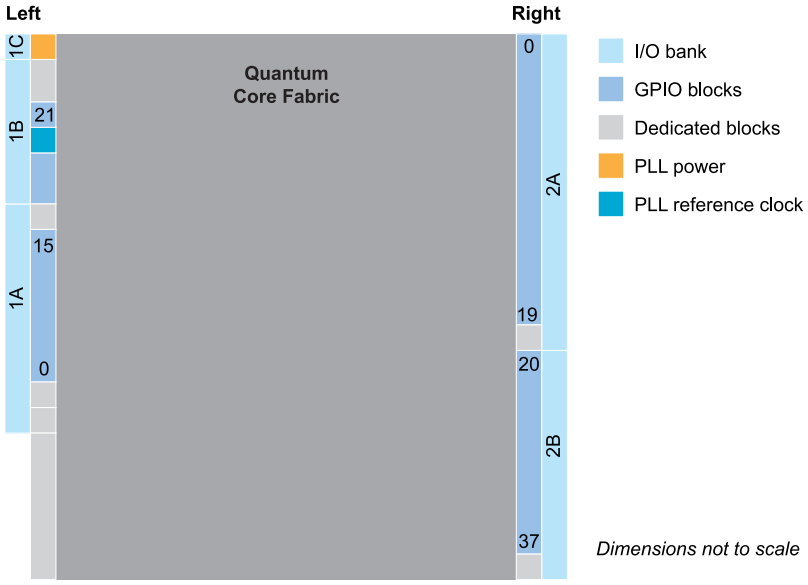
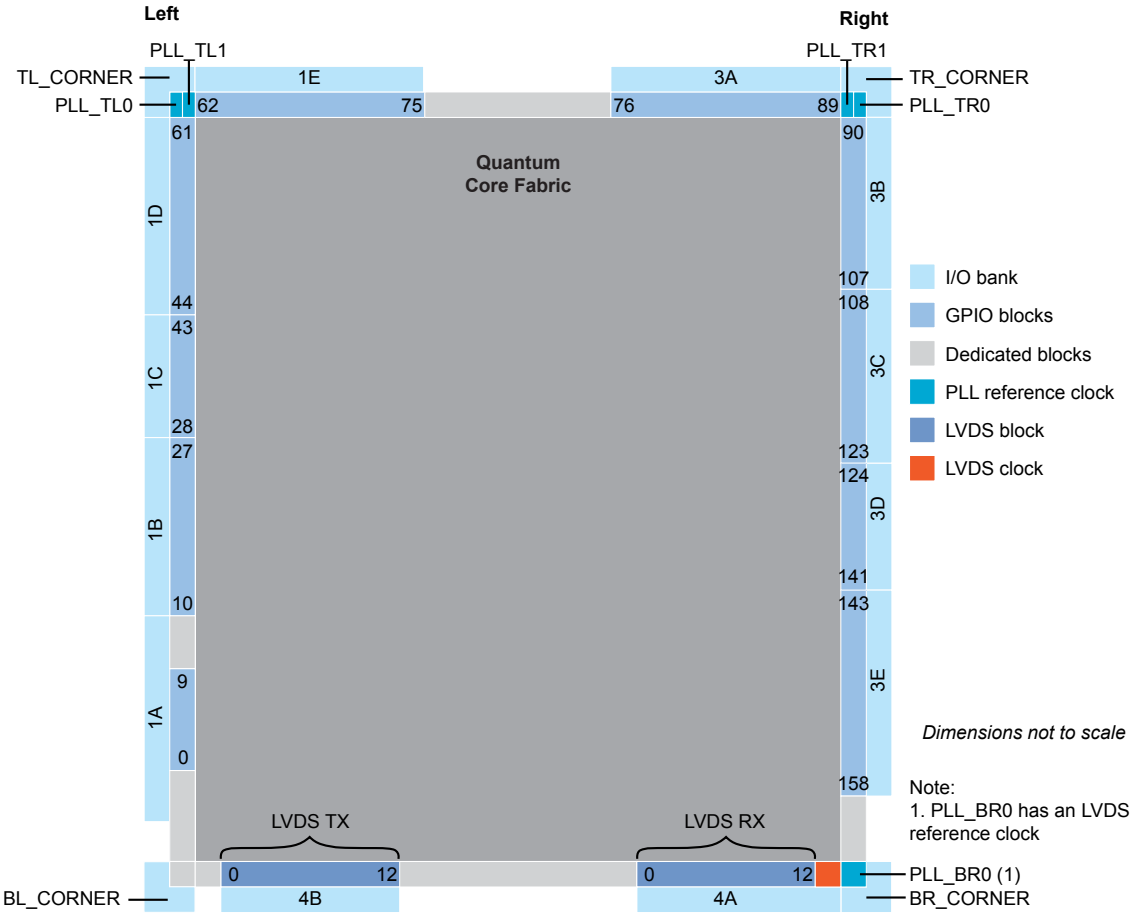


Figure 23: Floorplan Diagram for QFP144 Packages



Ordering Codes

Refer to the Trion Selector Guide for the full listing of T8 ordering codes.

Revision History

Table 52: Revision History

Date	Version	Description
December 2019	2.4	Updated PLL settings in the Interface Designer. Removed DIV1 and DIV2 active mode configuration frequencies; they are not supported. Added note to LVDS electrical specifications about RX differential I/O standard support.
October 2019	2.3	Added explanation that 2 unassigned pairs of LVDS pins should be located between and GPIO and LVDS pins in the same bank. Updated the reference clock pin assignments for TL_PLL0 and TL_PLL1. Added waveforms for configuration timing. Clarified I/O bank information.
September 2019	2.2	Minor clarifications.
August 2019	2.1	Updated formatting for I/O bank information.
August 2019	2.0	Added information about T8 FPGAs in 144-pin QFP packages.
February 2019	1.7	Removed incorrect footnote about LVDS under Available Package Options.
November 2018	1.6	Updated PLL interface description. Added packaging and floorplan information. Updated configuration timing and PLL timing information.
August 2018	1.5	Updated configuration pin table. Renamed RST PLL pin as RSTN.
August 2018	1.4	Updated standby current specifications. Updated ordering codes.
July 2018	1.3	Updated the PLL timing specification to add F_{PFD}. Clarified the slew rate description.
May 2018	1.2	Added ordering code information.
April 2018	1.1	Minor changes throughout.
December 2017	1.0	Initial release.

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