

SuperMOS – TO-252 150V BV_{DSS} , 57m Ω $R_{DS(ON)}$, 19A I_D N-channel MOSFET

1. Description

The ESD2544 is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. Device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product ESD2544 is Pb-free.

2. Features

- 150V, $R_{DS(ON)}=57m\Omega(Tpy)$, $V_{GS}=10V$
- $R_{DS(ON)}=75m\Omega(Tpy)$, $V_{GS}=6V$
- Use trench MOSFET technology
- High density cell design for low $R_{DS(on)}$
- Material : Halogen free
- Reliable and rugged
- Avalanche Rated
- Low leakage current

3. Applications

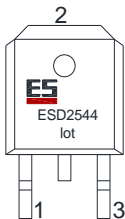
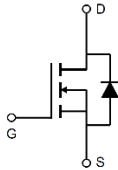
- PWM applications
- Load switch
- Power management in portable/desktop PCs
- DC/DC conversion

100% UIS TESTED!

4. Ordering Information

Part Number	Package	Marking	Material	Packing	Quantity per reel	Flammability Rating	Reel Size
ESD2544	TO-252	ESD2544/lot	Halogen free	Tape & Reel	2,500 PCS	UL 94V-0	13 inches

5. Pin Configuration and Functions

Pin	Function	Outline	Circuit Diagram
1	Gate		
2	Drain		
3	Source		

6. Specification

Absolute Maximum Rating & Thermal Characteristics

Ratings at 25 °C ambient temperature unless otherwise specified.

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	BV_{DSS}	150	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	19
		$T_C=75^\circ\text{C}$	14
Maximum Power Dissipation	P_D	$T_C=25^\circ\text{C}$	62.5
		$T_C=75^\circ\text{C}$	37.5
Pulsed Drain Current ^a	I_{DM}	45	A
Avalanche Current, Single Pulsed ^b	I_{AS}	15.5	A
Avalanche Energy, Single Pulsed ^b	E_{AS}	36	mJ
Operating Junction Temperature	T_J	150	°C
Lead Temperature	T_L	260	°C
Storage Temperature Range	T_{stg}	-55 to 150	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance	$t \leq 10 \text{ s}$	$R_{\theta JA}$		20	°C/W
Junction-to-Case Thermal Resistance ^c	Steady State	$R_{\theta JC}$		2.0	

Note:

a: Repetitive rating, pulse width limited by junction temperature, $t_p=10\mu\text{s}$, Duty Cycle=1%

b: $T_J=25^\circ\text{C}$, $V_{DD}=150\text{V}$, $V_G=10\text{V}$, $L=0.3\text{mH}$, $R_g=25\Omega$

c: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

Electrical Characteristics

At TA = 25°C unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	150			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=150V, V_{GS}=0V$			1	μA
Gate-to-source Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	3.0	5.0	V
Drain-to-source On-resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=5A$		57	69	m Ω
		$V_{GS}=6V, I_D=3A$		75	100	
Forward Trans conductance	g_{FS}	$V_{DS}=5.0V, I_D=5A$	1		40	S
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	$V_{GS}=0V, f=1MHz, V_{DS}=75V$		675		pF
Output Capacitance	C_{OSS}			78		
Reverse Transfer Capacitance	C_{RSS}			4		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS}=10V, V_{DS}=75V, I_D=5A$		11.5	20	nC
Gate-to-Source Charge	Q_{GS}			2		
Gate-to-Drain Charge	Q_{GD}			2.5		
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS}=10V, V_{DS}=75V, R_L=15\Omega, R_G=3\Omega$		6		ns
Rise Time	t_r			3		
Turn-Off Delay Time	$t_{d(OFF)}$			20		
Fall Time	t_f			5		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=1.0A$			1.4	V

7. Typical Characteristic

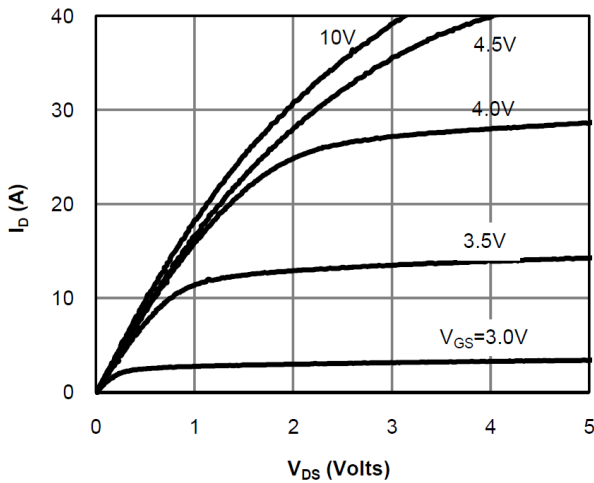


Figure 1: On-Region Characteristics (Note E)

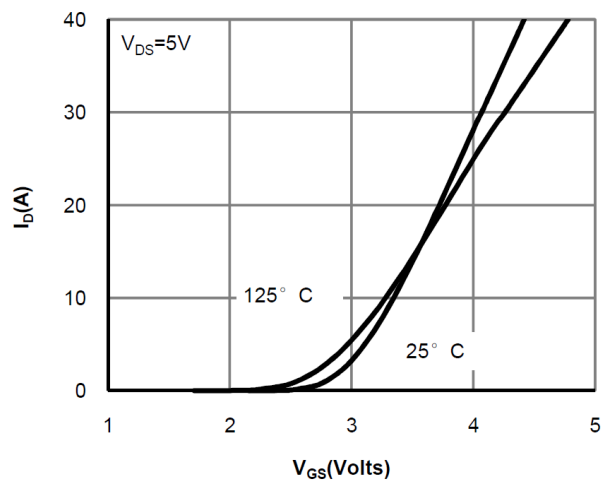


Figure 2: Transfer Characteristics (Note E)

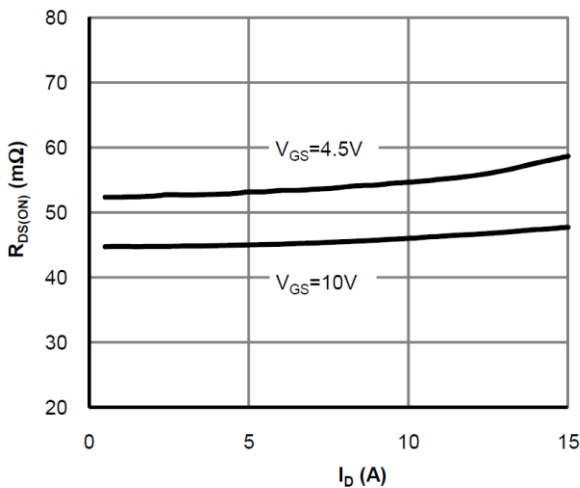


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

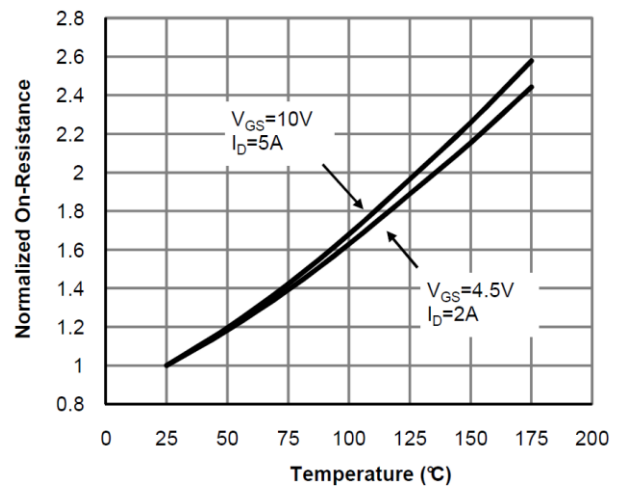


Figure 4: On-Resistance vs. Junction Temperature (Note E)

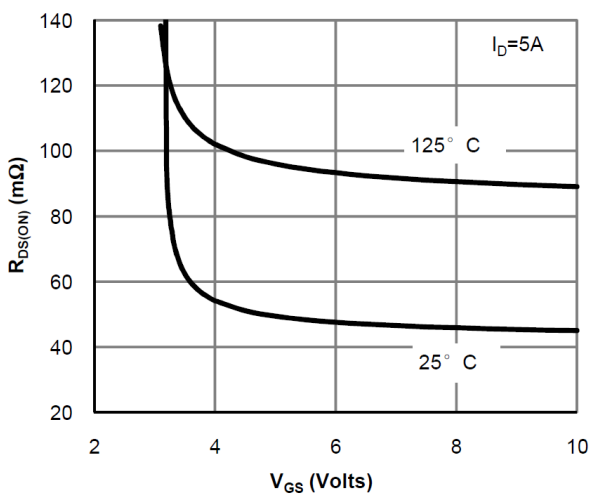


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

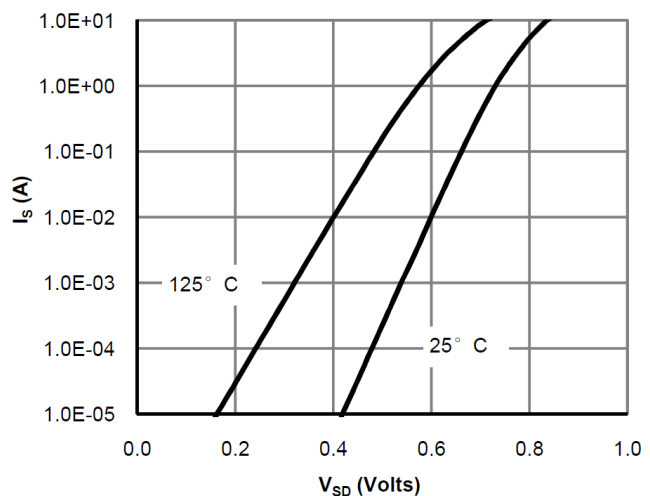


Figure 6: Body-Diode Characteristics (Note E)

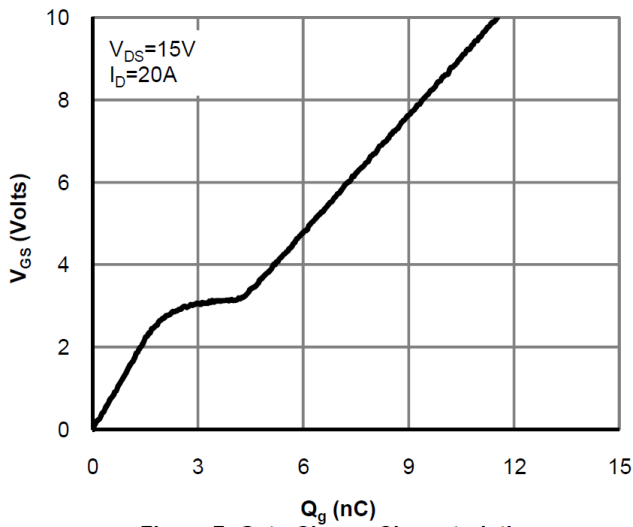


Figure 7: Gate-Charge Characteristics

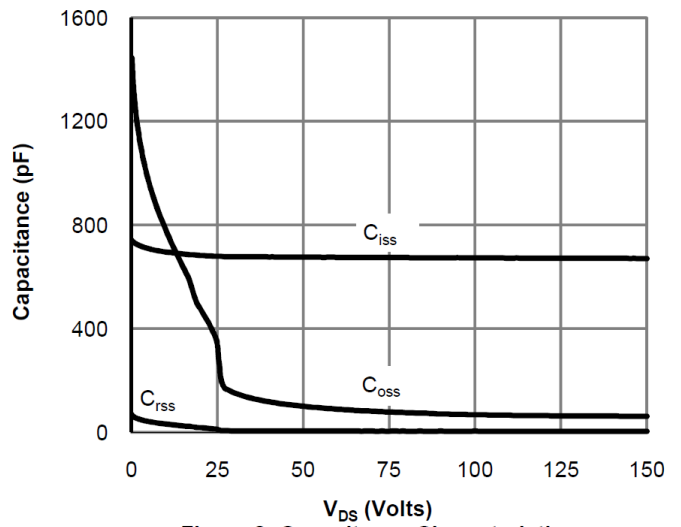


Figure 8: Capacitance Characteristics

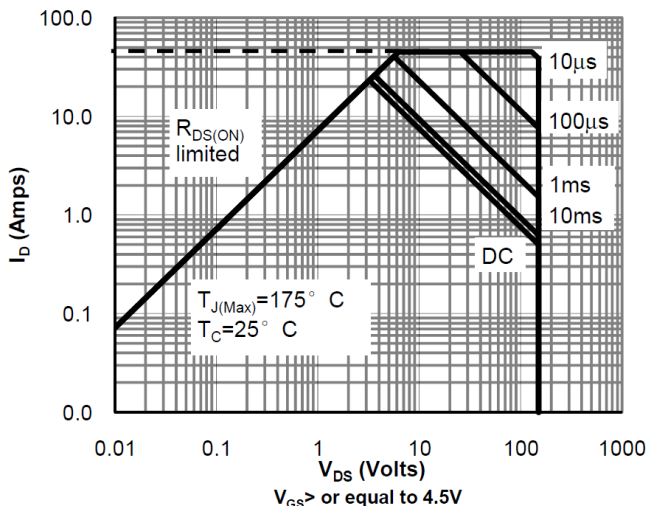


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

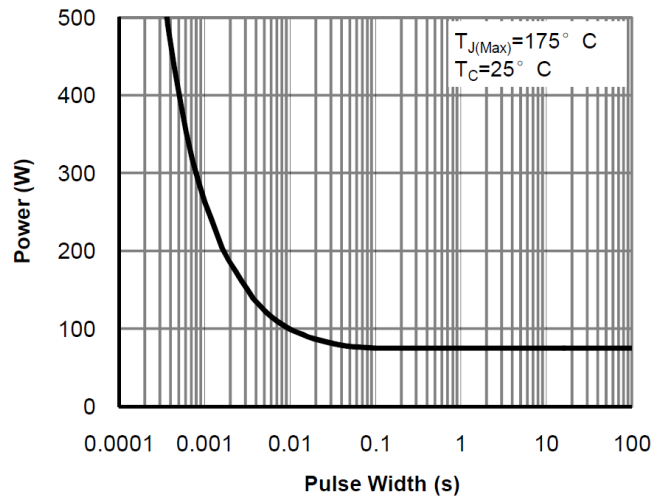


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

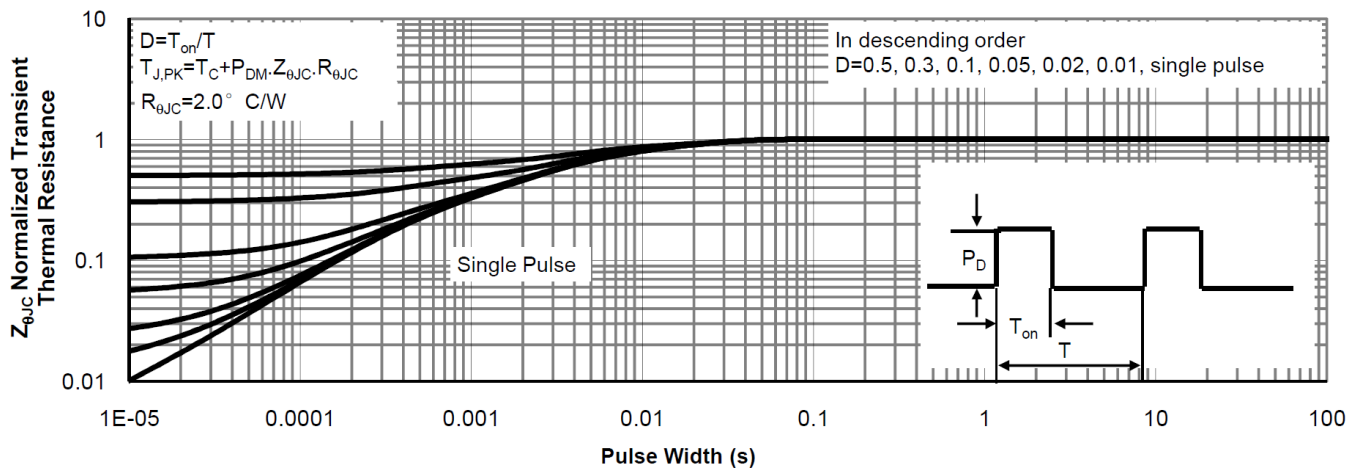
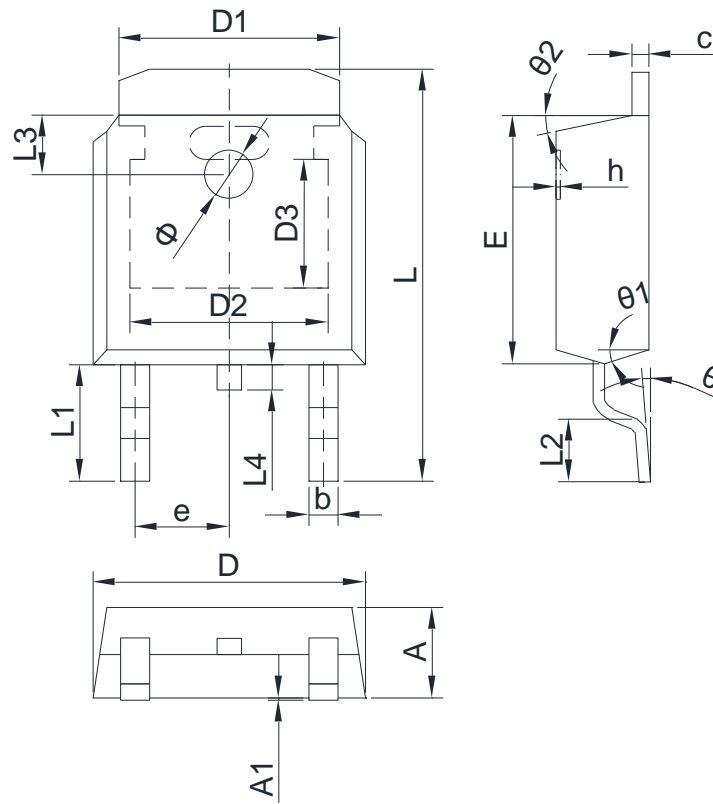


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

8. Dimension (TO-252)



SYMBOL	MILLIMETER			SYMBOL	MILLIMETER		
	MIN	Typ.	MAX		MIN	Typ.	MAX
A	2.200	2.300	2.400	h	0.000	0.100	0.200
A1	0.000		0.127	L	9.900	10.100	10.300
b	0.640	0.690	0.740	L1	2.888 REF		
C(电镀后)	0.460	0.520	0.580	L2	1.400	1.550	1.700
D	6.500	6.600	6.700	L3	1.600 REF		
D1	5.334 REF			L4	0.600	0.800	1.000
D2	4.826 REF			Φ	1.100	1.200	1.300
D3	3.166 REF			θ	0°		8°
E	6.000	6.100	6.200	θ_1	9° TYP		
e	2.286 TYP			θ_2	9° TYP		

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