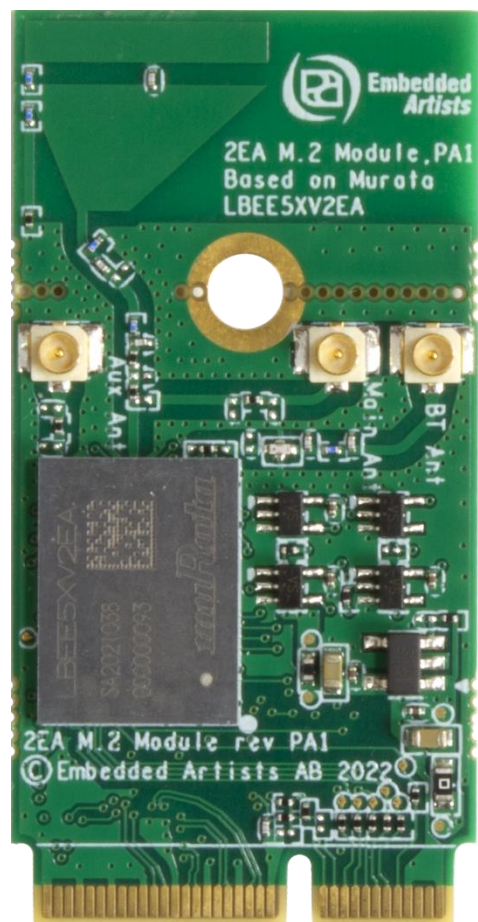


# 2EA M.2 Module Datasheet (EAR00413/ EAR00448)

- Wi-Fi 6E, 802.11 a/b/g/n/ac/ax 2x2 MIMO
- Bluetooth 5.2 BR/EDR/LE
- PCIe interface, in M.2 form factor (22 x 44 mm)
- Chipset: Infineon/Cypress CYW55573



*Get Up-and-Running Quickly and  
Start Developing Your Application on Day 1!*

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# 1 Document Information

This document applies to the following products.

| <i>Product Name</i>     | <i>Type Number</i>  | <i>Murata Module</i> | <i>Chipset</i> | <i>Product Status</i> |
|-------------------------|---------------------|----------------------|----------------|-----------------------|
| 2EA M.2 Module, rev PA1 | EAR00413 / EAR00448 | LBEE5XV2EA-SMP       | CYW55573       | Initial Production    |

This table below lists the product differences. All products are not stocked. Consult Embedded Artists for availability and lead time.

| <i>Type Number</i> | <i>Product Name</i> | <i>Host Interface for Wi-Fi / Bluetooth functionality</i> | <i>Packaging</i>                   |
|--------------------|---------------------|---|------------------------------------|
| EAR00413           | 2EA M.2 Module      | PCIe / UART   | Individual packing for evaluation. |
| EAR00448           | 2EA M.2 Module      | PCIe / UART   | Tray.                              |

## 1.1 Revision History

| <i>Revision</i> | <i>Date</i> | <i>Description</i>                                 |
|-----------------|-------------|--|
| PA1             | 2023-01-09  | First version.                                     |
| PA2             | 2023-05-11  | Added information on different reference antennas. |
| PA3             | 2023-06-14  | Corrected spelling error.                          |
| PA4             | 2024-03-15  | Added information about rev A of the board.        |

## 2 Introduction

This document is a datasheet that specifies and describes the *2EA M.2 module* mainly from a hardware point of view.

The main component in the design is Murata's 2EA module (full part number: LBEE5XV2EA-SMP). The 2EA M.2 module enables Wi-Fi, Bluetooth and Bluetooth Low Energy (LE) communication.

There are multiple application areas for the 2EA M.2 Module:

- Industrial and building automation
- Asset management
- IoT applications
- Smart home: Voice assist device, smart printer, smart speaker, home automation gateway, and IP camera
- Retail/POS
- Healthcare and medical devices
- Smart city

### 2.1 Benefits of Using an M.2 Module to get Wi-Fi/BT Connectivity

There are several benefits to use an *M.2 module* to add connectivity to an embedded design:

- Drop-in, certified solution!
- Modular and flexible approach to evaluate different Wi-Fi/BT solutions - with different trade-offs around performance, cost, power consumption, longevity, etc.
- Access to maintained software drivers (Linux and SDK) with responsive support from Murata.
- Supported by Embedded Artists' Developer's Kits for i.MX RT/6/7/8/9 development, including advanced debugging support on carrier boards
- One component to buy, instead of 40+
- No RF expertise is required
- Developed in close collaboration with Murata

### 2.2 More M.2 Related Information

For more information about the M.2 standard and Embedded Artists' adaptation, see: [M.2 Primer](#)

For more general information about the M.2 standard, see: <https://en.wikipedia.org/wiki/M.2>

The official M.2 specification (PCI Express M.2 Specification) is available from: [www.pcisig.com](http://www.pcisig.com)

### 2.3 ESD Precaution and Handling

Please note that the M.2 module come without any case/box and all components are exposed for finger touches – and therefore extra attention must be paid to ESD (electrostatic discharge) precaution, for example use of static-free workstation and grounding strap. Only qualified personnel shall handle the product.



***Make it a habit always to first touch the mounting hole (which is grounded) for a few seconds with both hands before touching any other parts of the boards.*** That way, you will have the same potential as the board and therefore minimize the risk for ESD.

In general, touch as little as possible on the boards to minimize the risk of ESD damage. The only reasons to touch the board are when mounting/unmounting it on a carrier board.

***Note that Embedded Artists does not replace modules that have been damaged by ESD.***

### 2.4 Product Compliance

Visit Embedded Artists' website at [http://www.embeddedartists.com/product\\_compliance](http://www.embeddedartists.com/product_compliance) for up-to-date information about product compliances such as CE, RoHS2/3, Conflict Minerals, REACH, etc.

### 3 Specification

This chapter lists some of the more important characteristics of the M.2 module, but it is not a full specification of performance and timing. The main component in the design is Murata's 2EA module (full part number: LBEE5XV2EA-SMP), which in turn is based around Infineon's CYW55573 chipset.

For a full specification, see Murata's 2EA Module (LBEE5XV2EA) product page:

<https://www.murata.com/en-us/products/connectivitymodule/wi-fi-bluetooth/overview/lineup/type2ea> and the LBEE5XV2EAdatasheet: <https://www.murata.com/products/productdata/TBD/type2ea.pdf>

| Module / Chipset |                   |
|------------------|-------------------|
| Murata module    | LBEE5XV2EA-802    |
| Chipset          | Infineon CYW55573 |

| Wi-Fi          |  |
|----------------|--|
| Standards      | 802.11a/b/g/n/ac/ax 2x2 MU-MIMO, Wi-Fi 6E                    |
| Network        | uAP and STA dual mode  |
| Frequency      | 2.4GHz, 5 GHz b and 6 GHz band                               |
| Data rates     | 11, 54, 144, 300, 867 Mbps                                   |
| Host interface | PCIe (default) or SDIO 3.0 with rework (or on special order) |

| Bluetooth       |                          |
|-----------------|--------------------------|
| Standards       | 5.2 BR/EDR/LE, 2Mbps PHY |
| Power Class     | Class 2                  |
| Host interface  | 4-wire UART@4MBaud       |
| Audio interface | PCM for audio            |

| Powering  |   |            |   |
|---|---|------------|---|
| Supply voltage to M.2 module  | <b>Min</b>  | <b>Typ</b> | <b>Max</b>  |
|   | 0.0V minimum<br>3.14V operating and<br>RF specification | 3.3V       | 3.5V  |
| <b>Note: Do not exceed minimum or maximum voltage. Module will be permanently damaged above this limit!</b> |   |            | <b>Note</b> that LBEE5XV2EA module specification has higher maximum voltage (4.8V), but other components on the M.2 module limit the maximum voltage. |
| Peak current  | TBD mA max  |            | <b>Note: The power supply must be designed for this peak current</b> , which typically happen during the startup calibration process.                 |
| Receive mode current (WLAN, Concurrent dual-band receive)   | TBD mA max  |            | Note that current consumption varies widely between different operational modes.  |

|   |            |  |
|---|------------|--|
| Transmit mode current (WLAN, Concurrent dual-band transmit) | TBD mA max | Note that current consumption varies widely between different operational modes. |
|---|------------|--|

| Environmental Specification                   |                            |
|---|----------------------------|
| Operational Temperature                       | -40 to +85 degrees Celsius |
| Specification Temperature                     | -30 to +70 degrees Celsius |
| Storage Temperature                           | -40 to +85 degrees Celsius |
| Relative Humidity (RH), operating and storage | 10 - 90% non-condensing    |

### 3.1 Power Up Sequence

The supply voltage shall not rise (10 - 90%) faster than 40 microseconds and not slower than 100 milliseconds.

Chipset signals WL\_REG\_ON (M.2 signal W\_DISABLE1#) and BT\_REG\_ON (M.2 signal W\_DISABLE2#) must be held low for at least 50 microseconds after supply voltage has reached specification level before pulled high. The 32.678kHz clock must also be active before any of the signals are pulled high. In addition to this, wait at least 150 ms after internal regulators and VDDIO are available before initiating PCIe accesses.

### 3.2 External Sleep Clock

The sleep clock signals can be applied to a powered and unpowered M.2 module (but have no effect when the M.2 module is unpowered).

| Clock Specification |  |
|---------------------|--|
| Frequency           | 32.768 kHz   |
| Frequency accuracy  | ±250 ppm including initial tolerance, aging, temperature, etc. |
| Duty cycle          | 30 - 70%   |
| Clock jitter        | 10 000 ppm max (during initial start-up)                       |
| Voltage level       | 3.3V logic, according to M.2 standard                          |



### 3.3 Mechanical Dimensions

The M.2 module is of type: 2230-D5-E according to the M.2 nomenclature. This means width 22 mm, length 30mm, top and bottom side component height 1.5 mm and key-E connector. The table below lists the different dimensions and weight.

| M.2 Module Dimension                    | Value ( $\pm 0.15$ mm) | Unit |
|---|------------------------|------|
| Width                                   | 22                     | mm   |
| Height, with pcb trace antenna          | 44                     | mm   |
| Height, without pcb trace antenna       | 30                     | mm   |
| PCB thickness                           | 0.8                    | mm   |
| Maximum component height on top side    | 1.5                    | mm   |
| Maximum component height on bottom side | 1.5                    | mm   |
| Ground hole diameter                    | 3.5                    | mm   |
| Plating around ground hole, diameter    | 5.5                    | mm   |
| Module weight                           | 1.5 $\pm$ 0.5 gram     | gram |

Embedded Artists has added a non-standard feature to the 2230 M.2 modules designed together with Murata, NXP and Infineon (former Cypress). The pictures below illustrate how the standard module size has been extended by 14 mm in the length direction to include a pcb trace antenna.

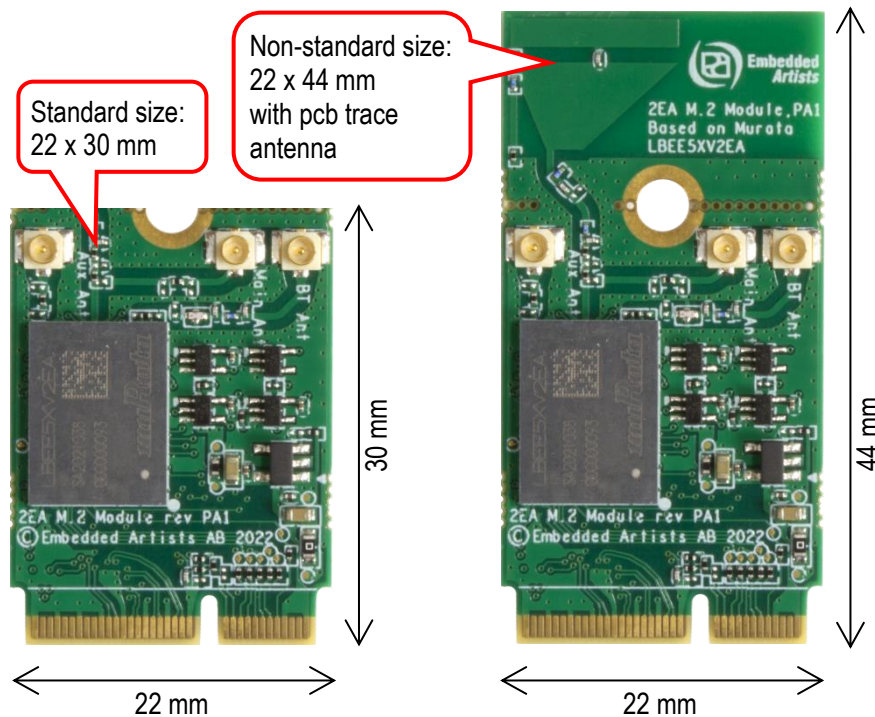


Figure 1 – M.2 Module with, and without, PCB Trace Antenna

The picture below gives dimensions for the grounded center (half) hole and the u.fl. antenna connector.

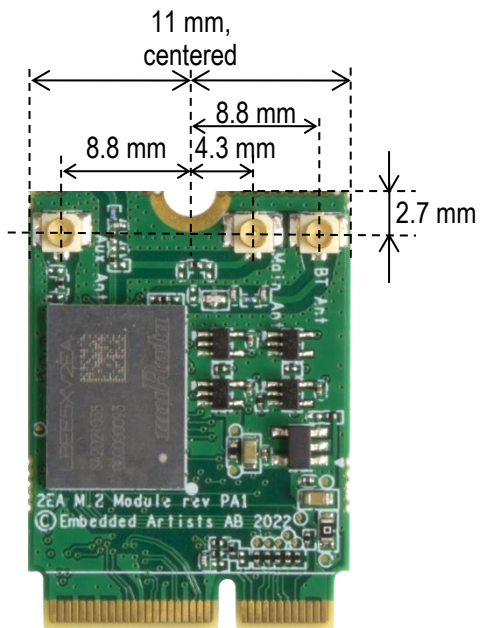


Figure 2 – M.2 Module Without Trace Antenna

### 3.4 M.2 Pinning

This section presents the pinning used for the M.2 module. It is essentially M.2 Key-E compliant with enhancements to support additional debug signals and 3.3V VDDIO override. The pin assignment for specific control and debug signals has been jointly defined by Embedded Artists, Murata, NXP and Infineon (former Cypress).

The picture below illustrates the edge pin numbering. It starts on the right edge and alternates between top and bottom side. The removed pads in the keying notch count (but are obviously non-existing).

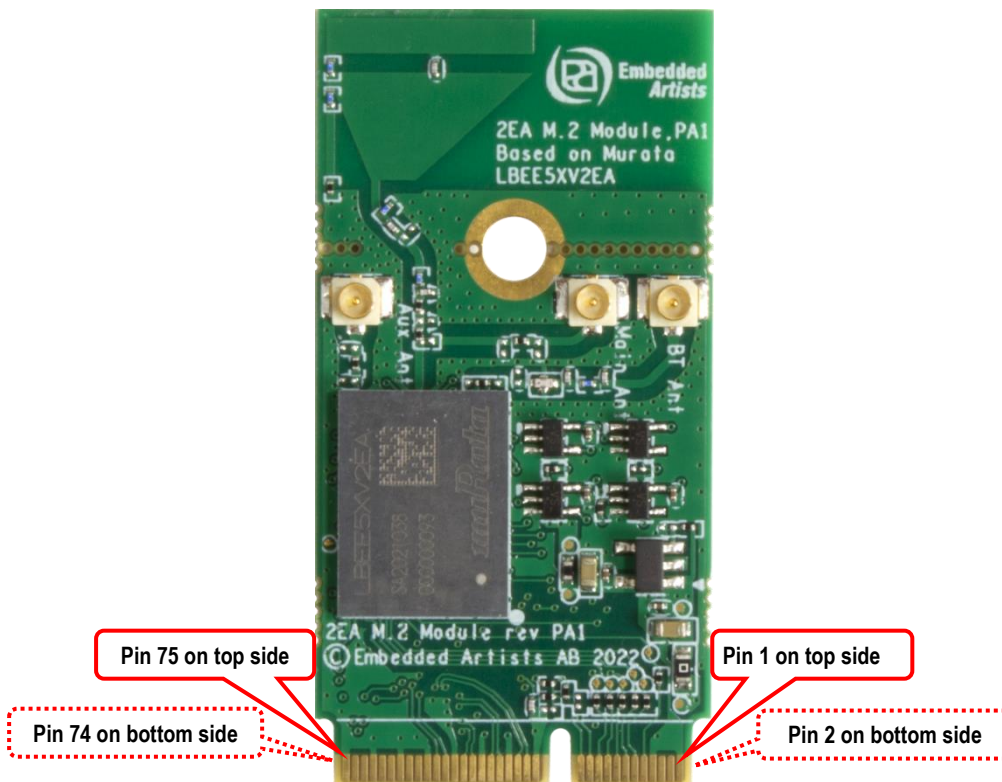


Figure 3 – M.2 Module Pin Numbering

The Wi-Fi interface uses the PCIe interface as default, but it is possible to configure the module to use the SDIO interface instead, see section 3.6 for details. The Bluetooth interface uses the UART interface for control and PCM interface for audio. The table below lists the pin usage for the 2EA M.2 module. The column "When is signal needed" signals four different categories:

- Always: These signals shall always be connected.
- Wi-Fi PCIe: These signals shall always be connected when the PCIe interface is used for Wi-Fi.
- Wi-Fi SDIO: These signals shall always be connected when the SDIO interface is used for Wi-Fi.
- Bluetooth: These signals shall always be connected when the Bluetooth interface is used.
- Optional: These signals are optional to connect.

| Pin # | Side of pcb | M.2 Name | Voltage Level and Signal Direction | When is signal needed | Note |
|-------|-------------|----------|------------------------------------|-----------------------|------|
|-------|-------------|----------|------------------------------------|-----------------------|------|

|    |        |            |                      |                 |   |
|----|--------|------------|----------------------|-----------------|---|
| 1  | Top    | GND        | GND                  | Always          | Connect to ground   |
| 2  | Bottom | 3.3 V      |                      | Always          | Power supply input. Connect to stable, low-noise 3.3V supply.   |
| 3  | Top    | USB_D+     |                      |                 | Not connected.  |
| 4  | Bottom | 3.3 V      |                      | Always          | Power supply input. Connect to stable, low-noise 3.3V supply.   |
| 5  | Top    | USB_D-     |                      |                 | Not connected.  |
| 6  | Bottom | LED_1#     |                      |                 | Not connected.  |
| 7  | Top    | GND        | GND                  | Always          | Connect to ground.  |
| 8  | Bottom | PCM_CLK    | 1.8V I/O             | Bluetooth audio | For Bluetooth audio interface: BT_PCM_CLK<br>Connected to 2EA module, signal BT_PCM_CLK, pin 7  |
| 9  | Top    | SDIO_CLK   | 1.8V Input to M.2    | Wi-Fi SDIO      | For Wi-Fi SDIO interface: SDIO_CLK<br>Connected to 2EA module, signal SDIO_CLK, pin 65  |
| 10 | Bottom | PCM_SYNC   | 1.8V I/O             | Bluetooth audio | For Bluetooth audio interface: BT_PCM_SYNC<br>Connected to 2EA module, signal BT_PCM_SYNC, pin 5  |
| 11 | Top    | SDIO_CMD   | 1.8V I/O             | Wi-Fi SDIO      | For Wi-Fi SDIO interface: SDIO_CMD<br>Connected to 2EA module, signal SDIO_CMD, pin 64<br>Note: Require an external 10-100K ohm pullup  |
| 12 | Bottom | PCM_OUT    | 1.8V output from M.2 | Bluetooth audio | For Bluetooth audio interface: BT_PCM_OUT<br>Connected to 2EA module, signal BT_PCM_OUT, pin 8  |
| 13 | Top    | SDIO_DATA0 | 1.8V I/O             | Wi-Fi SDIO      | For Wi-Fi SDIO interface: SDIO_D0<br>Connected to 2EA module, signal SDIO_DATA_0, pin 62<br>Note: Require an external 10-100K ohm pullup  |
| 14 | Bottom | PCM_IN     | 1.8V input to M.2    | Bluetooth audio | For Bluetooth audio interface: BT_PCM_IN<br>Connected to 2EA module, signal BT_PCM_IN, pin 6  |
| 15 | Top    | SDIO_DATA1 | 1.8V I/O             | Wi-Fi SDIO      | For Wi-Fi SDIO interface: SDIO_D1<br>Connected to 2EA module, signal SDIO_DATA_1, pin 63<br>Note: Require an external 10-100K ohm pullup  |
| 16 | Bottom | LED_2#     |                      |                 | Not connected.  |
| 17 | Top    | SDIO_DATA2 | 1.8V I/O             | Wi-Fi SDIO      | For Wi-Fi SDIO interface: SDIO_D2<br>Connected to 2EA module, signal SDIO_DATA_2, pin 61<br>Note: Require an external 10-100K ohm pullup  |
| 18 | Bottom | GND        |                      | Always          | Connect to ground.  |
| 19 | Top    | SDIO_DATA3 | 1.8V I/O             | Wi-Fi SDIO      | For Wi-Fi SDIO interface: SDIO_D3<br>Connected to 2EA module, signal SDIO_DATA_3, pin 66<br>Note: Require an external 10-100K ohm pullup  |
| 20 | Bottom | UART_WAKE# | 3.3V output from M.2 | Bluetooth       | For Bluetooth UART interface: BT_HOST_WAKE_L<br>This is a wake signal for the Bluetooth interface from the device (Wi-Fi/BT chipset) to the host (CPU).<br>Connected to 2EA module, via buffer, signal BT_HOST_WAKE, pin 27 |
| 21 | Top    | SDIO_WAKE# | 1.8V output from M.2 | Wi-Fi SDIO      | For Wi-Fi SDIO interface WL_HOST_WAKE_L<br>This is a wake signal for the Wi-Fi interface from the device (Wi-Fi/BT chipset) to the host (CPU).<br>Connected to 2EA module, via buffer, signal GPIO_0, pin 43                |
| 22 | Bottom | UART_TXD   | 1.8V output from M.2 | Bluetooth       | For Bluetooth UART interface: BT_UART_TXD<br>Connected to 2EA module, signal BT_UART_TXD, pin 18  |

|       |                   |                |                                  |            |   |
|-------|-------------------|----------------|----------------------------------|------------|---|
| 23    | Top               | SDIO RESET#    |                                  |            | Not connected.<br>The Wi-Fi SDIO interface is controlled by pin 56, W_DISABLE1#, which is a 3.3V logic level signal.  |
| 24-31 | Key, non-existing |                |                                  |            |   |
| 32    | Bottom            | UART_RXD       | 1.8V input to M.2                | Bluetooth  | For Bluetooth UART interface: BT_UART_RXD<br>Connected to 2EA module, signal BT_UART_RXD, pin 16  |
| 33    | Top               | GND            |                                  | Always     | Connect to ground.  |
| 34    | Bottom            | UART_RTS       | 1.8V output from M.2             | Bluetooth  | For Bluetooth UART interface: BT_UART_RTS<br>Connected to 2EA module, signal BT_UART_RTS_N, pin 17  |
| 35    | Top               | PERp0          | PCIe input to M.2                | Wi-Fi PCIe | PCIe data input (receive, positive signal)<br>Connected to 2EA module, signal PCIE_RDP, pin 68  |
| 36    | Bottom            | UART_CTS       | 1.8V input to M.2                | Bluetooth  | For Bluetooth UART interface: BT_UART_CTS<br>Connected to 2EA module, signal BT_UART_CTS_N, pin 19  |
| 37    | Top               | PERn0          | PCIe input to M.2                | Wi-Fi PCIe | PCIe data input (receive, negative signal)<br>Connected to 2EA module, signal PCIE_RDN, pin 69  |
| 38    | Bottom            | VENDOR DEFINED |                                  |            | Not connected.  |
| 39    | Top               | GND            |                                  | Always     | Connect to ground.  |
| 40    | Bottom            | VENDOR DEFINED | 1.8V I/O                         | Wi-Fi SDIO | For Wi-Fi SDIO interface WL_DEV_WAKE_L<br>This is a wake signal for the Wi-Fi interface from the host (CPU) to the device (Wi-Fi/BT chipset).<br>Connected to 2EA module, signal LHL_GPIO1, pin 32            |
| 41    | Top               | PETp0          | PCIe output from M.2             | Wi-Fi PCIe | PCIe data output (transmit, positive signal)<br>Connected to 2EA module, via 100nF capacitor, signal PCIE_TDP, pin 71   |
| 42    | Bottom            | VENDOR DEFINED | 1.8V input to M.2 <sup>(1)</sup> | Bluetooth  | For Bluetooth UART interface: BT_DEV_WAKE_L<br>This is a wake signal for the Bluetooth interface from the host (CPU) to the device (Wi-Fi/BT chipset).<br>Connected to 2EA module, signal BT_DEV_WAKE, pin 26 |
| 43    | Top               | PETn0          | PCIe output from M.2             | Wi-Fi PCIe | PCIe data output (transmit, negative signal)<br>Connected to 2EA module, via 100nF capacitor, signal PCIE_TDN, pin 72   |
| 44    | Bottom            | COEX3          |                                  |            | Not connected.  |
| 45    | Top               | GND            |                                  | Always     | Connect to ground.  |
| 46    | Bottom            | COEX_TXD       |                                  |            | Not connected.  |
| 47    | Top               | REFCLKp0       | PCIe clock input to M.2          | Wi-Fi PCIe | PCIe clock input (receive, positive signal)<br>Connected to 2EA module, signal PCIE_REFCLKP, pin 74   |
| 48    | Bottom            | COEX_RXD       |                                  |            | Not connected.  |
| 49    | Top               | REFCLKn0       | PCIe clock input to M.2          | Wi-Fi PCIe | PCIe clock input (receive, negative signal)<br>Connected to 2EA module, signal PCIE_REFCLKN, pin 75   |
| 50    | Bottom            | SUSCLK         |                                  |            | External sleep clock input (32.768kHz)<br>Connected to 2EA module, via buffer, signal LPO_IN, pin 51  |
| 51    | Top               | GND            |                                  | Always     | Connect to ground.  |
| 52    | Bottom            | PERST0#        | 3.3V input to M.2                | Wi-Fi PCIe | PCIe PERST# signal, used to initialize the M.2 functions once power sources stabilize.<br>Connected to 2EA module, via voltage translator, signal PCIE_PERST_L, pin 1   |

|    |        |                      |                         |            |  |
|----|--------|----------------------|-------------------------|------------|--|
| 53 | Top    | CLKREQ0#             | 3.3V OD output from M.2 | Wi-Fi PCIe | PCIe clock request (low level request reference clock)<br>Connected to 2EA module, via open drain buffer, signal PCIE_CLKREQ_N, pin 2<br><b>Note:</b> Requires external 10Kohm pull-up |
| 54 | Bottom | W_DISABLE2#          | 3.3V input to M.2       | Always     | Connected to 2EA module, via buffer, signal BTREG_ON, pin 45<br>High = Bluetooth funct. enabled/internally powered,<br>Low = Bluetooth funct. disabled/powered down                    |
| 55 | Top    | PEWAKE0#             | 3.3V OD output from M.2 | Wi-Fi PCIe | PCIe wake request (low level request host wakeup)<br>Connected to 2EA module, via open drain buffer, signal PCIE_PME_L, pin 3<br><b>Note:</b> Requires external 10Kohm pull-up         |
| 56 | Bottom | W_DISABLE1#          | 3.3V input to M.2       | Always     | Connected to 2EA module, via buffer, signal WLREG_ON, pin 60<br>High = Wi-Fi funct. enabled/internally powered,<br>Low = Wi-Fi funct. disabled/powered down                            |
| 57 | Top    | GND                  |                         | Always     | Connect to ground.   |
| 58 | Bottom | I2C_SDA              |                         |            | Not connected.   |
| 59 | Top    | Reserved             |                         |            | Not connected.   |
| 60 | Bottom | I2C_CLK              |                         |            | Not connected.   |
| 61 | Top    | Reserved             |                         |            | Not connected.   |
| 62 | Bottom | ALERT#               |                         |            | Not connected.   |
| 63 | Top    | GND                  |                         | Always     | Connect to ground.   |
| 64 | Bottom | RESERVED             |                         |            | Not connected.   |
| 65 | Top    | Reserved             |                         |            | Not connected.   |
| 66 | Bottom | UIM_SWP              |                         |            | Not connected.   |
| 67 | Top    | Reserved             |                         |            | Not connected.   |
| 68 | Bottom | UIM_POWER_SNK        |                         |            | Not connected.   |
| 69 | Top    | GND                  |                         | Always     | Connect to ground.   |
| 70 | Bottom | UIM_POWER_SRC/GPIO_1 |                         |            | Not connected.   |
| 71 | Top    | Reserved             |                         |            | Not connected.   |
| 72 | Bottom | 3.3 V                |                         | Always     | Power supply input. Connect to stable, low-noise 3.3V supply.  |
| 73 | Top    | Reserved             |                         |            | Not connected.   |
| 74 | Bottom | 3.3 V                |                         | Always     | Power supply input. Connect to stable, low-noise 3.3V supply.  |
| 75 | Top    | GND                  |                         | Always     | Connect to ground.   |

### 3.5 SDIO Interface

The SDIO interface conforms to the SDIO v3.0 specification, including the UHS-I modes, and is backward compatible with SDIO v2.0.

**Note: The SDIO interface is not enabled by default.** It requires a manual rework of the hardware to be enabled (can be ordered as a special mounting option). Software drivers must also be updated to support the SDIO interface.

| SDIO bus speed modes | Max SDIO clock frequency | Max bus speed | Signaling voltage according to M.2 specification |
|----------------------|--------------------------|---------------|--|
| DS (Default speed)   | 25 MHz                   | 12.5 MByte/s  | 1.8 V  |
| HS (High speed)      | 50 MHz                   | 25 MByte/s    | 1.8 V  |
| SDR12                | 25 MHz                   | 12.5 MByte/s  | 1.8 V  |
| SDR25                | 50 MHz                   | 25 MByte/s    | 1.8 V  |
| SDR50                | 100 MHz                  | 50 MByte/s    | 1.8 V  |
| SDR104               | 208 MHz                  | 104 MByte/s   | 1.8 V  |

### 3.6 Wi-Fi Interface Control

The **default interface** for Wi-Fi is **PCIe**. It is possible to change this to the SDIO interface with a small rework, as described in the picture below.

The picture below illustrates how to do the rework on rev PA1 boards.

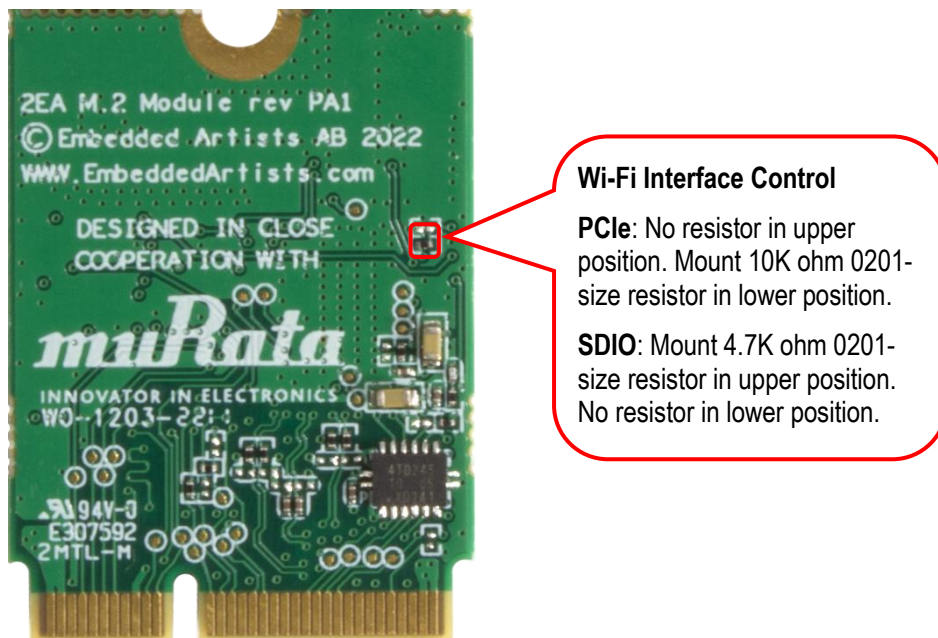


Figure 4 – 2EA M.2 Module Wi-Fi Interface Control, rev PA1

The picture below illustrates how to do the rework on rev A boards. Note that the zero ohm resistor (0402 or 0603 size recommended) can also be just a solder bump. The solder bump is a simple solution if there is no SMT resistor available.

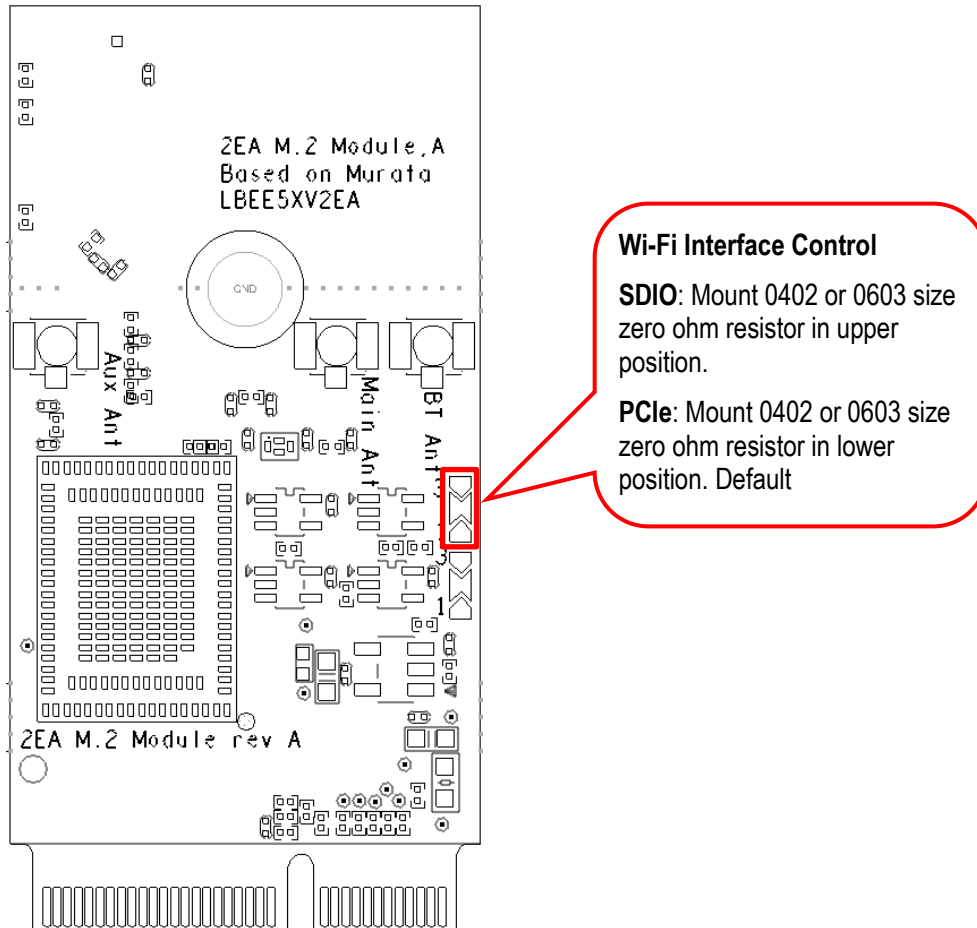


Figure 5 – 2EA M.2 Module Wi-Fi Interface Control, rev A



### 3.7 Test Points

There are some test points that can be of interest to probe for debugging purposes, as illustrated in the picture below.

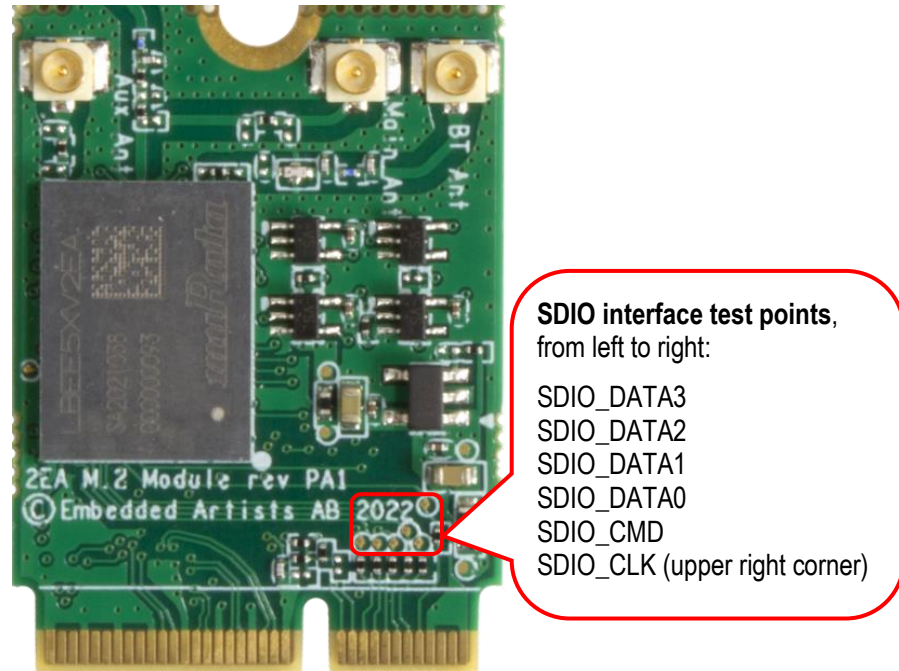


Figure 6 – 2EA M.2 Module Top Side Test Points

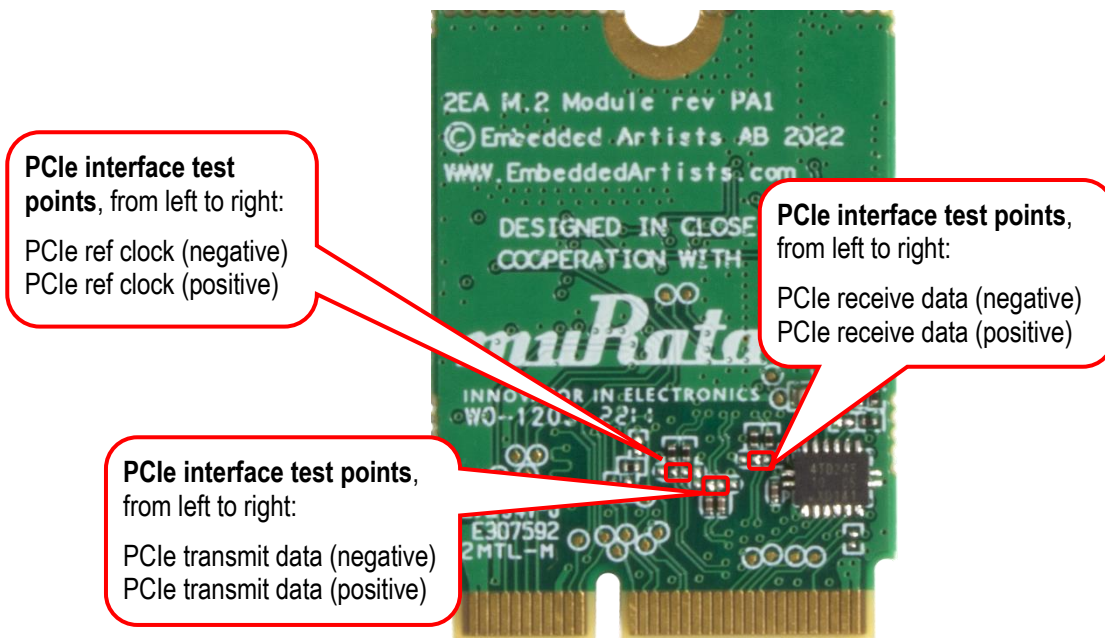


Figure 7 – 2EA M.2 Module Bottom Side Test Points

### 3.8 Current Consumption Measurements

It is possible to measure the currents of the power supplies to the 2EA module, VBAT and VDDIO. VBAT is the 3.3V that is supplied to the M.2 interface and VDDIO is an on-board generated 1.8V. VDDIO is generated from the supplied 3.3V. Note that when measuring the VBAT current, the VDDIO current will be included in this measurement. The VDDIO current can however be measured independently.

Note that zero ohm resistors are mounted by default. Select a series resistor with as low resistance as possible to keep the voltage drop to a minimum. Keep the drop below 100mV. VBAT can be above 1 Amp in peak which means that maximum series resistance is 100 milliOhm for the VBAT resistor. For VDDIO the current is lower so a 1 ohm resistor can be a suitable value.

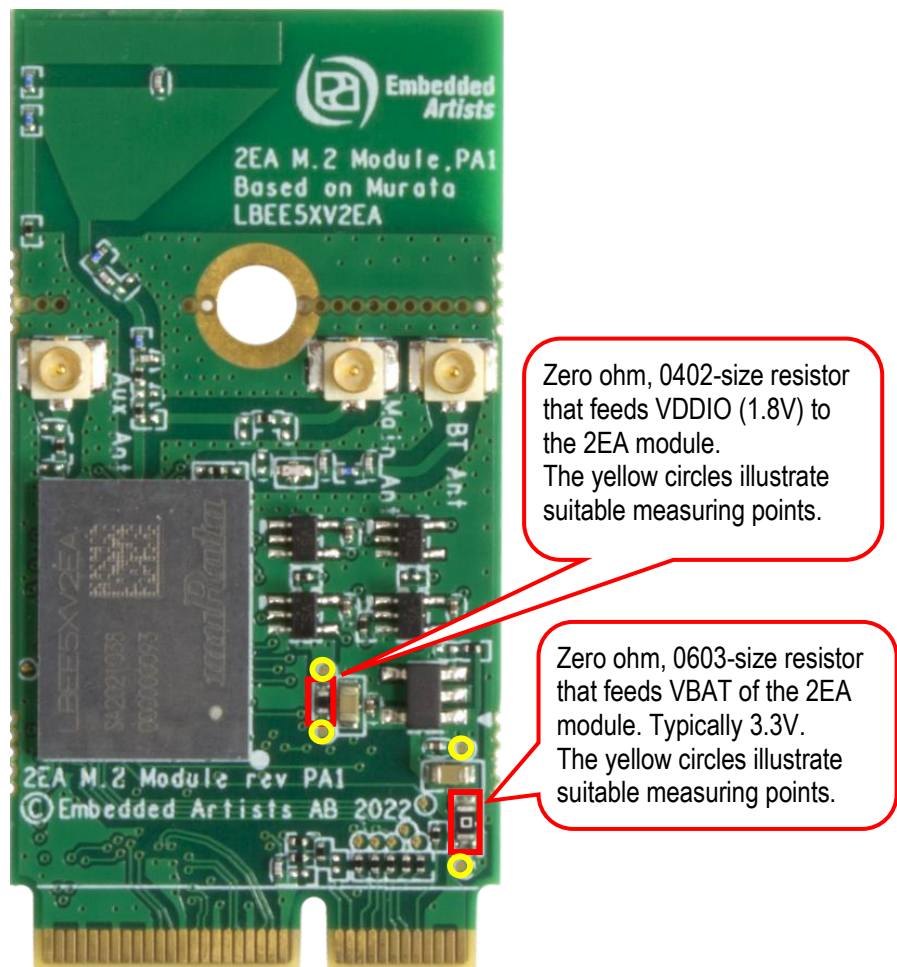


Figure 8 – Current Measurement

## 4 Antenna

This chapter addresses the antenna side of the module. There is an on-board, reference certified pcb trace antenna for 1x1 SISO operation. This can be used for testing/evaluation purposes, but also for the final product. Also, for testing and evaluation purposes, it is possible to disconnect the on-board antenna and instead use the u.fl. connectors to connect external antennas.

It is not possible to have two on-board antennas for 2x2 MIMO operation because the M.2 module is too small to get spatial separation of the two antennas. Two external antennas must be connected to support 2x2 MIMO operation.

### 4.1 Reference Certified External Antenna

There are multiple reference certified antennas to choose from, see table below. Note that there are different antennas depending on if the 2EA module operates in SISO or MIMO mode.

| Mode of Operation      | Antenna type | Supplier | Antenna Part Number | Frequency (MHz) | Peak Antenna Gain (dBi) |
|------------------------|--------------|----------|---------------------|-----------------|-------------------------|
| SISO operation         | Monopole     | Murata   | On-board            | 5925-7125       | 2.5                     |
| SISO operation         | Dipole       | Molex    | 146153              | 5925-7125       | 5.8                     |
| SISO or MIMO operation | Dipole       | Molex    | 219611              | 5925-7125       | 4                       |
| SISO or MIMO operation | Dipole       | Unictron | WT32D1-KX           | 5925-7125       | 4                       |

Both Molex 1461530050 and 2196110050 are balanced, dipole-type, high efficiency antennas used for the reference certification of the Murata 2EA module (note that 1461530050 is only certified for SISO operation). These are ground plane independent, tripple band antennas that support the 2400-2500MHz, 5150-5850MHz, 5925-7125MHz frequency bands. They are physically small (41 x 9 x 0.7mm and 35.4 x 15.4 x 0.23mm, respectively). The antenna cables come in 6 standard length options: 50/100/150/200/250/300mm (50mm is used for the reference certification) and the connector is MHF-I, which is a U.FL compatible connector.



Figure 9 – Reference Certified Antenna

Note that no antennas are included when ordering the evaluation bundle of the 2EA M.2 board. The on-board antenna is used for the default SISO operation.

## 4.2 Antenna Connector

The M.2 standard specifies a 1.5 mm outer ring diameter male connector, which is compatible with the Murata MSC and IPEX MHF4 connector specifications. This connector is not used since our M.2 modules also target industrial users, where the Hirose U.FL. connector standard is more commonly used. U.FL. is compatible with the IPEX MHF1 connector specification.

## 4.3 Mounting and Clearance for On-board Antenna

Ideally, arrange the M.2 module so that the antenna is located at a corner of the product. Keep plastic case (i.e., non-metallic) away from the antenna area with at least 5 mm clearance (in all directions). Also keep any metal elements (e.g., connectors, battery, etc.) away from the antenna area with at least 5 mm clearance (in all directions). Keep a clearance area under and above the antenna area of at least 7.5mm, both under and over the PCB.

Human hands or body parts should be kept away (in the normal use case) from the antenna area.

The ground hole in the middle shall be grounded. Use a metal stand-off according to M.2 standard (height suitable for selected M.2 connector) and use metal screw to create a proper ground connection.

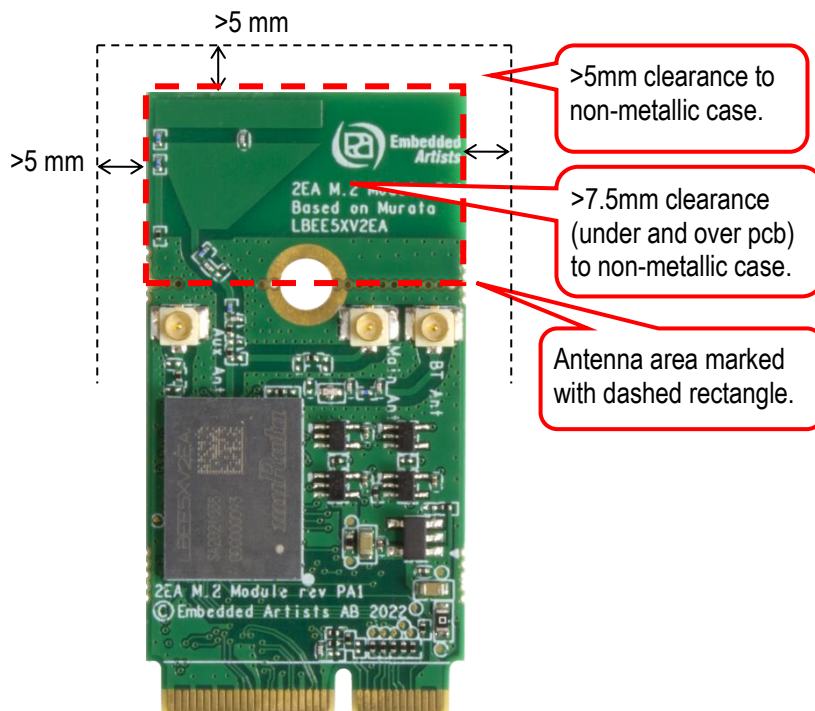


Figure 10 – M.2 Module Clearance Area

#### 4.4 Overriding on-board PCB Trace Antenna

Per default, the on-board PCB trace antenna is used for the Wi-Fi and Bluetooth interface. The antenna connection from the 2EA module can be redirected to the U.FL. connector by just moving one zero ohm 0201 series resistor, see illustration below. The on-board trace antenna can be left as-is, or the antenna part can be snapped-off.

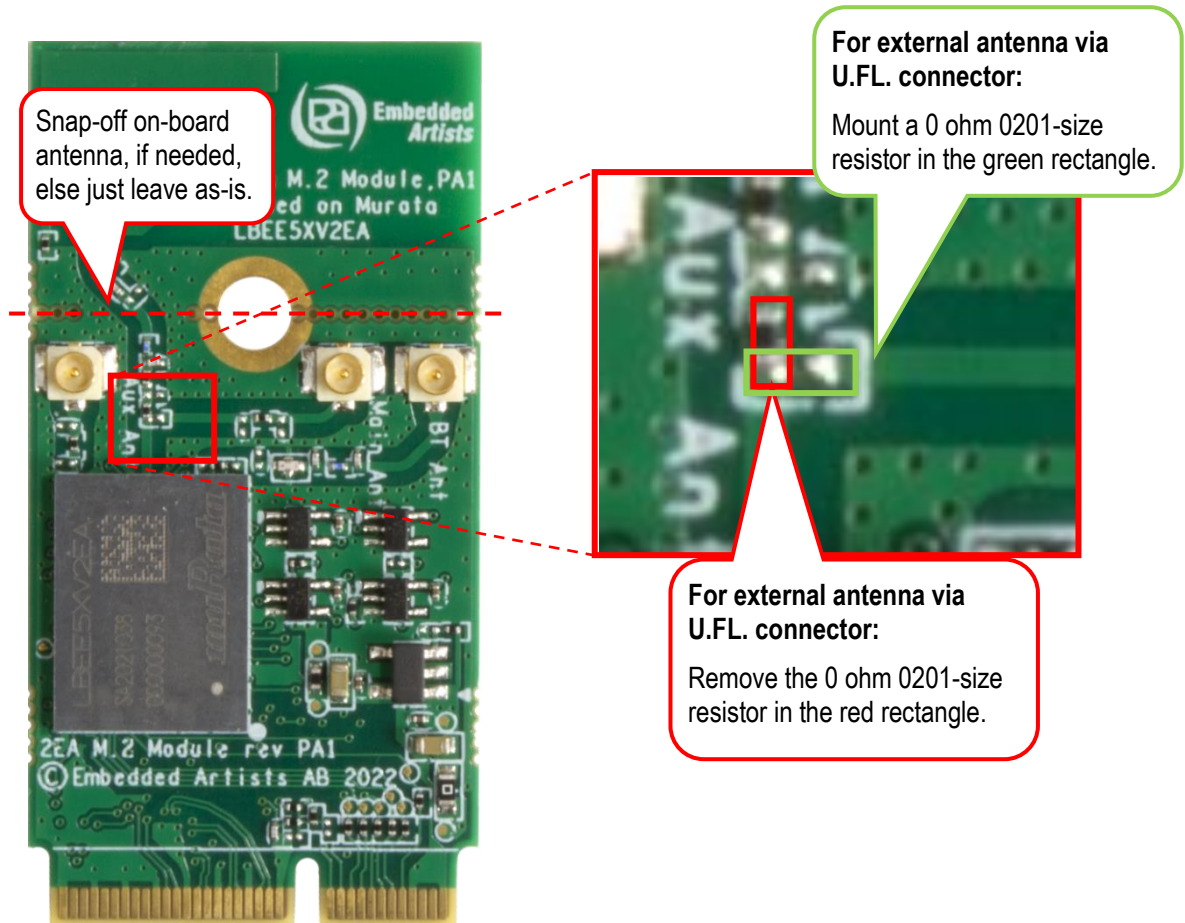


Figure 11 – Rework to Connect U.F.L. Connector

After the rework, the three antenna connectors are located as illustrated below.

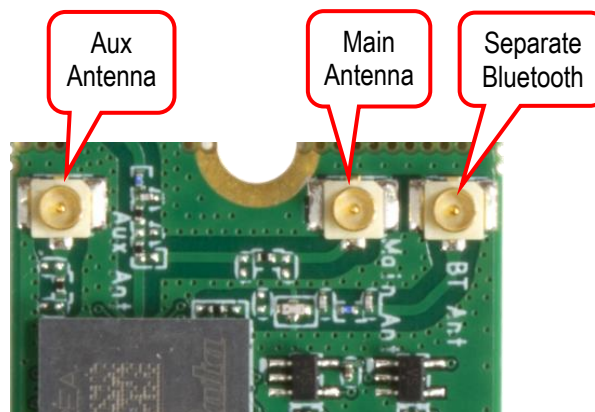


Figure 12 – 2EA M.2 Module Antenna Connectors

### 4.5 On-board PCB Trace Antenna Performance

The on-board pcb trace antenna type is monopole, certified by Murata.

The table below lists total efficiency:

| Measurement condition   | Frequency MHz |      |      |      |      |      | Total Efficiency in dB |                    | Total Efficiency in % |                    |
|-------------------------|---------------|------|------|------|------|------|------------------------|--------------------|-----------------------|--------------------|
|                         | 2400          | 2442 | 2484 | 5150 | 5500 | 5850 | Average 2 GHz band     | Average 5 GHz band | Average 2 GHz band    | Average 5 GHz band |
| Certified trace antenna | -1.0          | -1.0 | -0.9 | -1.3 | -1.6 | -1.5 | -1.0                   | -1.5               | 80.1                  | 71.5               |

The table below lists peak gain:

| Measurement condition   | Frequency MHz |      |      |      |      |      | Max dBi        |                |
|-------------------------|---------------|------|------|------|------|------|----------------|----------------|
|                         | 2400          | 2442 | 2484 | 5150 | 5500 | 5850 | Max 2 GHz band | Max 5 GHz band |
| Certified trace antenna | 2.6           | 2.4  | 2.5  | 3.5  | 3.6  | 3.5  | 2.6            | 3.64           |

The pictures below illustrate the return loss and efficiency.

### <Return Loss>

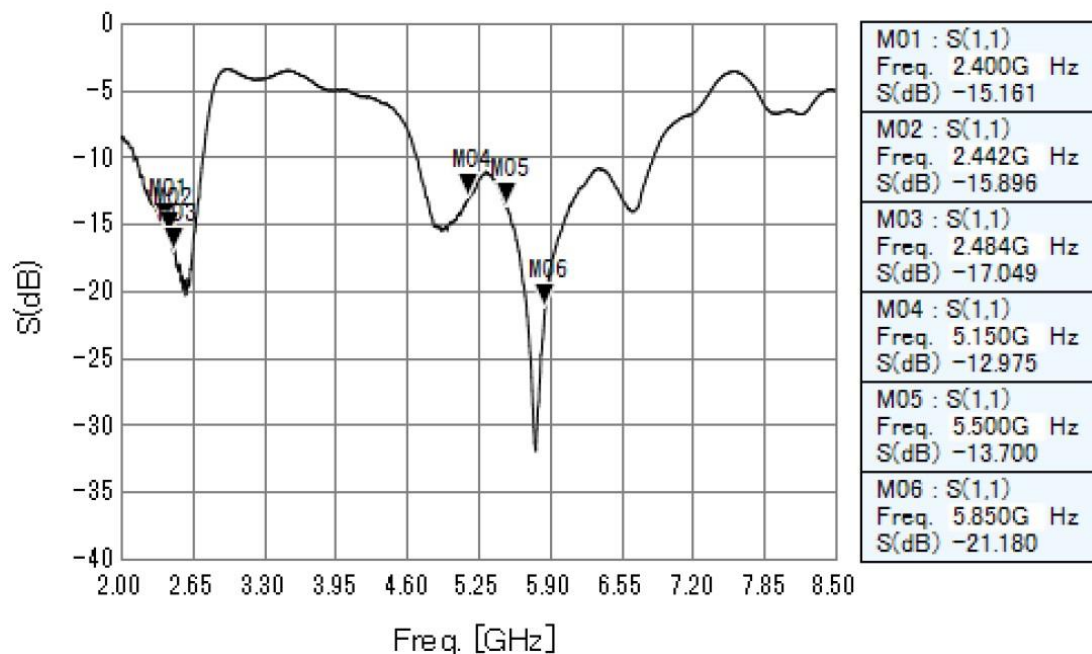


Figure 13 – Return Loss for Certified Trace Antenna

### <Efficiency>

| LINEAR POLARIZATION |      | XY-plane |      | YZ-plane |       | ZX-plane |      | Total Efficiency |
|---------------------|------|----------|------|----------|-------|----------|------|------------------|
|                     |      | hor.     | ver. | hor.     | ver.  | hor.     | ver. |                  |
| 2400 MHz            | MAX. | -1.6     | -0.9 | 2.6      | -16.3 | -2.2     | 1.0  | -1.0             |
|                     | AVE. | -4.9     | -4.6 | -2.0     | -20.4 | -8.3     | -0.9 |                  |
| 2442 MHz            | MAX. | -1.6     | -0.8 | 2.4      | -15.0 | -2.0     | 1.1  | -1.0             |
|                     | AVE. | -5.1     | -4.6 | -1.9     | -19.5 | -8.3     | -0.7 |                  |
| 2484 MHz            | MAX. | -1.7     | -0.7 | 2.5      | -13.6 | -1.7     | 1.6  | -0.9             |
|                     | AVE. | -5.2     | -4.5 | -1.6     | -18.7 | -8.2     | -0.5 |                  |

| LINEAR POLARIZATION |      | XY-plane |      | YZ-plane |       | ZX-plane |      | Total Efficiency |
|---------------------|------|----------|------|----------|-------|----------|------|------------------|
|                     |      | hor.     | ver. | hor.     | ver.  | hor.     | ver. |                  |
| 5150 MHz            | MAX. | 2.3      | 0.1  | 2.2      | -11.4 | 3.5      | -0.2 | -1.3             |
|                     | AVE. | -4.1     | -4.5 | -2.0     | -19.2 | -3.9     | -3.9 |                  |
| 5500 MHz            | MAX. | 2.3      | -0.6 | 1.0      | -12.7 | 3.6      | -1.8 | -1.6             |
|                     | AVE. | -4.3     | -5.0 | -2.4     | -20.0 | -4.3     | -5.1 |                  |
| 5850 MHz            | MAX. | 2.3      | -0.7 | 1.0      | -12.9 | 3.5      | -1.6 | -1.5             |
|                     | AVE. | -4.1     | -5.4 | -2.4     | -19.8 | -4.2     | -5.5 |                  |

Figure 14 – Efficiency for Certified Trace Antenna

The directivity measurements are presented below for the 2 GHz and 5GHz bands with the orientation as illustrated below.

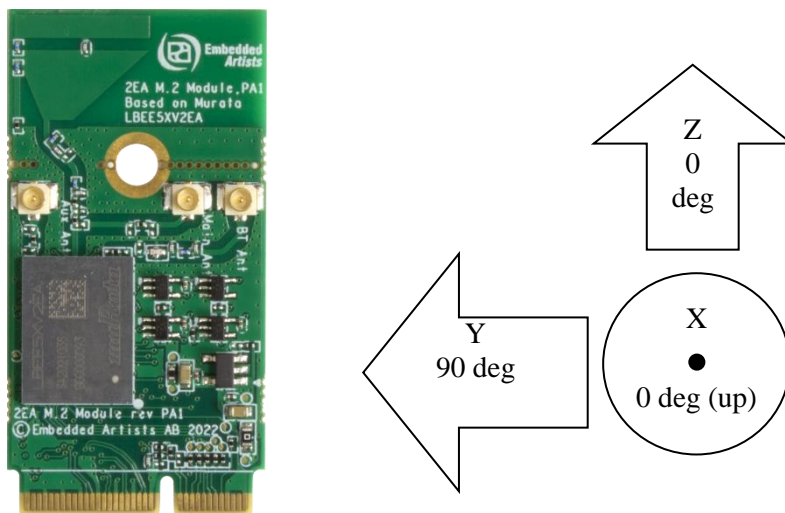
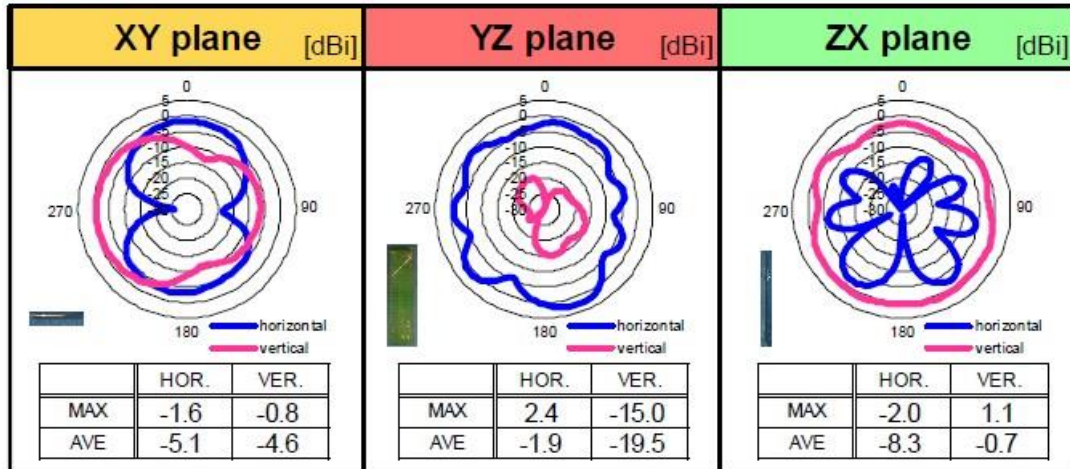


Figure 15 –Plane Orientations

### <Directivity>

@2442MHz



@5500MHz

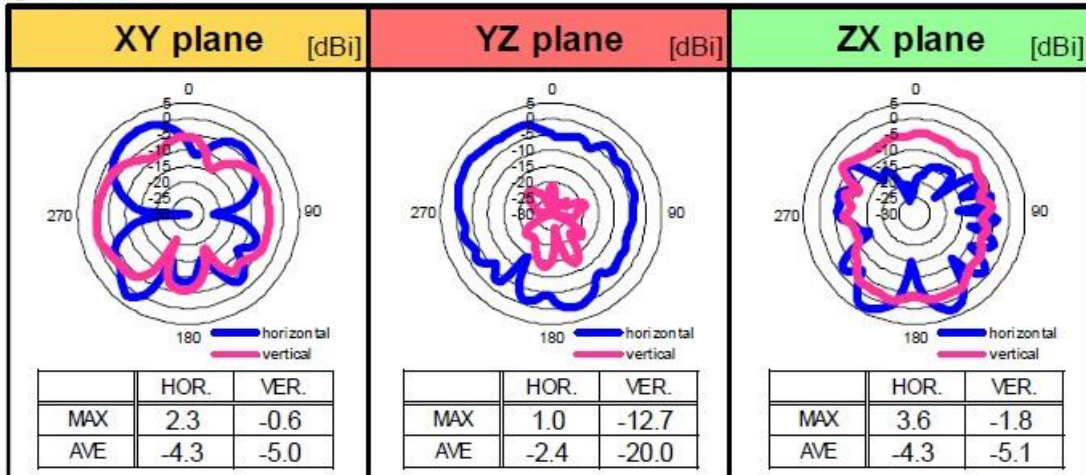


Figure 16 – Directivity for Certified Trace Antenna



## 5 Software and Support

This chapter contains information about software and support.

### 5.1 Software Driver

The CYW 55573 chipset does not contain any persistent software. A firmware image must be downloaded by the host at start-up. This is the responsibility of the operating system driver.

There are three different cases, depending on which host processor is used:

1. **Embedded Artists' Computer-on-Modules, (u)COM, as host processor**

Embedded Artists' Linux BSPs and SDKs for the different (u)COM board contains all drivers available and pre-configured. Everything has been tested and works out-of-the-box on our many iMX Developer's Kits.

| iMX Developer's Kit    | 2EA M.2 PCIe support | 2EA M.2 SDIO support |
|------------------------|----------------------|----------------------|
| iMX93 uCOM             | Not yet released     | Not yet released     |
| iMX8M Mini uCOM        | Linux v5.10.72       | TBD                  |
| iMX8M Nano uCOM        | No                   | No                   |
| iMX7 Dual COM          | Linux v5.10.72       | TBD                  |
| iMX7 Dual uCOM         | Linux v5.10.72       | TBD                  |
| iMX7ULP uCOM           | No                   | No                   |
| iMX6 Quad COM          | Linux v5.10.72       | TBD                  |
| iMX6 DualLite COM      | Linux v5.10.72       | TBD                  |
| iMX6 SoloX COM         | Linux v5.10.72       | TBD                  |
| iMX6 UltraLite/ULL COM | No                   | No                   |
| iMX RT1176 uCOM        | No                   | No                   |
| iMX RT1166 uCOM        | No                   | No                   |
| iMX RT1064 uCOM        | No                   | No                   |
| iMX RT1062 OEM         | No                   | No                   |

2. **Other i.MX based, for example NXP's EVKs**

Murata has created documentation how to compile the Linux kernel for the NXP EVKs  
<https://wireless.murata.com/products/rf-modules-1/wi-fi-bluetooth-for-nxp-i-mx.html#Linux>

3. **Non-i.MX host processor**

There is no ready-to-go driver exist. Contact Murata to check driver availability on the hardware platform used.

### 5.2 Support

Embedded Artists supports customers that use our M.2 module in combination with Embedded Artists' Computer-on-Modules, (u)COM, based on NXP's i.MX RT/6/7/8/9 families.

For other platforms, support is provided by Murata via their Community Support Forum:  
<https://community.murata.com/s/topic/0TO5F0000002TLWWA2/connectivity-modules>

## 6 Regulatory

The Murata 2EA module is reference certified. See the LBEE5XV2EA datasheet from Murata for details.

### 6.1 European Union Regulatory Compliance

**EUROPEAN DECLARATION OF CONFORMITY** (Simplified DoC per Article 10.9 of the Radio Equipment Directive 2014/53/EU)

This apparatus, namely 2EA M.2 module (pn EAR00413 / EAR00448) conforms to the Radio Equipment Directive (RED) 2014/53/EU. The full EU Declaration of Conformity for this apparatus can be found at this location: <https://www.embeddedartists.com/products/2ea-m-2-module/>, see documents *2EA M.2 module Declaration of Conformity*.

The following information is provided per Article 10.8 of the Radio Equipment Directive 2014/53/EU:

(a) Frequency bands in which the equipment operates.

(b) The maximum RF power transmitted.

| PN                  | RF Technology              | (a) Frequency Ranges (EU) | (b) Max Transmitted Power |
|---------------------|----------------------------|---------------------------|---------------------------|
| EAR00413 / EAR00448 | Bluetooth BR/EDR/LE        | 2400 MHz – 2484 MHz       | 6 dBm                     |
| EAR00413 / EAR00448 | Wi-Fi IEEE 802.11b/g/n     | 2400 MHz – 2484 MHz       | 20 dBm                    |
| EAR00413 / EAR00448 | Wi-Fi IEEE 802.11a/n/ac/ax | 5150 MHz – 5850 MHz       | 19 dBm                    |
| EAR00413 / EAR00448 | Wi-Fi IEEE 802.11ax        | 5985 MHz – 7025 MHz       | TBD dBm                   |

The 2EA M.2 module complies with the Directive 2011/65/EU (EU RoHS 2) and its amendment Directive (EU) 2015/863 (EU RoHS 3).

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