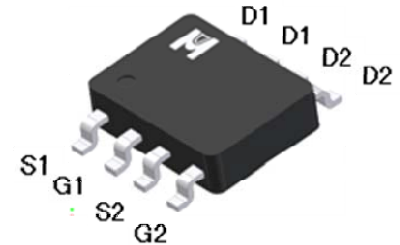
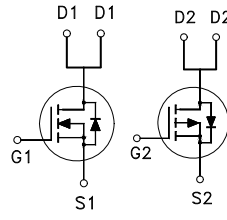


N & P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH	P-CH
$BV_{DSS}$	30V	-30V
$R_{DS(on) (MAX.)}$	17m $\Omega$	20m $\Omega$
$I_D$	10A	-8A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$  Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		$V_{GS}$	N-CH	P-CH	V
			$\pm 20$	$\pm 20$	
Continuous Drain Current	$T_C = 25^\circ\text{C}$	$I_D$	10	-8	A
	$T_C = 100^\circ\text{C}$		7	-6	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	40	-32	
Avalanche Current		$I_{AS}$	10	-10	
Avalanche Energy	L = 0.1mH, $I_D=8\text{A}$ , $R_G=25\Omega$ (N) L = 0.1mH, $I_D=-7\text{A}$ , $R_G=25\Omega$ (P)	$E_{AS}$	3.2	2.45	mJ
Repetitive Avalanche Energy <sup>2</sup>	L = 0.05mH	$E_{AR}$	1.6	1.23	
Power Dissipation	$T_C = 25^\circ\text{C}$	$P_D$	2		W
	$T_C = 100^\circ\text{C}$		0.8		
Operating Junction & Storage Temperature Range		$T_{j, T_{stg}}$	-55 to 150		$^\circ\text{C}$

100% UIS testing in condition of  $V_D=15\text{V}$ ,  $L=0.1\text{mH}$ ,  $V_G=10\text{V}$ ,  $I_L=8\text{A}$ , Rated  $V_{DS}=30\text{V}$  N-CH

100% UIS testing in condition of  $V_D=15\text{V}$ ,  $L=0.1\text{mH}$ ,  $V_G=-10\text{V}$ ,  $I_L=-7\text{A}$ , Rated  $V_{DS}=-30\text{V}$  P-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^\circ\text{C}/\text{W}$
Junction-to-Ambient <sup>3</sup>	$R_{\theta JA}$		62.5	



<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$

<sup>3</sup>62.5°C / W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.

**ELECTRICAL CHARACTERISTICS (T<sub>c</sub> = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
<b>STATIC</b>							
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	N-CH	30		V	
		V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	P-CH	-30			
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	N-CH	1	1.5	3	
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	P-CH	-1	-1.5	-3	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	N-CH			±100	
		V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	P-CH			±100	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V	N-CH			1	
		V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V	P-CH			-1	
		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C	N-CH				25
		V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125 °C	P-CH				-25
On-State Drain Current <sup>1</sup>	I <sub>D(ON)</sub>	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 10V	N-CH	10		A	
		V <sub>DS</sub> = -5V, V <sub>GS</sub> = -10V	P-CH	-8			
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A	N-CH		14.5	17	
		V <sub>GS</sub> = -10V, I <sub>D</sub> = -8A	P-CH		17.5	20	
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 6A	N-CH		21	26	
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -6A	P-CH		26	35	
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 10A	N-CH		18	S	
		V <sub>DS</sub> = -5V, I <sub>D</sub> = -8A	P-CH		24		
<b>DYNAMIC</b>							
Input Capacitance	C <sub>iss</sub>	N-CH V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V, f = 1MHz P=CH V <sub>GS</sub> = 0V, V <sub>DS</sub> = -15V, f = 1MHz	N-CH		597	pF	
			P-CH		1407		
Output Capacitance	C <sub>oss</sub>		N-CH		111		
			P-CH		208		
Reverse Transfer Capacitance	C <sub>rss</sub>	N-CH		96			
		P-CH		164			



Gate Resistance	$R_g$	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$	N-CH	2.0	$\Omega$
			P-CH	4.0	
Total Gate Charge <sup>1,2</sup>	$Q_g(V_{GS}=10V)$	N-CH $V_{DS} = 15V, V_{GS} = 10V,$ $I_D = 10A$ P-CH $V_{DS} = -15V, V_{GS} = -10V,$ $I_D = -8A$	N-CH	14	nC
	$Q_g(V_{GS}=-10V)$		P-CH	20.3	
	$Q_g(V_{GS}=4.5V)$		N-CH	7.8	
	$Q_g(V_{GS}=-4.5V)$		P-CH	9.8	
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$		N-CH	1.8	
			P-CH	3.2	
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$		N-CH	4.7	
			P-CH	4.9	
Turn-On Delay Time <sup>1,2</sup>	$t_{d(on)}$	N-CH $V_{DS} = 15V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$ P-CH	N-CH	11	nS
			P-CH	10	
Rise Time <sup>1,2</sup>	$t_r$	P-CH $V_{DS} = -15V,$ $I_D = -1A, V_{GS} = -10V, R_{GS} = 6\Omega$	N-CH	16	
			P-CH	8	
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(off)}$		N-CH	36	
			P-CH	25	
Fall Time <sup>1,2</sup>	$t_f$		N-CH	20	
			P-CH	10	
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_c = 25^\circ C</math>)</b>					
Continuous Current	$I_S$		N-CH	2.3	A
			P-CH	-2.3	
Pulsed Current <sup>3</sup>	$I_{SM}$		N-CH	9.2	
			P-CH	-9.2	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = I_S, V_{GS} = 0V$	N-CH	1.2	V
			P-CH	-1.2	
Reverse Recovery Time	$t_{rr}$		N-CH	50	nS
			P-CH	32	
Peak Reverse Recovery Current	$I_{RM(REC)}$	$I_F = I_S, di_F/dt = 100A / \mu S$	N-CH	30	A
			P-CH	-28	
Reverse Recovery Charge	$Q_{rr}$		N-CH	20	nC
			P-CH	26	

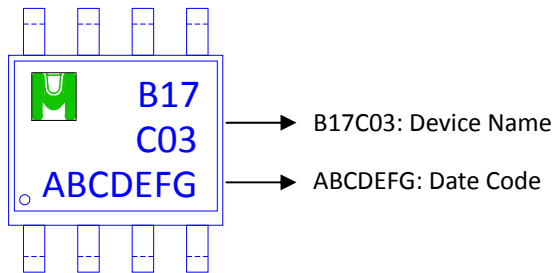
<sup>1</sup>Pulse test : Pulse Width  $\leq 300 \mu sec$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

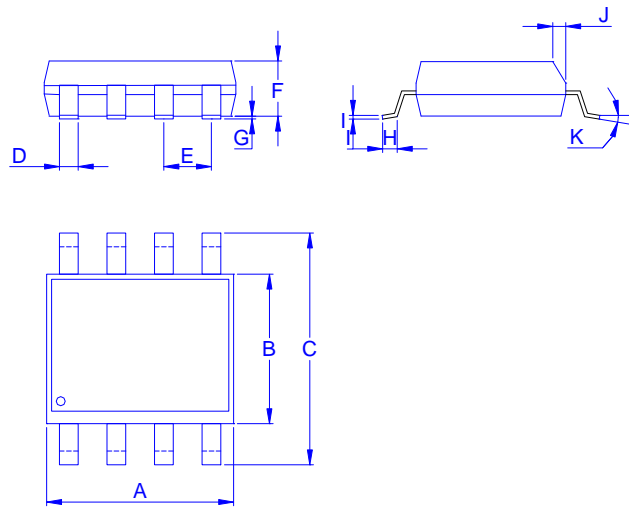
<sup>3</sup>Pulse width limited by maximum junction temperature.

### Ordering & Marking Information:

Device Name: EMB17C03G for SOP-8



### Outline Drawing

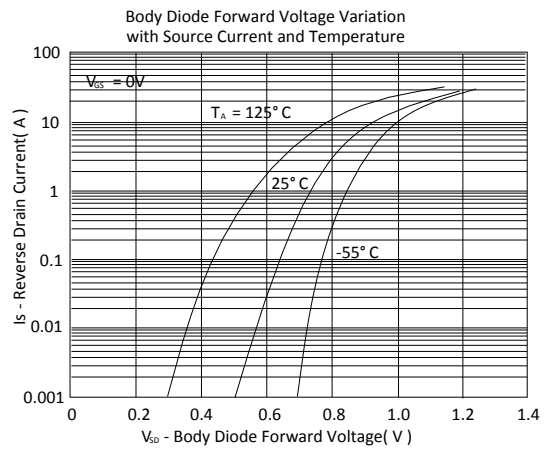
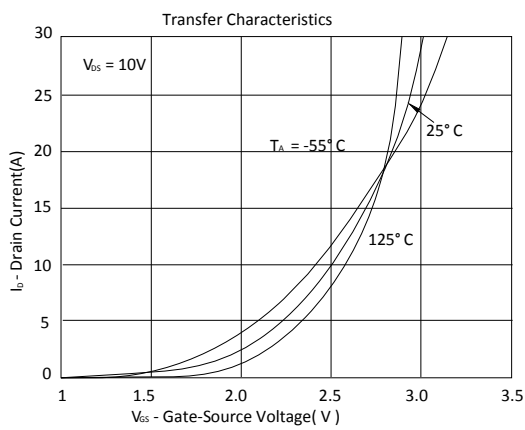
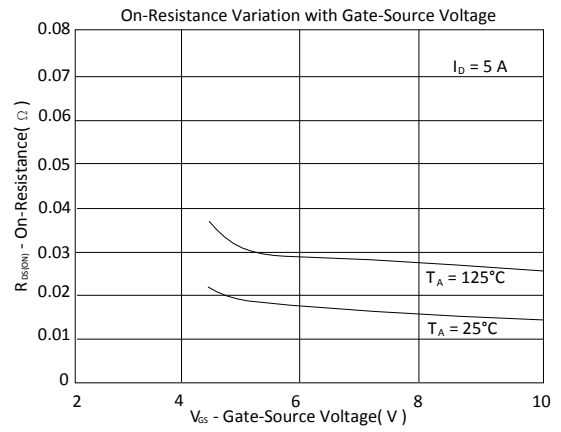
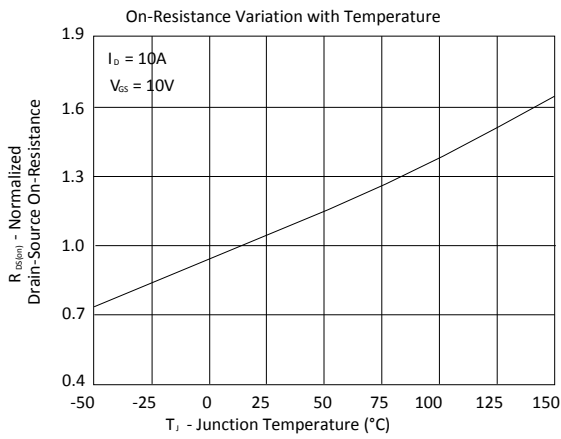
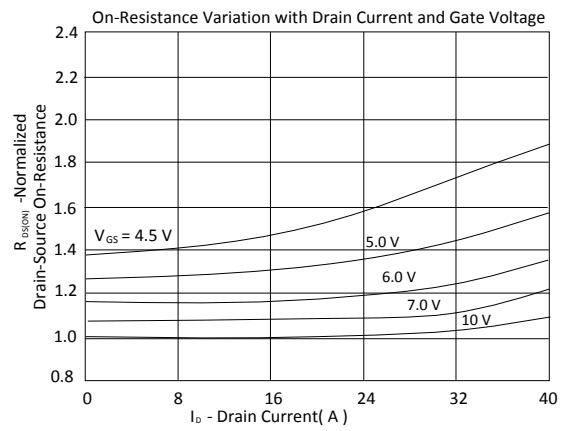
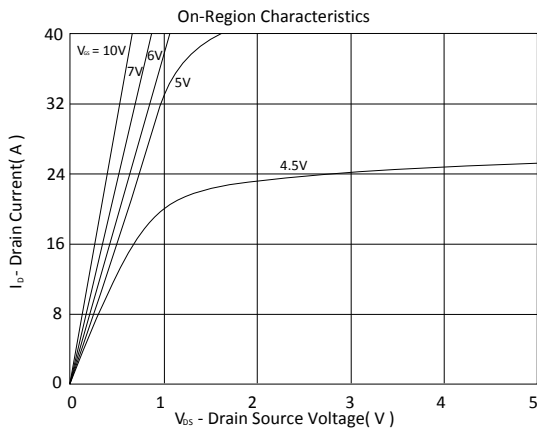


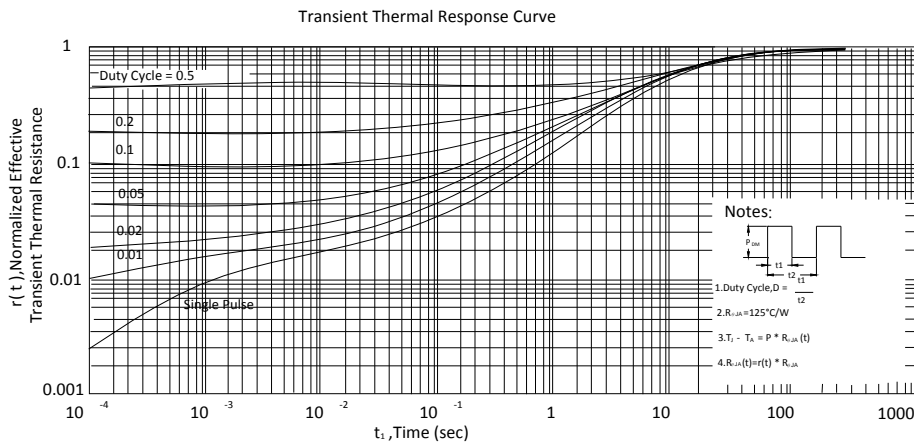
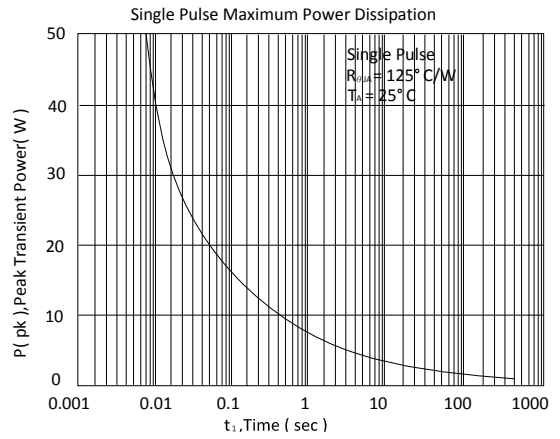
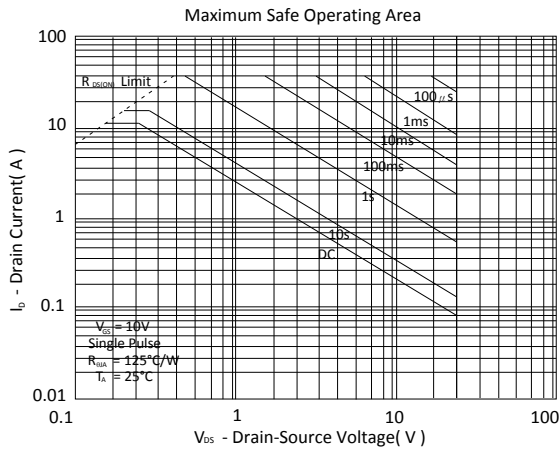
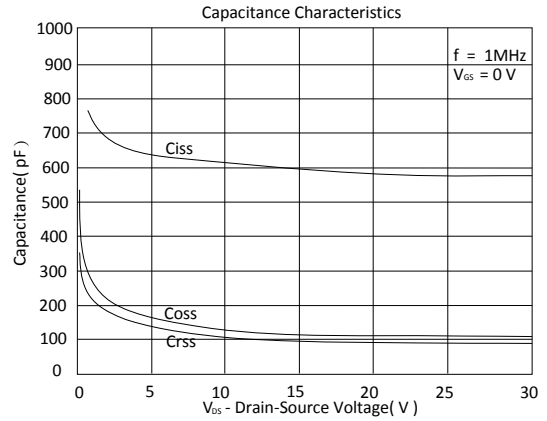
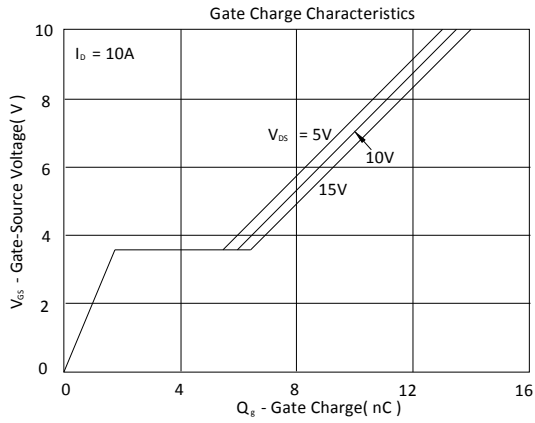
### Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°



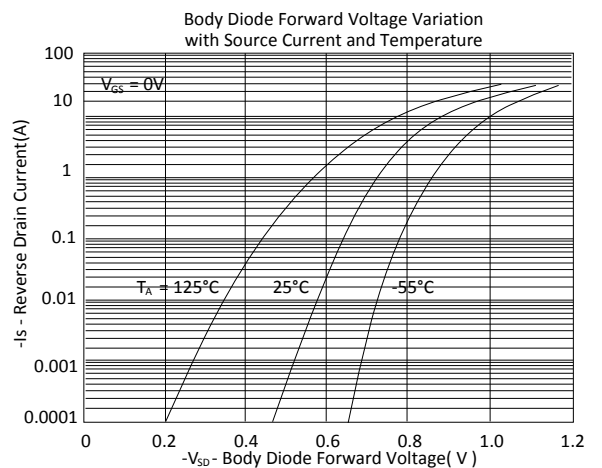
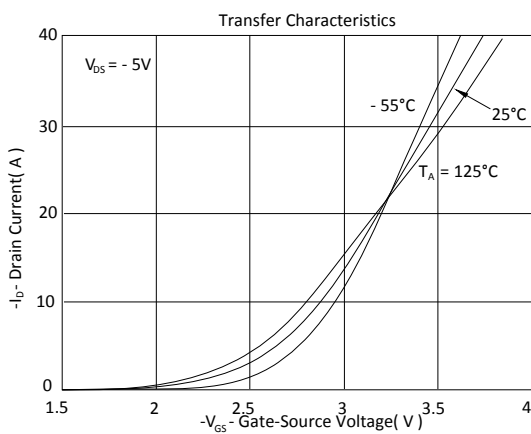
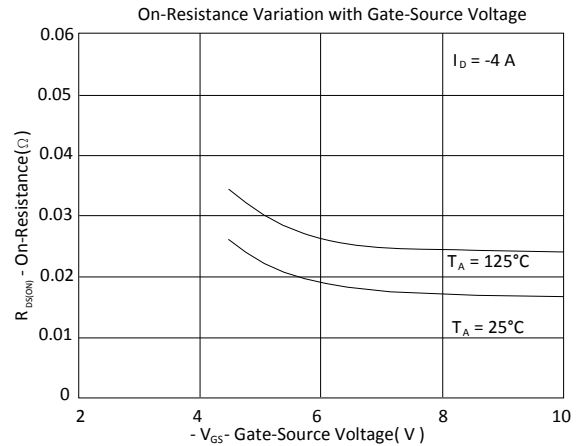
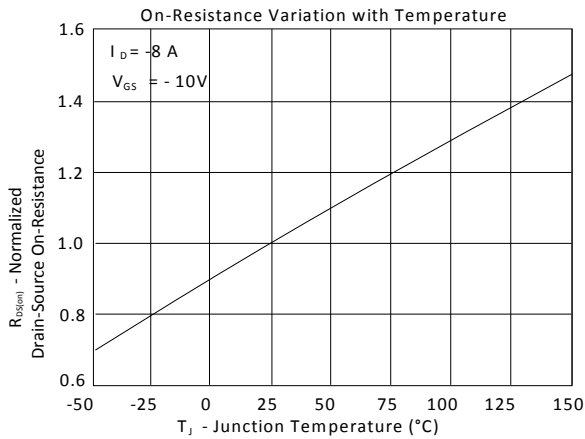
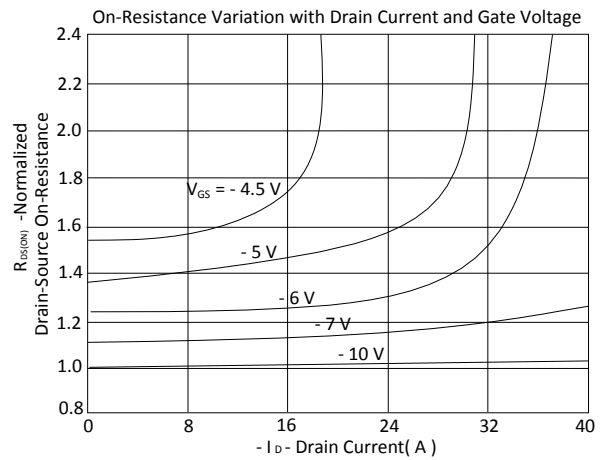
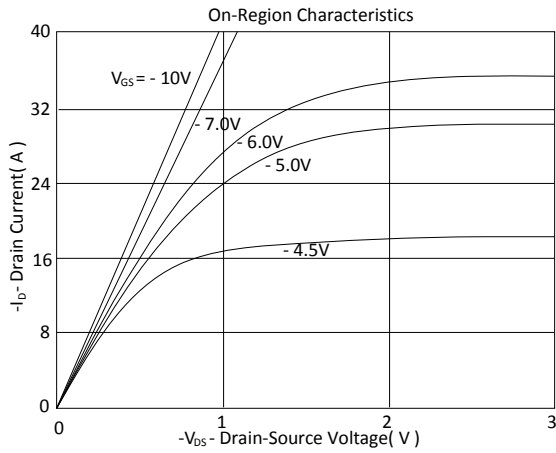
N-Channel

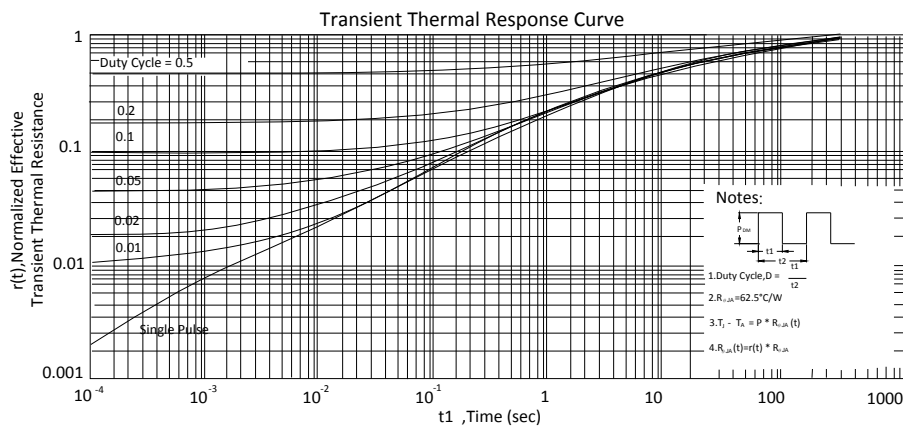
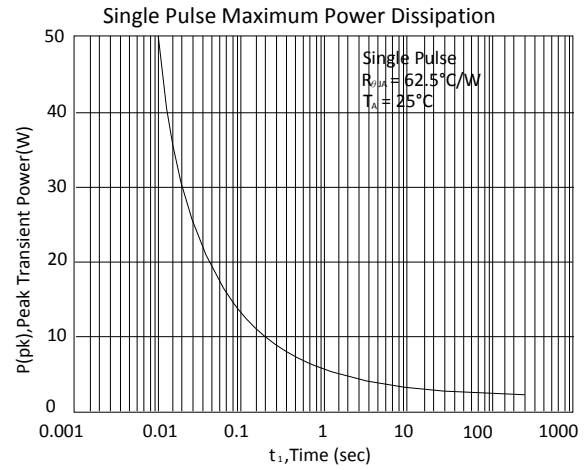
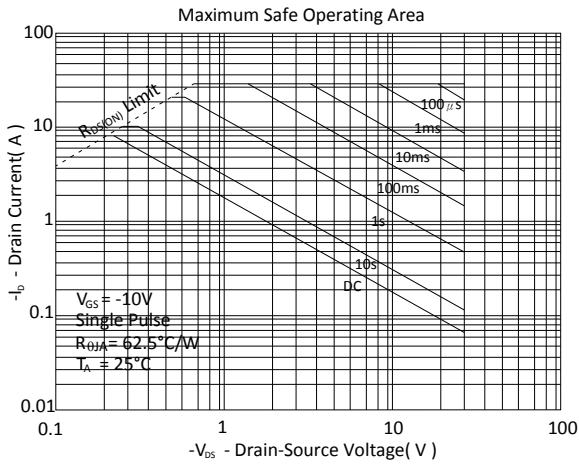
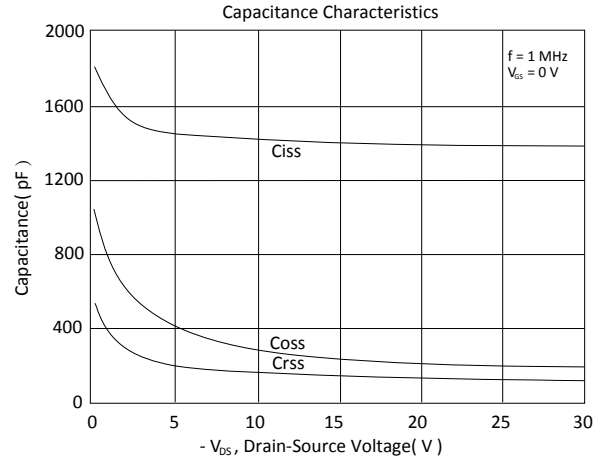
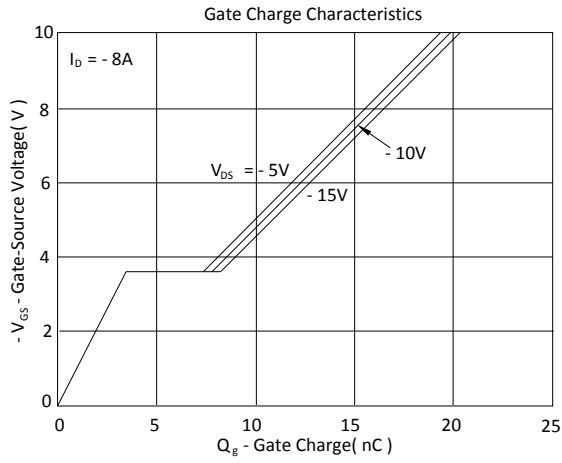






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