NOT RECOMMENDED FOR NEW DESIGN

The Altera Enpirion ES1020QI is an integrated 4-channel controlled-on/controlled-off power-supply sequencer with supply monitoring, fault protection and a "sequence completed" signal ($\overline{\text{RESET}}$). For larger systems, more than four supplies can be sequenced by simply connecting a wire between the $\overline{\text{SYSRESET}}$ pins of cascaded ICs. The ES1020QI uses a patented, micropower 7x charge pump to drive four external low-cost NFET switch gates above the supply rail by 5.3V. These ICs can be biased from 5V down to 1.5V by any supply.

External resistors provide flexible voltage threshold programming of monitored rail voltages. Delay and sequencing are provided by external capacitors for ramp-up and ramp-down.

Additional I/O is provided for indicating and driving the RESET state in various configurations.

For volume applications, other programmable options and features are available.

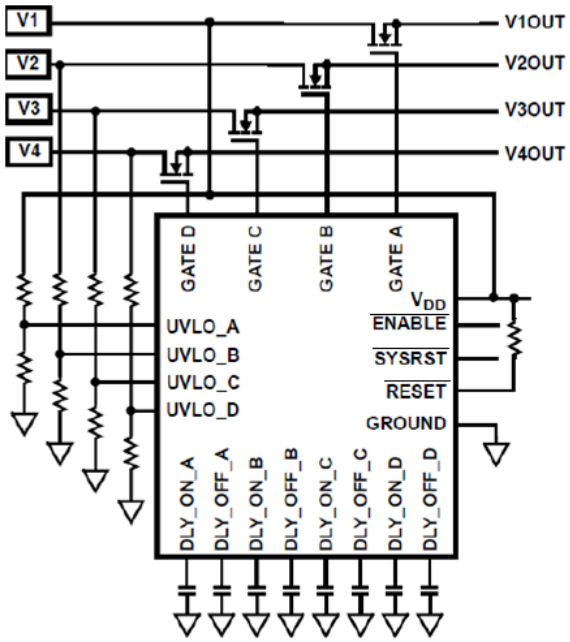


FIGURE 1. TYPICAL ES1020QI APPLICATION

Features

- Enables Arbitrary Turn-on and Turn-off Sequencing of Up to Four Power Supplies (0.7V to 5V)
- Operates From 1.5V to 5V Supply Voltage
- Supplies V_{DD} +5.3V of Charge Pumped Gate Drive
- Adjustable Voltage Slew Rate for Each Rail
- Multiple Sequencers Can be Daisy-Chained to Sequence an Infinite Number of Independent Supplies
- Glitch Immunity
- Undervoltage Lockout for Each Supply
- Low $\overline{\text{ENABLE}}$ Input
- QFN Package
- Pb-free (RoHS-compliant)

Applications

- Graphics Cards
- FPGA/ASIC/Microprocessor/PowerPC Supply Sequencing
- Network Routers
- Telecommunications Systems

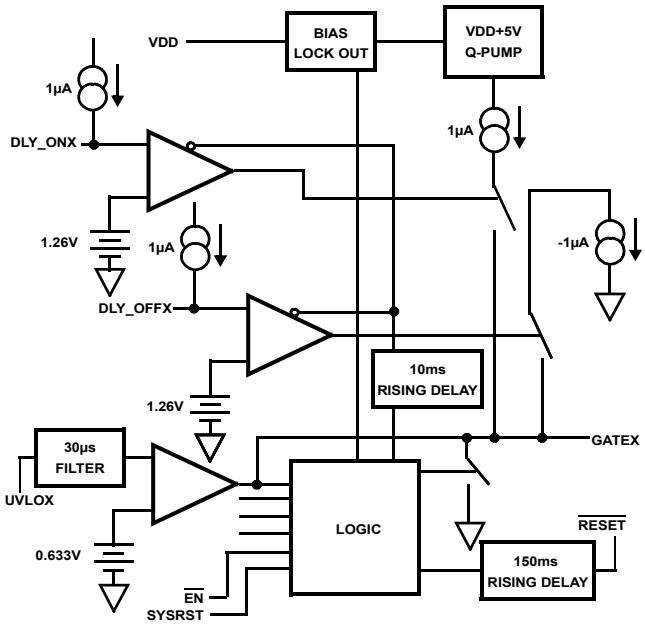


FIGURE 2. ES1020QI Block Diagram

101 Innovation Drive
San Jose, CA 95134
www.altera.com

Ordering Information

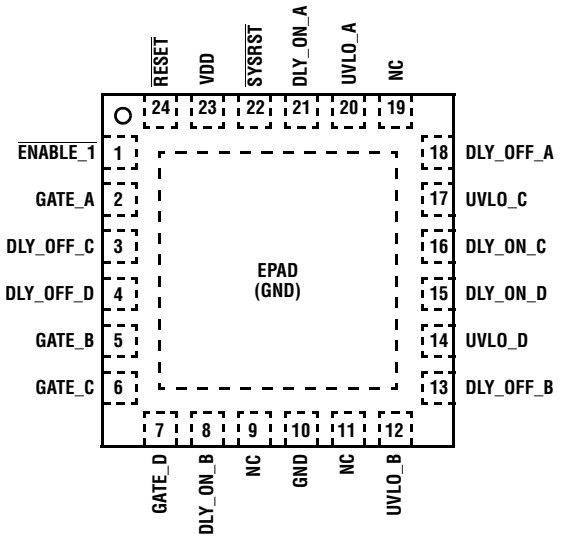
PART NUMBER (Notes 1, 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ES1020QI	S1020	-40 to +85	24 Ld 4x4 QFN	L24.4x4

NOTES:

1. Add "T" suffix for Tape and Reel. Please refer to Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html
2. These Altera Enpirion Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Altera Enpirion Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Configurations

ES1020QI
(24 LD QFN)
TOP VIEW



ES1020QI Feature Matrix

PART NAME	EN/$\overline{EN}$	CMOS/ TTL	GATE DRIVE OR OPEN DRAIN OUTPUTS	REQUIRED CONDITIONS FOR INITIAL START-UP	NUMBER OF UVLO INPUTS MONITORED BY EACH $\overline{RESET}$	NUMBER OF CHANNELS THAT TURN OFF WHEN ONE UVLO FAULTS	PRESET OR ADJUSTABLE SEQUENCE	NUMBER OF UVLO AND PAIRS OF I/O	FEATURES
ES1020QI	$\overline{EN}$	CMOS	Gate Drive	4 UVLO 1 EN	4 UVLO	4 Gates	Time Adjustable On and Off	4 Monitors with 1 I/O	Auto Restart

Pin Descriptions

PIN NAME	PIN NUMBER ES1020QI	DESCRIPTION
V_{DD}	23	Chip Bias. Bias IC from nominal 1.5V to 5V.
GND	10	Bias Return. IC ground.
$\overline{\text{ENABLE}}$_1	1	Input to start on/off sequencing. Input to initiate start of programmed sequencing of supplies on or off. Enable functionality disabled for 10ms after UVLO is satisfied.
$\overline{\text{RESET}}$	24	$\overline{\text{RESET}}$ Output. $\overline{\text{RESET}}$ provides low signal 150ms after all GATEs are fully enhanced. Delay is for stabilization of output voltages. $\overline{\text{RESET}}$ asserts low upon UVLO not being satisfied or $\overline{\text{ENABLE}}$ being deasserted. $\overline{\text{RESET}}$ outputs are open-drain, N-channel FET and are guaranteed to be in correct state for VDD down to 1V and are filtered to ignore fast transients on VDD and UVLO_X.
UVLO_A	20	Undervoltage Lockout/Monitoring Input. Provides a programmable UV lockout referenced to an internal 0.633V reference. Filtered to ignore short (<30µs) transients below programmed UVLO level.
UVLO_B	12	
UVLO_C	17	
UVLO_D	14	
DLY_ON_A	21	Gate On Delay Timer Output. Allows programming of delay and sequence for VOUT turn-on using a capacitor to ground. Each capacitor charged with 1µA 10ms after turn-on initiated by $\overline{\text{ENABLE}}$. Internal current source provides delay to associated FET GATE turn-on.
DLY_ON_B	8	
DLY_ON_C	16	
DLY_ON_D	15	
DLY_OFF_A	18	Gate Off Delay Timer Output. Allows programming of delay and sequence for VOUT turn-off through $\overline{\text{ENABLE}}$ via a capacitor to ground. Each capacitor charged with 1µA internal current source to an internal reference voltage, causing corresponding gate to be pulled down, thus turning off FET.
DLY_OFF_B	13	
DLY_OFF_C	3	
DLY_OFF_D	4	
GATE_A	2	FET Gate Drive Output. Drives external FETs with 1µA current source to soft-start ramp into load.
GATE_B	5	
GATE_C	6	
GATE_D	7	
$\overline{\text{SYSRST}}$	22	System Reset I/O. As an input, allows for immediate and unconditional latch-off of all GATE outputs when driven low. This input can also be used to initiate programmed sequence with ‘zero’ wait (no 10ms stabilization delay) from input signal on this pin being driven high to first GATE. As an output, when there is a UV condition, this pin pulls low. If common to other $\overline{\text{SYSRST}}$ pins in a multiple IC configuration, it causes immediate and unconditional latch-off of all other GATEs on all other ES1020QI sequencers.
GND	EPAD	Ground. Die Substrate. Can be left floating.
NC	9, 11, 19	No Connect

Absolute Maximum Ratings (Note 5)

V_{DD} . . . . . +6.0V
GATE . . . . . -0.3V to V_{DD}+6V
UVLO, $\overline{ENABLE}$, $\overline{SYSRST}$. . . . . .-0.3V to V_{DD} + 0.3V
$\overline{RESET}$, DLY_ON, DLYOFF. . . . . .-0.3V to V_{DD} + 0.3V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld 4x4 QFN Package (Notes 3, 4)	46	8

Maximum Junction Temperature . . . . . +125°C
Maximum Storage Temperature Range . . . . . .-65°C to +150°C

Operating Conditions

V_{DD} Supply Voltage Range . . . . . .+1.5V to +5.5V
Temperature Range (T_A) . . . . . .-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
5. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

V_{DD} = 1.5V to +5V, T_A = T_J = -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
UVLO						
Falling Undervoltage Lockout Threshold	$V_{UVLOvth}$	T_J = +25°C	619	633	647	mV
Undervoltage Lockout Threshold Tempco	$TC_{UVLOvth}$			40		µV/°C
Undervoltage Lockout Hysteresis	$V_{UVLOhys}$			10		mV
Undervoltage Lockout Threshold Range	RUVLOvth	Max $V_{UVLOvth}$- Min $V_{UVLOvth}$		7		mV
Undervoltage Lockout Delay	TUVLOdel	$\overline{ENABLE}$ satisfied		10		ms
Transient Filter Duration	t_{FIL}	V_{DD}, UVLO, $\overline{ENABLE}$ glitch filter		30		µs
DELAY ON/OFF						
Delay Charging Current	DLY_ichg	V_{DLY} = 0V	**0.92**	1	**1.08**	µA
Delay Charging Current Range	DLY_ichg_r	DLY_ichg(max) - DLY_ichg(min)		0.08		µA
Delay Charging Current Temperature Coefficient	TC_DLY_ichg			0.2		nA/°C
Delay Threshold Voltage	DLY_Vth		**1.238**	1.266	**1.294**	V
Delay Threshold Voltage Temperature Coefficient	TC_DLY_Vth			0.2		mV/°C
$\overline{ENABLE}$, $\overline{RESET}$ AND $\overline{SYSRST}$ I/O						
$\overline{ENABLE}$ Threshold	V_{ENh}			0.5 V_{DD}		V
$\overline{ENABLE}$ Hysteresis	V_{ENh} .V_{ENl}	Measured at V_{DD} = 1.5V		0.2		V
$\overline{ENABLE}$ Lockout Delay	t_{delEN_LO}	UVLO satisfied		10		ms
$\overline{ENABLE}$ Input Capacitance	Cin_en			5		pF
$\overline{RESET}$ Pull-up Voltage	Vpu_rst			V_{DD}		V
$\overline{RESET}$ Pull-Down Current	$I_{\overline{RST}pd1}$	V_{DD} = 1.5V, $\overline{RST}$ = 0.1V		5		mA
	$I_{\overline{RST}pd3}$	V_{DD} = 3.3V, $\overline{RST}$ = 0.1V		13		mA
	$I_{\overline{RST}pd5}$	V_{DD} = 5V, $\overline{RST}$ = 0.1V		17		mA
$\overline{RESET}$ Delay after GATE High	$T_{\overline{RST}del}$	GATE = V_{DD}+5V		160		ms

Electrical Specifications V_{DD} = 1.5V to +5V, $T_A = T_J$ = -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
$\overline{\text{RESET}}$ Output Low	$V_{\overline{RST}l}$	Measured at V_{DD} = 5V with 5k pull-up resistors			**0.1**	V
$\overline{\text{RESET}}$ Output Capacitance	C_{OUT_RST}			10		pF
$\overline{\text{SYSRST}}$ Pull-Up Voltage	Vpu_srst			V_{DD}		V
$\overline{\text{SYSRST}}$ Pull-Down Current	Ipu_1.5	V_{DD} = 1.5V		5		µA
	Ipu_5	V_{DD} = 5V		100		µA
$\overline{\text{SYSRST}}$ Low Output Voltage	Vol_srst	V_{DD} = 1.5V, I_{OUT} = 100µA		150		mV
$\overline{\text{SYSRST}}$ Output Capacitance	Cout_srst			10		pF
$\overline{\text{SYSRST}}$ Low to GATE Turn-Off	t_{delSYS_G}	GATE = 80% of V_{DD} + 5V		40		ns
GATE						
GATE Turn-On Current	I_{GATEon}	GATE = 0V	**0.8**	1.1	**1.4**	µA
GATE Turn-Off Current	$I_{GATEoff\_l}$	GATE = V_{DD}, Disabled	**-1.4**	-1.05	**-0.8**	µA
GATE Current Range	I_{GATE_range}	Within IC I_{GATE} max-min			**0.35**	µA
GATE Turn-On/Off Current Temperature Coefficient	TC_I_{GATE}			0.2		nA/°C
GATE Pull-Down High Current	$I_{GATEoff\_h}$	GATE = V_{DD}, UVLO = 0V		88		mA
GATE High Voltage	V_{GATEh}	V_{DD} < 2V, T_J = +25°C		V_{DD} + 4.9V		V
	V_{GATEh}	V_{DD} > 2V	**V_{DD} + 5V**	V_{DD} + 5.3V		V
GATE Low Voltage	V_{GATEl}	Gate Low Voltage, V_{DD} = 1V		0	**0.1**	V
BIAS						
IC Supply Current	I_{VDD_5V}	V_{DD} = 5V		0.20	**0.5**	mA
	$I_{VDD\_3.3V}$	V_{DD} = 3.3V		0.14		mA
	$I_{VDD\_1.5V}$	V_{DD} = 1.5V		0.10		mA
V_{DD} Power-on Reset	V_{DD}_POR				**1**	V

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

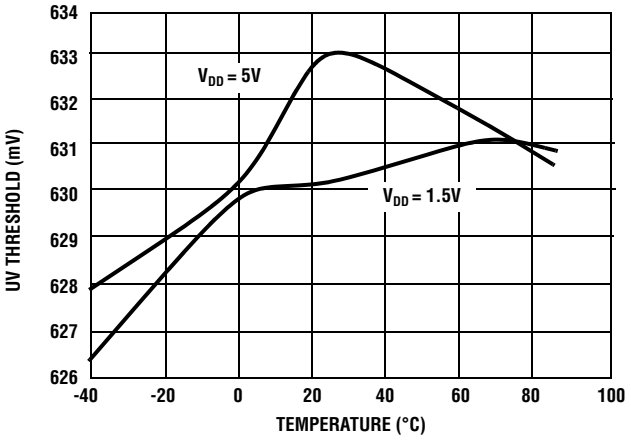


FIGURE 3. UVLO THRESHOLD VOLTAGE

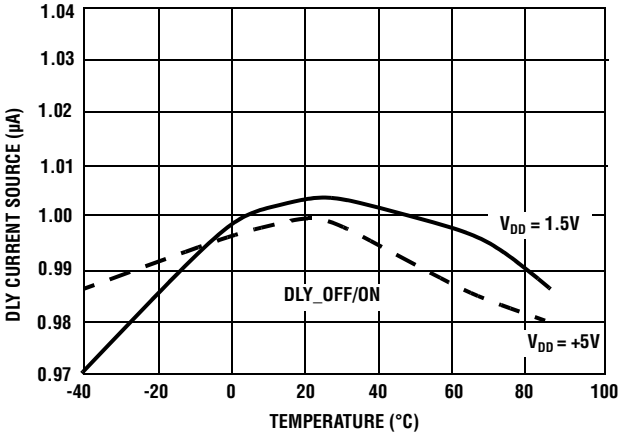


FIGURE 4. DLY CHARGE CURRENT

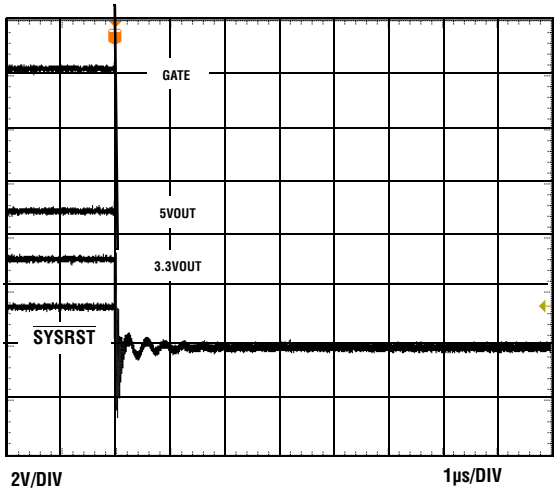


FIGURE 5. $\overline{\text{SYSRST}}$ LOW TO OUTPUT LATCH-OFF

Descriptions and Operation

The ES1020QI sequencer is a 4-channel voltage sequencing controller, and is designed for use in multiple-voltage systems requiring power sequencing of various supply voltages. Individual voltage rails are gated on and off by external N-Channel MOSFETs, the gates of which are driven by an internal charge pump to V_{DD} + 5.3V (VQP) in a user-programmed sequence.

The 4-channel ES1020QI $\overline{\text{ENABLE}}$ must be asserted low, and all four voltages to be sequenced must be above their respective user-programmed undervoltage lockout (UVLO) levels before programmed output turn-on sequencing can begin. Sequencing order and delay are determined by the choice of external capacitor values on the DLY_ON and DLY_OFF pins. Once all four UVLO inputs and $\overline{\text{ENABLE}}$ are satisfied for 10ms (t_{delEN_LO}), the four DLY_ON capacitors are simultaneously charged with 1µA current sources to the DLY_Vth level of 1.27V. As each DLY_ON pin reaches the DLY_Vth level, its associated GATE turns on, with a 1µA source current to the charge pump voltage (VQP) of V_{DD} + 5.3V. Thus, all four GATEs sequentially turn on in the user defined order. Once at DLY_Vth, the DLY_ON pins discharge so they are ready when next needed.

After the entire turn-on sequence has been completed and all GATEs have reached the charge pumped voltage (VQP), a 160ms delay ($T_{\overline{RST}del}$) is started to ensure stability, after which the $\overline{\text{RESET}}$ output is released to go high.

After turn-on, if any input falls below its UVLO point for longer than the glitch filter period (~30µs), it is considered a fault. $\overline{\text{RESET}}$ and $\overline{\text{SYSRST}}$ are pulled low, and all GATEs are simultaneously also pulled low. In this mode, the GATEs are pulled low with 88mA.

Normal shutdown mode is entered when no UVLO is violated and $\overline{\text{ENABLE}}$ is deasserted. When $\overline{\text{ENABLE}}$ is deasserted, $\overline{\text{RESET}}$ is immediately asserted and pulled low. Next, all four shutdown ramp capacitors on the DLY_OFF pins are charged with a 1µA source. When any ramp-capacitor reaches DLY_Vth, a latch is set, and a current is sunk on the respective GATE pin to turn off its external MOSFET. When the GATE voltage is approximately 0.6V, the GATE is pulled down the rest of the way at a higher current level. Each individual external FET is thus turned off, which removes the voltages from the load in the user programmed sequence.

Table 1 shows the nominal time delay on the DLY_X pins for various capacitor values, from the start of charging to the 1.27V reference. This table does not include the 10ms of $\overline{\text{ENABLE}}$ lockout delay during a start-up sequence, but it does represent the time from the end of the $\overline{\text{ENABLE}}$ lockout delay to the start of GATE transition. There is no $\overline{\text{ENABLE}}$ lockout delay for a sequence-off, so this table illustrates the delay to GATE transition from a disable signal.

TABLE 1. NOMINAL DELAY TO SEQUENCING THRESHOLD

DLY PIN CAPACITANCE	TIME(s)
Open	0.00006
100pF	0.00013
1000pF	0.0013
0.01µF	0.013
0.1µF	0.13
1µF	1.3
10µF	13

NOTE: Nom. T_{DEL_SEQ} = Capacitor (µF)*1.3MΩ

Figure 6 shows the turn-on and Figure 7 shows the nominal turn-off timing diagram of the ES1020QI.

Delay and flexible sequencing possibilities include multiple series, parallel, or adjustable capacitors that can be used to easily fine-tune timing over that offered by standard value capacitors.

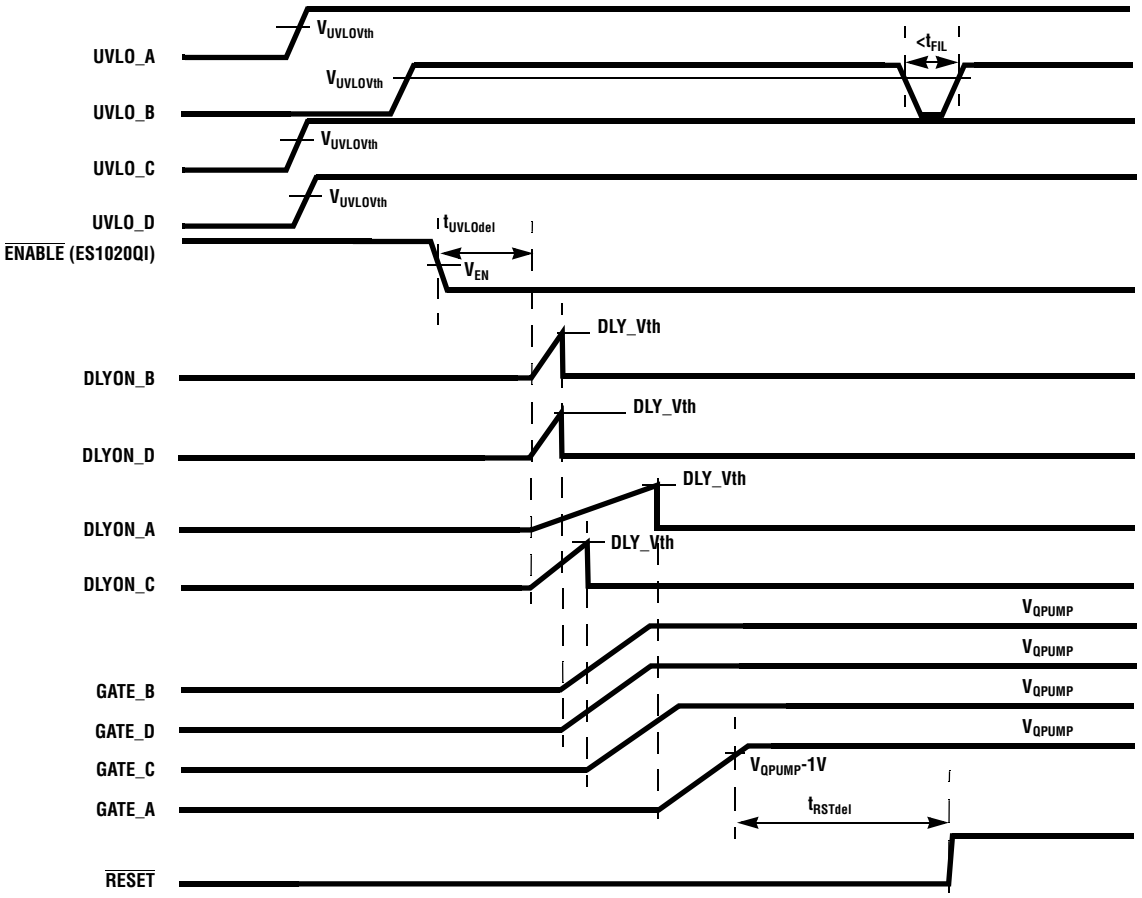


FIGURE 6. ES1020QI TURN-ON AND GLITCH RESPONSE TIMING DIAGRAM

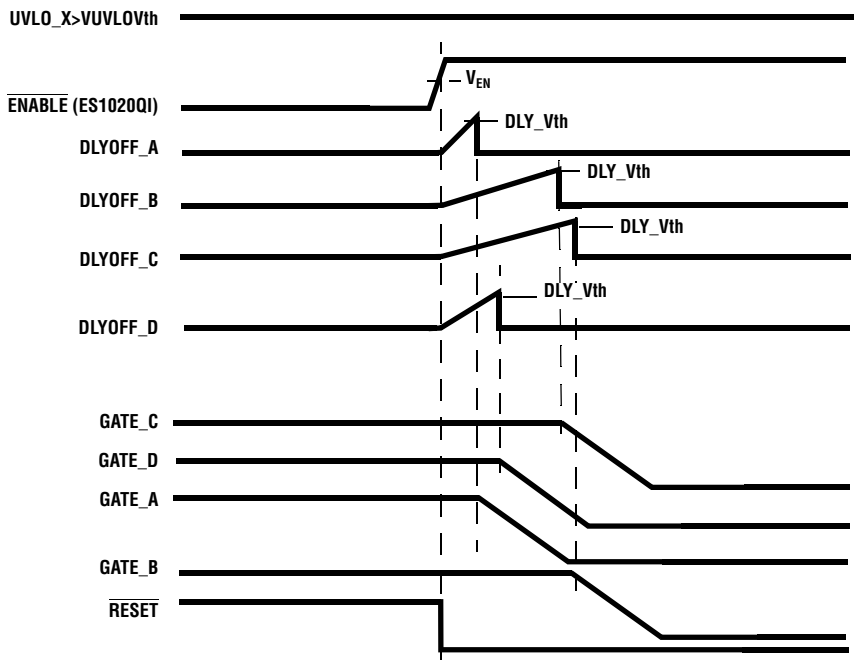


FIGURE 7. ES1020QI TURN-OFF TIMING DIAGRAM

Typical Performance Waveforms

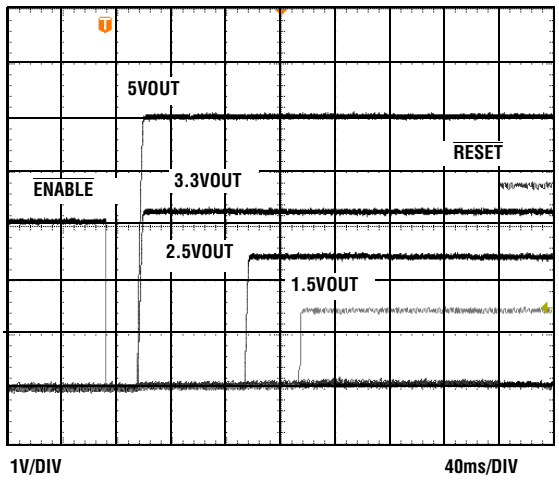


FIGURE 8. ES1020QI SEQUENCED TURN-ON

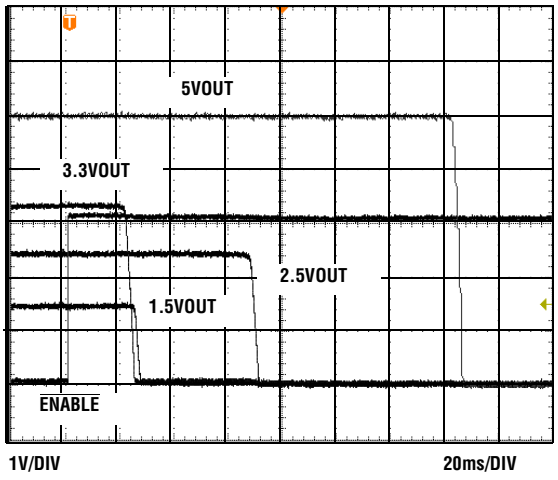


FIGURE 9. ES1020QI SEQUENCED TURN-OFF

Application Considerations

Timing Error Sources

In any system there are variance contributors. For the ES1020QI, timing errors are mainly contributed by three sources.

Capacitor Timing Mismatch Error

Obviously, the absolute capacitor value is an error source; thus, lower-percentage tolerance capacitors help to reduce this error source. Figure 10 illustrates a difference of 0.57ms between two DLY_X outputs ramping to DLY_X threshold voltage. These 5% capacitors were from a common source. In applications where two or more GATEs or LOGIC outputs must have concurrent transitions, it is recommended that a common GATE drive be used to eliminate this timing error.

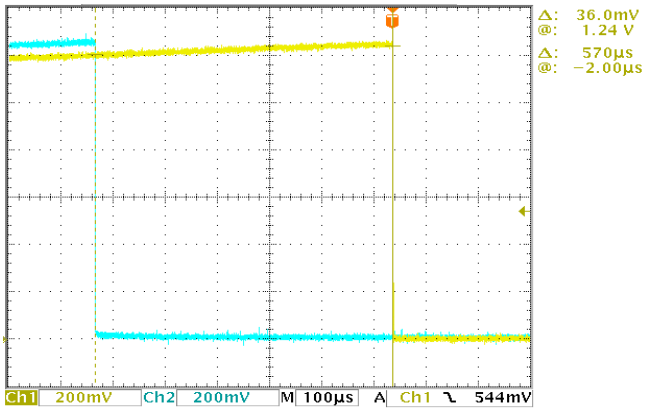


FIGURE 10. CAPACITOR TIMING MISMATCH

DLY_X Threshold Voltage and Charging Current Mismatch

The two other error sources come from the IC itself and are found across the four DLY_X outputs. These errors are the DLY_X threshold voltage (DLY_Vth) variance when the GATE_X charging and discharging current latches are set, and the DLY_X charging current (DLY_ichg) variances to determine the time to next sequencing event. Both of these parameters are bounded by specification. Figure 11 shows that, with a common capacitor, the typical error contributed by these factors is insignificant, since both DLY_X traces overlay each other.

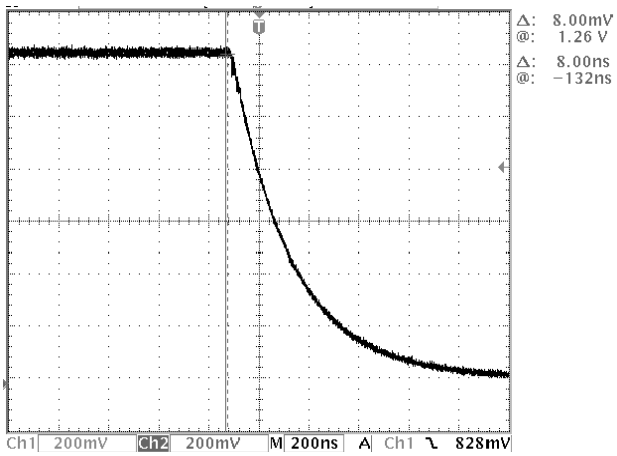


FIGURE 11. DLY_VTH AND DLY_ICHG TIMING MISMATCH

Revision History

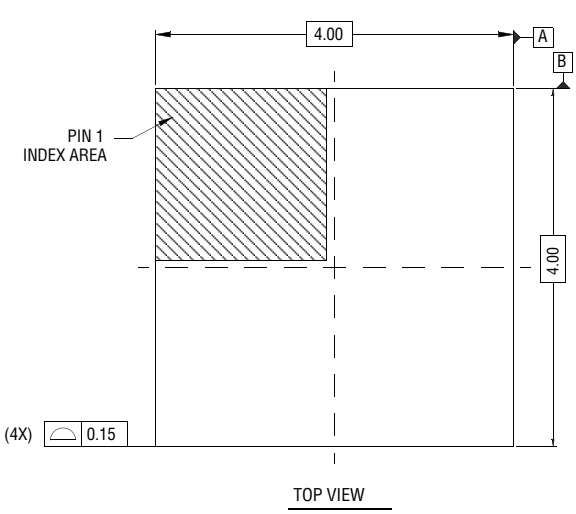
The table lists the revision history for this document.

DATE	REVISION	CHANGE
May, 2014	A	Initial release.

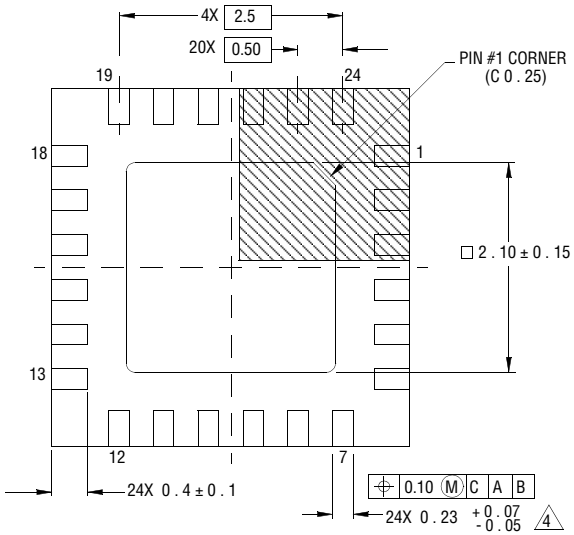
Package Outline Drawing

L24.4x4

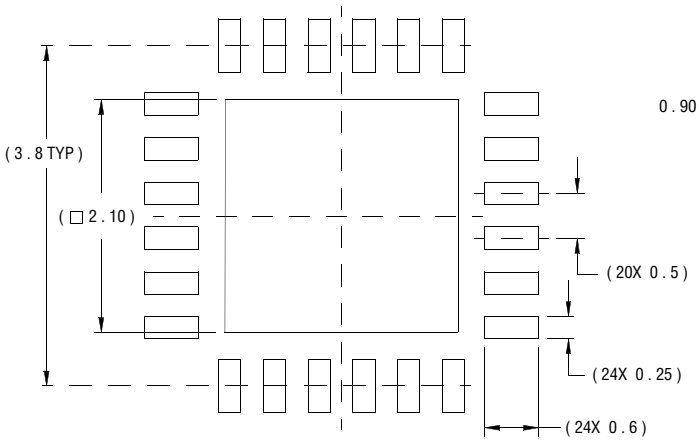
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 10/06



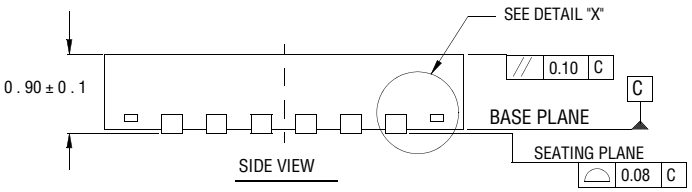
TOP VIEW



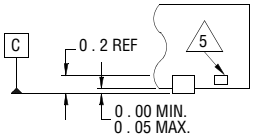
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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