EN5335QI 3A PowerSoC

Step-Down DC-DC Switching Converter with Integrated Inductor

DESCRIPTION

The EN5335QI is an Intel® Enpirion® Power System on a Chip (PowerSoC) DC-DC converter. It is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, memory boards and system level applications in a distributed power architecture.

Advanced circuit techniques, ultra high switching frequency, and very advanced, high-density, integrated circuit and proprietary inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion. Operating this converter requires as few as three external components that include small value input and output ceramic capacitors and a soft-start capacitor.

The Intel Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of vendors required for the complete power solution helps to enable an overall system cost savings.

All Intel Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

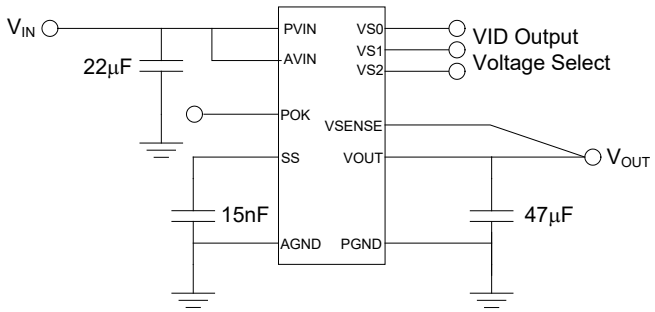


Figure 1: Simplified Applications Circuit

FEATURES

- Integrated INDUCTOR, MOSFETS, Controller
- Footprint 1/3rd that of competing solutions
- Low Part Count: only 3 MLC Capacitors
- Up to 10W continuous output power
- 5MHz operating frequency
- High efficiency, up to 93%
- VOUT accuracy 3% over line, load and temp
- Wide input voltage range of 2.375V to 6.6V
- 3-pin VID output voltage select to choose one of 7 pre-programmed voltage levels
- Output enable pin and Power OK signal
- Programmable soft-start time
- Programmable over-current protection
- Thermal shutdown, short circuit, and UVLO
- Output over-voltage protection
- RoHS compliant, MSL level 3, 260C reflow

APPLICATIONS

- Point of load regulation for low-power processors, network processors, DSPs, FPGAs, and ASICs
- Notebook computers, servers, workstations
- Broadband, networking, LAN/WAN, optical
- Low voltage, distributed power architectures with 2.5V, 3.3V or 5V rails
- DSL, STB, DVR, DTV, iPC
- Ripple sensitive application

ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
EN5335QI	EN5335QI	-40°C to +125°C	44-pin (7.5mm x 10mm x 1.85mm) QFN
EN5335QI-E	EN5335QI	QFN Evaluation Board	

Packing and Marking Information: https://www.intel.com/support/quality-and-reliability/packing.html

PIN FUNCTIONS

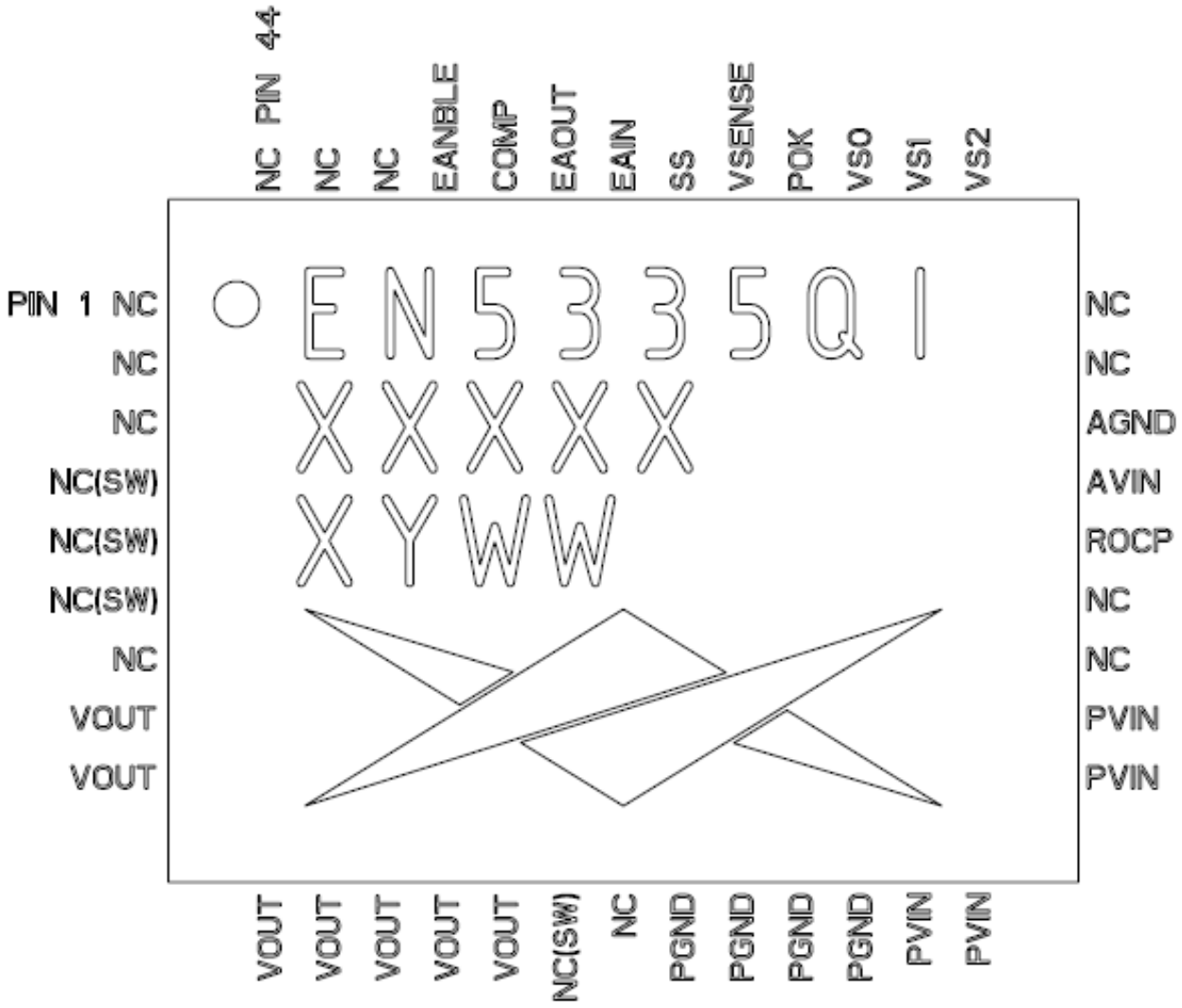


Figure 2: Pin Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1-3, 7, 16, 25-26, 30-31, 42-44	NC	-	NO CONNECT – Do not electrically connect these pins to each other or to PCB.
4-6, 15	N(SW)	-	No Connect. These pins are internally connected to the switch node of the internal MOSFETs. NC(SW) pins are not to be electrically connected to any external signal, ground, or voltage.
8-14	VOUT	Power	Regulated converter output. Connect these pins to the load and place output capacitor from these pins the PGND pins 17-18
17-20	PGND	Power	Output power ground. Connect these pins to the ground electrode of the output filter capacitors. Refer to layout guideline section.
21-24	PVIN	Power	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND (pins 19-20).
25-26	VFB	Analog	This is the external feedback input pin. A resistor divider connects from the output to AGND. The mid-point of the resistor divider is connected to VFB. A feed-forward capacitor is required parallel to the upper feedback resistor (R_A). The output voltage regulation is based on the VFB node voltage equal to 0.600V.
27	ROCP	Analog	Optional Over Current Protection adjust pin. Place ROCP resistor between this pin and AGND (pin 40) to increase the over current trip point by 50%.
28	AVIN	Power	Analog voltage input for the controller circuits. Connect this pin to the input power supply.
29	AGND	Power	Analog ground for the controller circuits.
32	VS2	Digital	Voltage select line 2 input. See Table 1.
33	VS1	Power	Voltage select line 1 input. See Table 1.
34	VS0	Ground	Voltage select line 0 input. See Table 1.
35	POK	Analog	Power OK is an open drain transistor for power system state indication. POK is a logic high when VOUT is with -10% to +20% of VOUT nominal.
36	VSENSE	Analog	Remote voltage sense input. Connect this pin to the load voltage at the point to be regulated.
37	SS	Analog	Soft-Start node. The soft-start capacitor is connected between this pin and AGND. The value of this resistor determines the startup timing.
38	EAIN	Analog	Optional Error Amplifier input. Allows for customization of the control loop.
39	EAOUT	Analog	Optional Error Amplifier output. Allows for customization of the control loop.

PIN	NAME	TYPE	FUNCTION
40	COMP	Analog	Optional Error Amplifier Buffer output. Allows for customization of the control loop.
41	ENABLE	Analog	Input Enable. Applying a logic high, enables the output and initiates a soft-start. Applying a logic low disables the output.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
VIN, VOUT		-0.3	7.0	V
ENABLE, VSENSE		-0.3	V_{IN}+0.3	V
VS0-VS2[1]		-0.3	2.7	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Ambient Temperature Range		-40	+85	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V
CDM (Charged Device Model)		±500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range (for output voltages < 1.2V)	V_{IN}	2.375	5.5	V
Input Voltage Range (for output voltages ≥ 1.2V)	V_{IN}	2.375	6.6	V
Output Current Range	I_{OUT}		3	A
Operating Ambient Temperature Range	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	150	°C
Thermal Shutdown Hysteresis	T_{SDHYS}	15	°C
Thermal Resistance: Junction to Ambient (0 LFM)	θ_{JA}	25	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	3	°C/W

ELECTRICAL CHARACTERISTICS

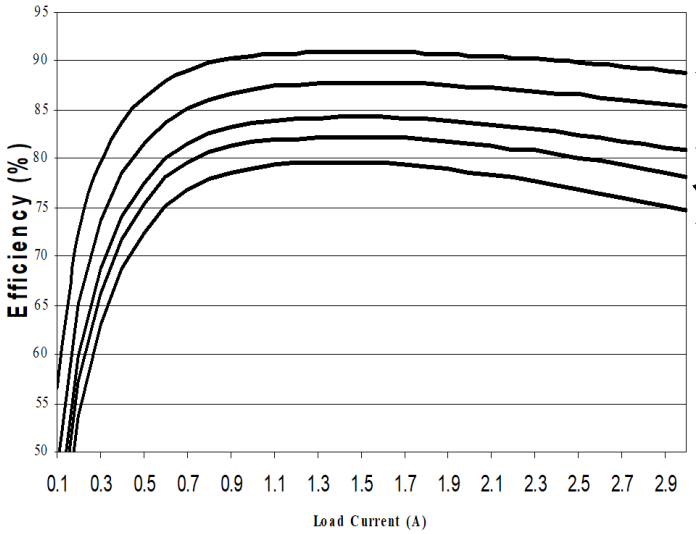
NOTE: V_{IN} = 5V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage (for output voltages < 1.2V)	V_{IN}		2.375		5.5	V
Operating Input Voltage (for output voltages ≥ 1.2V)	V_{IN}		2.375		6.6	V
V_{OUT} Initial Accuracy	ΔV_{OUT_INIT}	T_A = 25C, V_{IN} = 5.0V, I_{LOAD} = 0A; • All VID Settings except 0.8V • 0.8V	-2 -3		+2 +2	%
Drop out voltage	V_{IN} - V_{OUT}	Drop out voltage at full load			600	mV
Shut-Down Supply Current	I_S	ENABLE=0V		100		µA
Switching Frequency	F_{OSC}			5		MHz
Output Voltage Regulation	V_{OUT}	Over line, load and temperature VID Output Voltage Setting (V): 1.2, 1.25, 1.5, 1.8, 2.5, 3.3 0.8V	 -3.0 -4.0		 3.0 4.0	%
Over Current Trip Piont	I_{OCP}			4.5		A
Disable Threshold	$V_{DISABLE}$	Max voltage to ensure the converter is disabled			0.8	V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Enable Threshold	V_{ENABLE}	2.375V ≤ V_{IN} ≤ 5.5V 5.5V < V_{IN}	1.8 2.0			V
Enable Pin Current	I_{ENABLE}	V_{IN} = 5.5V		50		µA
VS_X Logic Low Threshold	V_{SX-Low}	Threshold voltage for Logic Low			0.8	V
VS_X Logic High Threshold	$V_{SX-High}$	Threshold voltage for Logic High (internally pulled high; can be left floating to achieve logic high)	1.8		V_{IN}	V
VS_X Pin Current	I_{VSX}	(V_{IN} = 5.5V) VSx = GND VSx = V_{IN} VSx = Open		50 0 0		µA
POK low voltage	V_{POK}	I_{POK} = 4mA (sink current)			0.4	V
Max POK Voltage	V_{POK}				V_{IN}	V

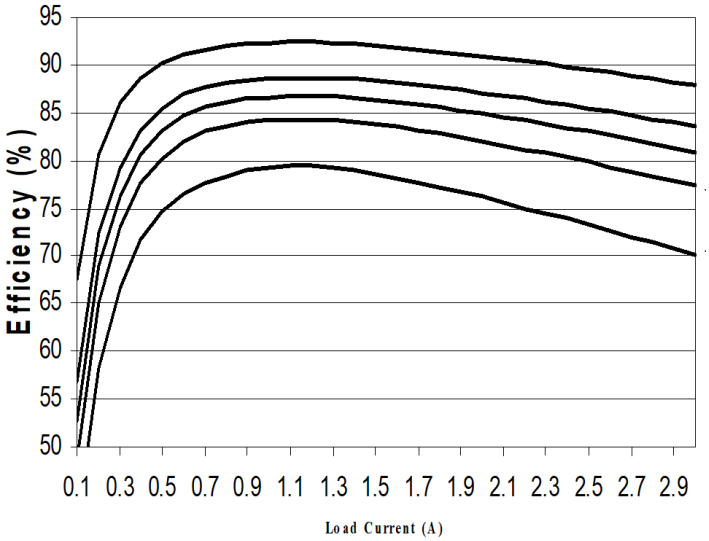
(1) V_{S0}-V_{S2} pins have an internal pull-up resistor, only ground potentials should be placed on them as required.

TYPICAL PERFORMANCE CURVES



Efficiency versus Load, VIN = 5.0V

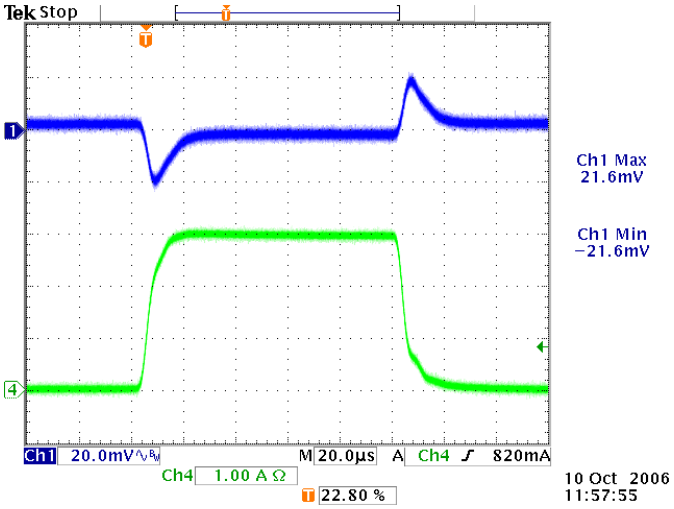
Top to Bottom: V_{OUT} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V



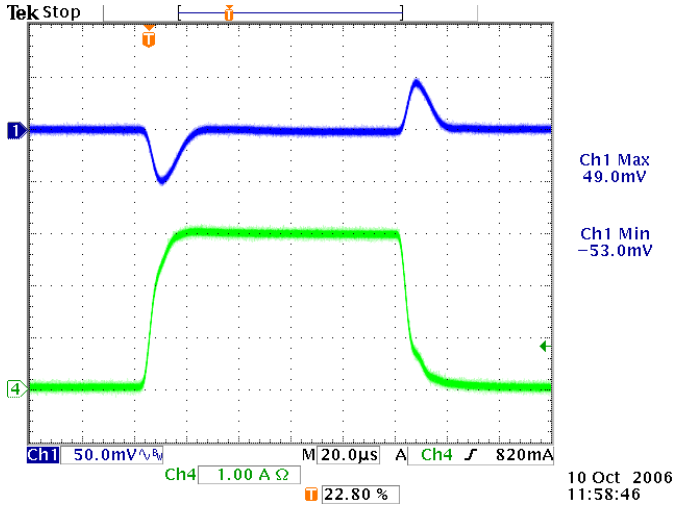
Efficiency versus Load, VIN = 3.3V

Top to Bottom: V_{OUT} = 2.5V, 1.8V, 1.5V, 1.2V, 0.8V

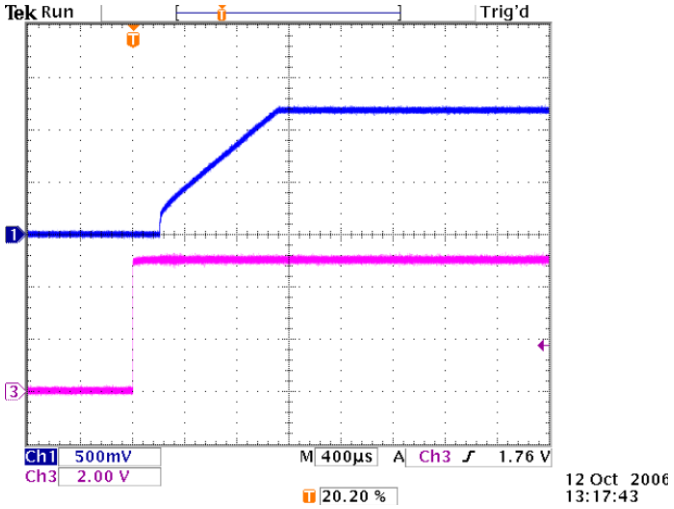
TYPICAL PERFORMANCE CHARACTERISTICS



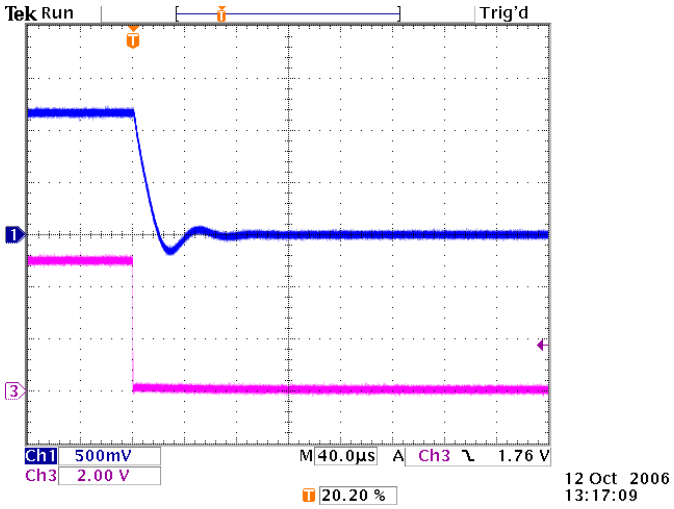
Load transient, 0 – 3A, V_{IN}/V_{OUT} = 5.5V/1.2V



Load transient, 0 – 3A, V_{IN}/V_{OUT} = 5.5V/3.3V



Start-up waveform, V_{IN}/V_{OUT} = 5.5V/1.2V



Shut-down waveform, V_{IN}/V_{OUT} = 5.5V/1.2V

FUNCTIONAL BLOCK DIAGRAM

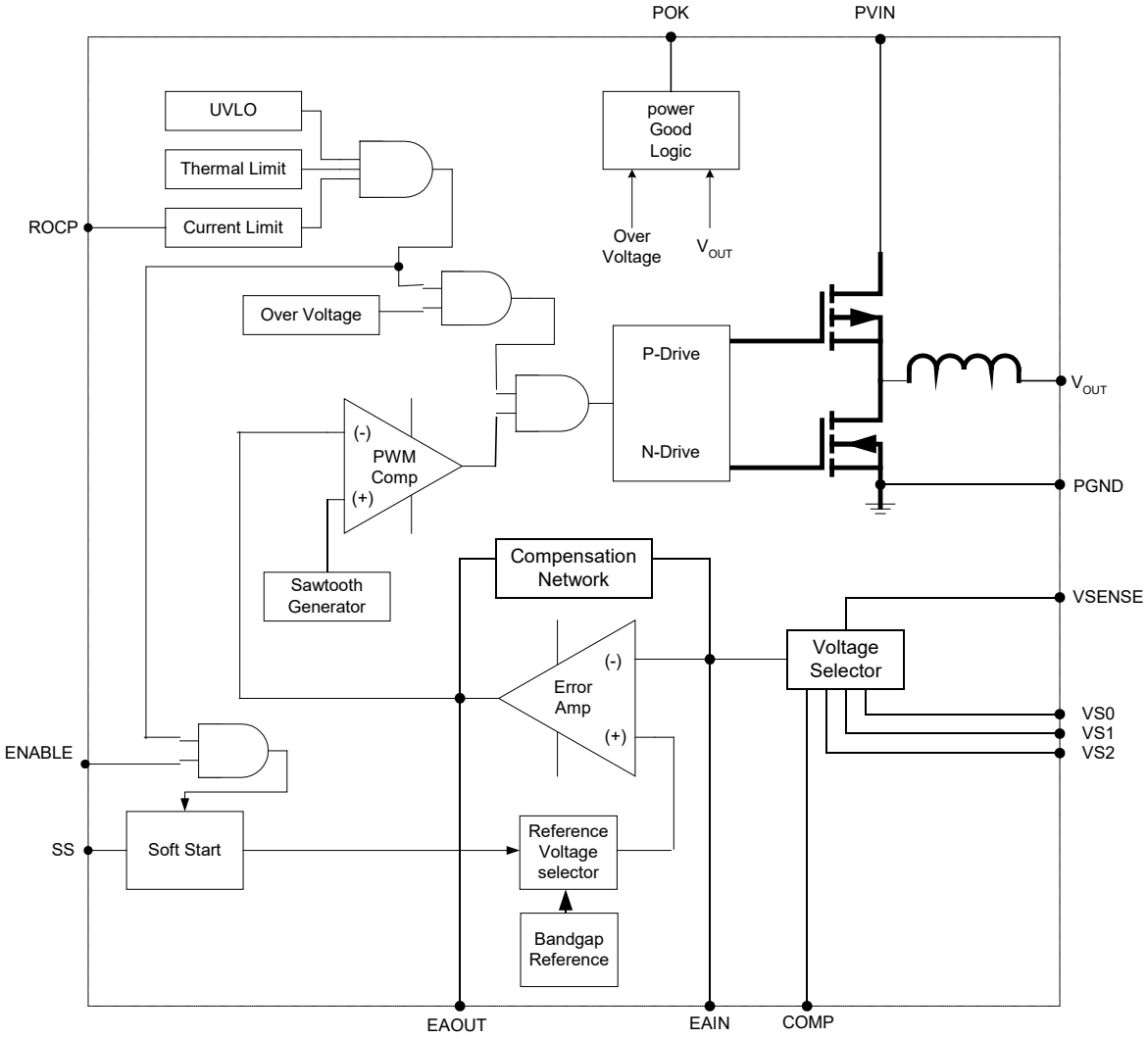


Figure 3: Functional Block Diagram

FUNCTIONAL DESCRIPTION

Synchronous DC-DC Step-Down PowerSoC

The EN5335QI is a synchronous, pin programmable power supply with integrated power MOSFET switches and integrated inductor. The nominal input voltage range is 2.4-5.0V. The output can be set to common pre-set voltages by connecting appropriate combinations of 3 voltage selection pins to ground. The feedback control loop is a type III voltage-mode and the part uses a low-noise PWM topology. Up to 3A of output current can be drawn from this converter. The 5MHz operating frequency enables the use of small-size output capacitors.

The power supply has the following protection features:

- Over-current protection (to protect the IC from excessive load current)
- Thermal shutdown with hysteresis
- Over-voltage protection
- Under-voltage lockout circuit to disable the converter output when the input voltage is less than approximately 2.2V

Additional features include:

- Soft-start circuit, limiting the in-rush current when the converter is powered up
- Power good circuit indicating whether the output voltage is within 90% - 120% of the programmed voltage.

Output Voltage Programming

The EN5335QI output voltage is programmed using a 3-pin voltage-ID or VID selector. Three binary VID pins allow the user to choose one of seven pre-set voltages. Refer to Table 1 for the proper VID pin settings to choose VOUT.

The voltage select pins, VS0, VS1, and VS2, are pulled-up internally and so will default to a logic high, or "1", if left "open". Connecting the voltage select pin to ground will result in a logic "0".

Table 1: Output Voltage Select Table

VS2*	VS1*	VS0*	Output Voltage
0	0	0	3.3V
0	0	1	2.5V
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V
1	1	0	0.8V
1	1	1	Reserved

Input Capacitor Selection

The EN5335QI requires about 20µF of input capacitance. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this converter. The dielectric must be X5R or X7R rated. In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling. It is recommended to use 10V rated MLCC capacitors.

Table 2: Recommended input capacitors

Description	MFG	P/N
10µF, 10V, 10%, X7R, 1206 (2 capacitors needed)	Murata Taiyo Yuden	GRM31CR71A106KA01L LMK316B7106KL-T
22µF, 10V, 10%, X7R, 1210 (1 capacitor needed)	Murata Taiyo Yuden	GRM32ER71A226KE20L LMK325B7226KM-T

Output Capacitor Selection

The EN5335QI has been optimized for use with approximately 50µF of output capacitance. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose capacitance with frequency, temperature and bias voltage.

Output ripple voltage is determined by the aggregate output capacitor impedance. Output impedance, denoted as Z, is comprised of effective series resistance, ESR, and effective series inductance, ESL:

Z = ESR + ESL

Placing output capacitors in parallel reduces the impedance and will hence result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

Table 3: Typical ripple versus capacitance is given below

Output Capacitor Configuration	Typical Output Ripple (mVp-p) (as measured on EN5335QI Evaluation Board)
1 x 47 µF	30
3 x 22 µF	15

Table 4: Recommended output capacitors

Description	MFG	P/N
22µF, 6.3V, 10%, X5R, 1206 (3 capacitors needed)	Murata Taiyo Yuden	GRM31CR60J226KE19L JMK316BJ226KL-T
47µF, 10V, 10%, X5R, 1210 47µF, 6.3V, 10%, X5R, 1210 (1 capacitor needed)	Murata AVX	GRM32ER61A476KE20L 12106D476KAT2A

Enable Operation

The ENABLE pin provides a means to shut down the device, or enable normal operation. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted, the device will undergo a normal soft start. A logic low will disable the converter and cause it to shut down. When Enable goes low, circuitry internal to the device continue to operate to ensure the output voltage is gradually returned to zero and the circuits turn off subsequently. A short low going pulse on Enable is ignored.

Soft-Start Operation

Soft start is a method to reduce in-rush current when the device is enabled. The output voltage is ramped up slowly upon start-up. The output rise time is controlled by choice of a soft-start capacitor, which is placed between the SS pin (pin 37) and the AGND pin (pin 29).

Rise Time: $T_R = C_{ss}$* 75KΩ

During start-up of the converter, the reference voltage to the error amplifier is gradually increased from zero to its final level by an internal current source of typically 10uA. Typical soft-start rise time is 1mS to 3mS. The rise time is measured from the time when AVIN > V_{UVLO} and the Enable signal crosses its logic high threshold. Typical SS capacitor values are in the range of 15nF to 50 nF.

Power-Up/Down Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. The PVIN should never be powered when AVIN is off. During power down, the AVIN should not be powered down before the PVIN. Tying PVIN and AVIN or all three pins (AVIN, PVIN, ENABLE) together during power up or power down meets these requirements.

Pre-Bias Start-up

The EN5335QI does not support startup into a pre-biased condition. Be sure the output capacitors are not charged or the output of the EN5335QI is not pre-biased when the EN5335QI is first enabled.

POK Operation

The POK signal is an open drain signal from the converter indicating the output voltage is within the specified range. The POK signal will be a logic high when the output voltage is within 90% - 120% of the programmed output voltage. If the output voltage goes outside of this range, the POK signal will be a logic low until the output voltage has returned to within this range. In the event of an over-voltage condition the POK signal will go low and will remain in this condition until the output voltage has dropped to 95% of the programmed output voltage before returning to the high state (see also: Over-Voltage Protection).

Over-Current Protection

The current limit function is achieved by sensing the current flowing through the sense P-MOSFET. When the sensed current exceeds the current limit, both NFET and PFET switches are turned off. If the over-current condition is removed, the over-current protection circuit will enable the PWM operation. This circuit is designed to provide high noise immunity.

The nominal over current trip point is set to 4.5A. It is possible to increase the over-current set point by about 50% by connecting a 7.5kΩ resistor between ROCP (pin 27) and GND. The typical voltage at the ROCP pin is 0.75V.

In some cases, such as the start-up of FPGA devices, it is desirable to blank the over-current protection feature. In order to disable over-current protection, the ROCP pin should be tied to any voltage between 2.5V and PVIN.

Over-Voltage Protection

When the output voltage exceeds 120% of the programmed output voltage, the PWM operation stops, the lower N-MOSFET is turned on and the POK signal goes low. When the output voltage drops below 95% of the programmed output voltage, normal PWM operation resumes and POK returns to its high state.

Thermal Overload Protection

Thermal shutdown will disable operation once the Junction temperature exceeds approximately 150ºC. Once the junction temperature drops by approx 25ºC, the converter will re-start with a normal soft-start.

Input Under-voltage Lock-out

Circuitry is provided to ensure that when the input voltage is below the specified voltage range, the converter will not start-up. Circuits for hysteresis, input de-glitch and output leading edge blanking are included to ensure high noise immunity and prevent false tripping.

Compensation

The EN5335QI is internally compensated through the use of a type 3 compensation network and is optimized for use with about 50µF of output capacitance and will provide excellent loop bandwidth and transient performance for most applications. (See the section on Capacitor Selection for details on recommended capacitor types.) Voltage mode operation provides high noise immunity at light load.

In some cases modifications to the compensation may be required. For more information, contact Intel Power Applications support.

LAYOUT RECOMMENDATIONS

Figure 4 shows critical components and layer 1 traces of a recommended minimum footprint EN5335QI layout. Alternate ENABLE configurations and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files on the Intel website www.intel.com/enpirion for exact dimensions and other layers. Please refer to Figure 4 while reading the layout recommendations in this section.

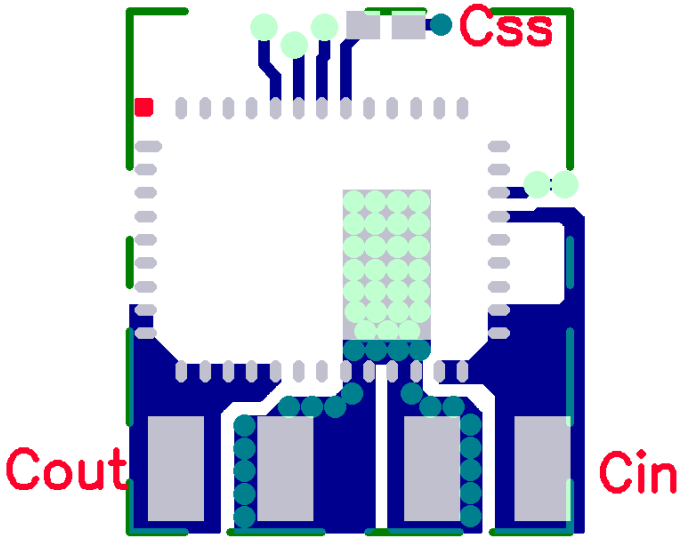


Figure 4: Optimized Layout Recommendations

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN5335QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN5335QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: Two PGND pins are dedicated to the input circuit, and two to the output circuit. The slit in Figure 4 separating the input and output GND circuits helps minimize noise coupling between the converter input and output switching loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the Gerber files on the Intel website www.intel.com/enpirion.

Recommendation 4: The large thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter. Please see Figures: 5, 6, and 7.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4 should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. Please see Figure 4. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND slit separating the two components. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

Recommendation 6: AVIN is the power supply for the internal small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 4 this connection is made at the input capacitor close to the V_{IN} connection.

Recommendation 7: The layer 1 metal under the device must not be more than shown in Figure 4. See the section regarding exposed metal on bottom of package. As with any switch-mode DC-DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 8: The VSENSE point should be just after the last output filter capacitor. Keep the sense trace as short as possible in order to avoid noise coupling into the control loop.

DESIGN CONSIDERATIONS FOR LEAD-FRAME BASED MODULES

Exposed Metal on Bottom of Package

Lead frame offers many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package.

Only the large thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN5335QI should be clear of any metal except for the large thermal pad. The “grayed-out” area in Figure 5 represents the area that should be clear of any metal (traces, vias, or planes), on the top layer of the PCB. Figure 6 shows the recommended PCB footprint for this device.

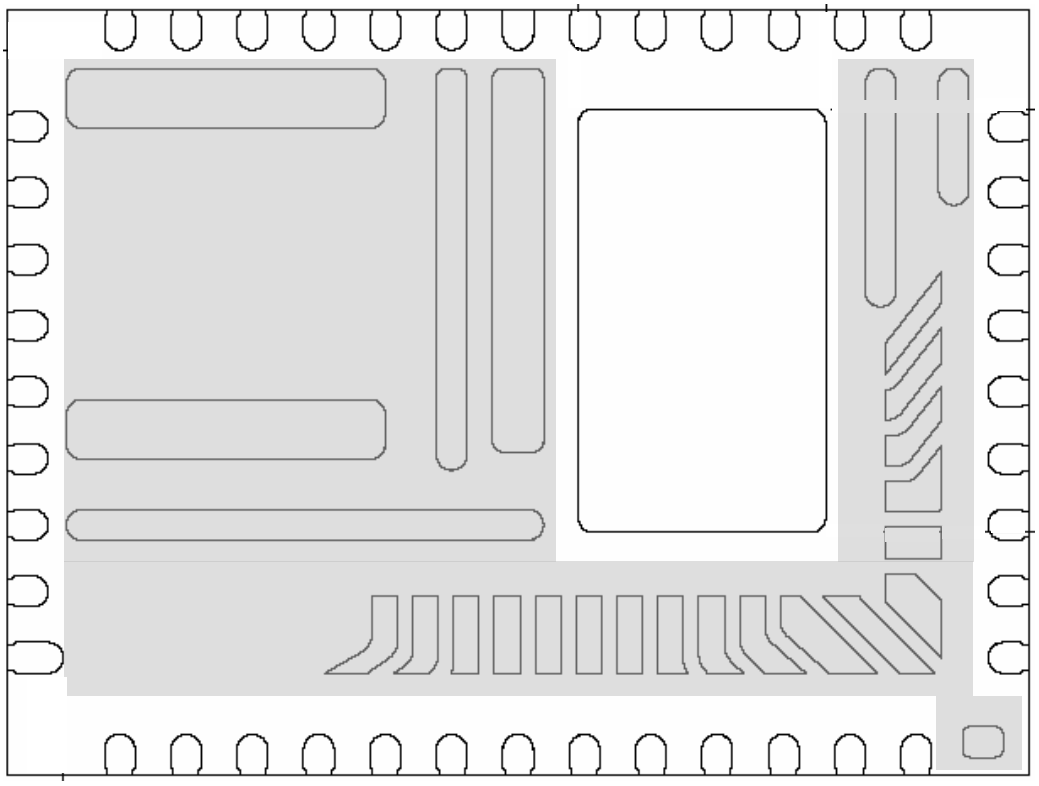


Figure 5. Lead-Frame exposed metal. Grey area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

RECOMMENDED PCB FOOTPRINT

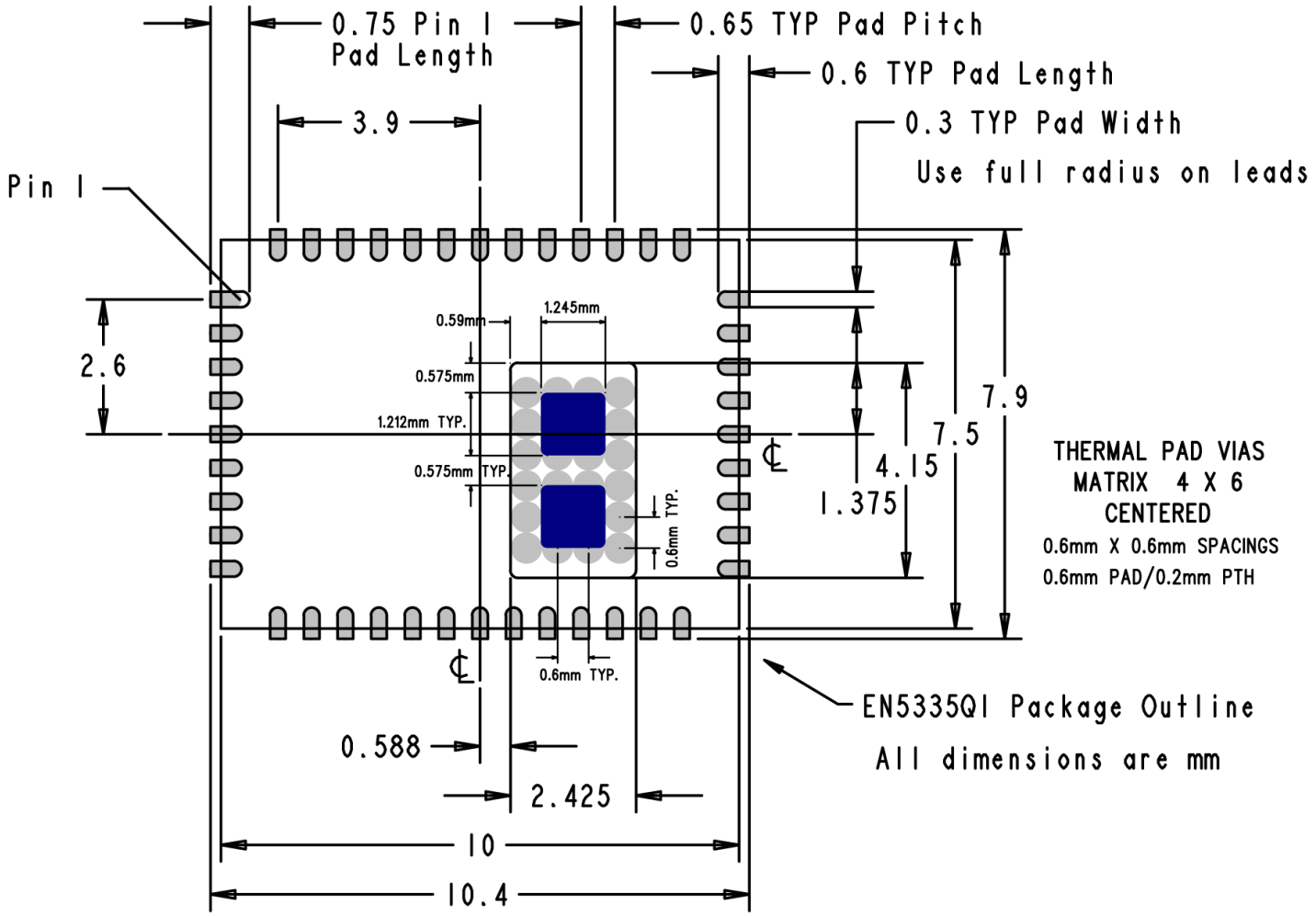


Figure 6: EN5335QI PCB Footprint (Top View)

The solder stencil aperture for the thermal pad is shown in blue and is based on Enpirion power product manufacturing specifications.

PACKAGE DIMENSIONS

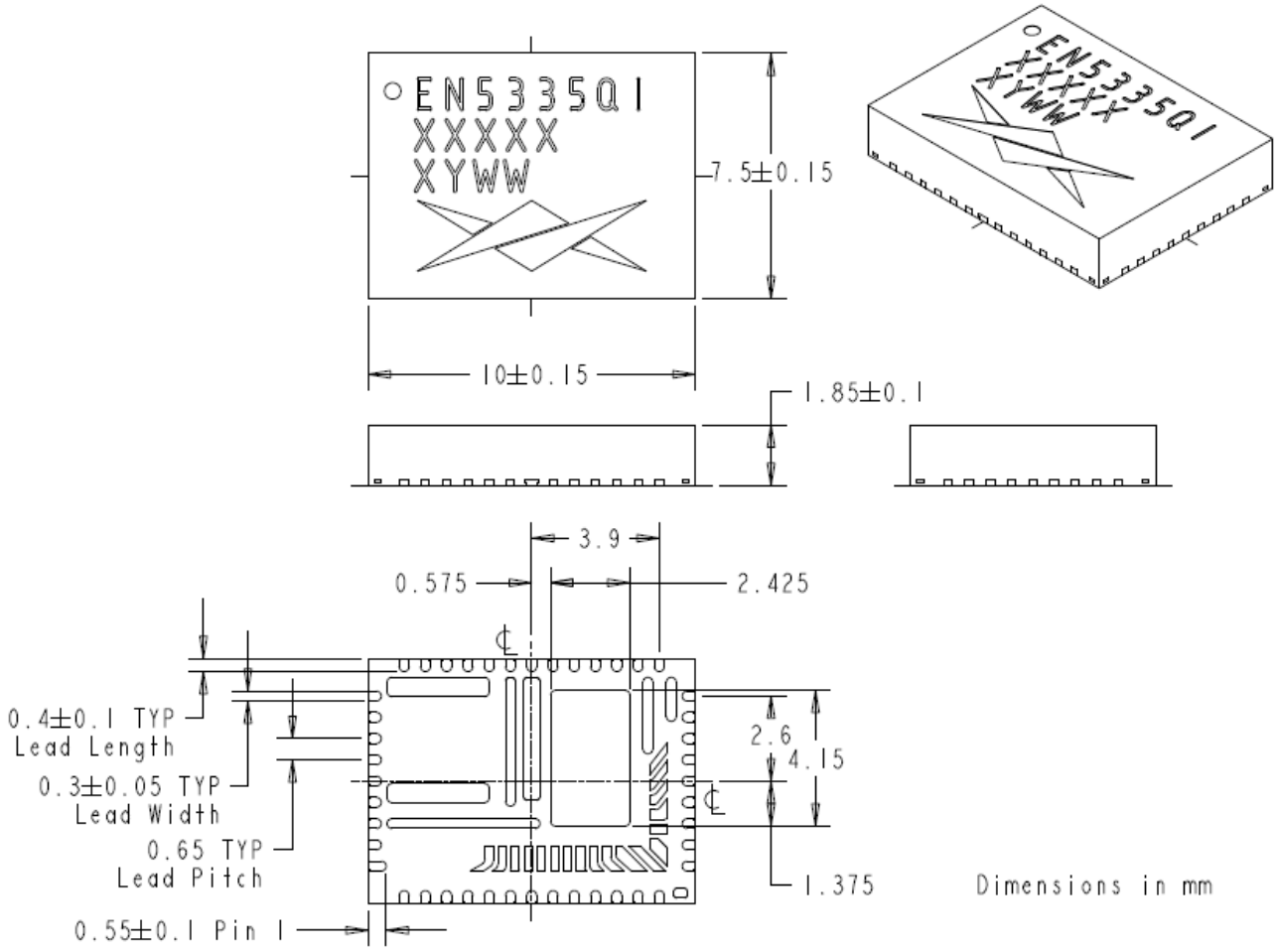


Figure 7: EN5335QI Package Dimensions (Bottom View)

Packing and Marking Information: https://www.intel.com/support/quality-and-reliability/packing.html

REVISION HISTORY

Rev	Date	Change(s)
K	Feb, 2019	Changed datasheet into Intel format.

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

www.intel.com/enpirion

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