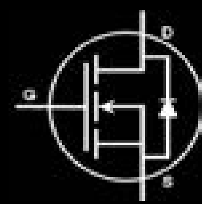
EPC2018 – Enhancement Mode Power Transistor

V_{DSS} , 150 V
$R_{DS(ON)}$, 25 mΩ
I_D , 12 A

NEW PRODUCT



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 55 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(ON)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage	150	V
I_D	Continuous (T_A =25˚C, θ_{JA} = 17)	12	A
	Pulsed (25˚C, Tpulse = 300 µs)	60	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-5	
T_J	Operating Temperature	-40 to 125	˚C
T_{STG}	Storage Temperature	-40 to 150	

EPC2018 eGaN® FETs are supplied only in passivated die form with solder bars

Applications

- High Speed DC-DC conversion
- Class D Audio
- Hard Switched and High Frequency Circuits

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics (T_J= 25˚C unless otherwise stated)						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 200 µA	150			V
I_{DSS}	Drain Source Leakage	V_{DS} = 120 V, V_{GS} = 0 V		50	150	µA
I_{GSS}	Gate-Source Forward Leakage	V_{GS} = 5 V		1	3	mA
	Gate-Source Reverse Leakage	V_{GS} = -5 V		0.2	1	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 3 mA	0.7	1.4	2.5	V
$R_{DS(ON)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 6 A		18	25	mΩ
Source-Drain Characteristics (T_J= 25˚C unless otherwise stated)						
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V, T = 25˚C		1.8		V
		I_S = 0.5 A, V_{GS} = 0 V, T = 125˚C		1.8		

Thermal Characteristics			
		TYP	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.4	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	16	˚C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	56	˚C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Characteristics (T_J = 25˚C unless otherwise stated)						
C_{ISS}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V		480	540	pF
C_{OSS}	Output Capacitance			270	350	
C_{RSS}	Reverse Transfer Capacitance			9.2	12	
Q_G	Total Gate Charge (V_{GS} = 5 V)	V_{DS} = 100 V, I_D = 12 A		5	7.5	nC
Q_{GD}	Gate to Drain Charge			1.7	2.6	
Q_{GS}	Gate to Source Charge			1.3	2	
Q_{OSS}	Output Charge	V_{DS} = 100 V, V_{GS} = 0 V		40	50	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate shorted to source.

Figure 1: Typical Output Characteristics

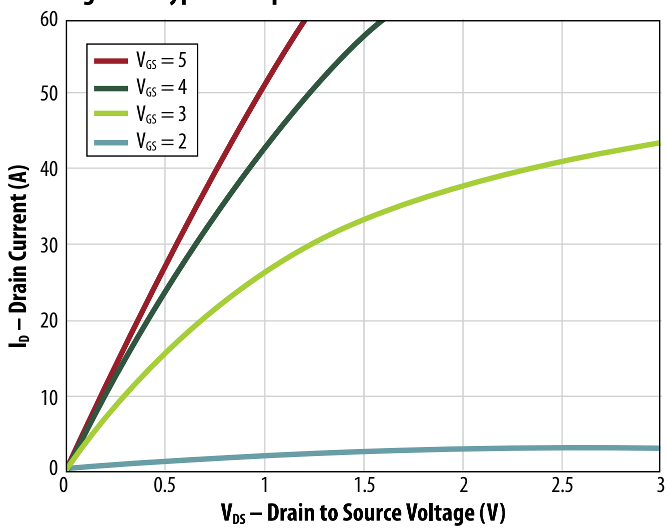


Figure 2: Transfer Characteristics

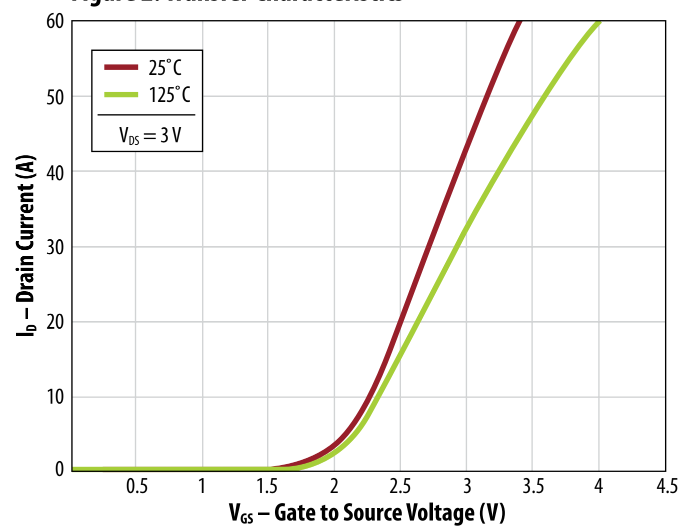


Figure 3: $R_{DS(ON)}$ vs V_G for Various Current

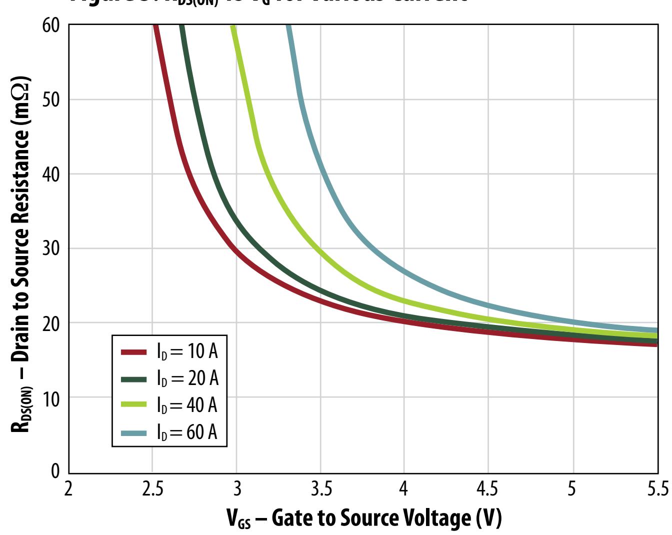


Figure 4: $R_{DS(ON)}$ vs V_G for Various Temperature

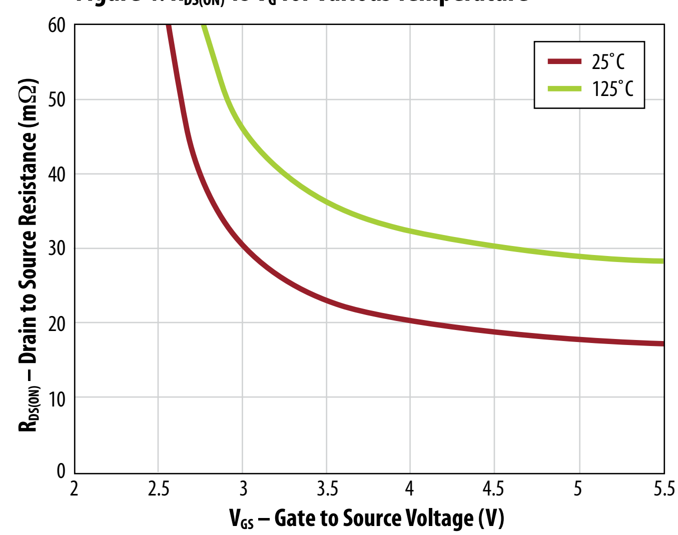


Figure 5: Capacitance

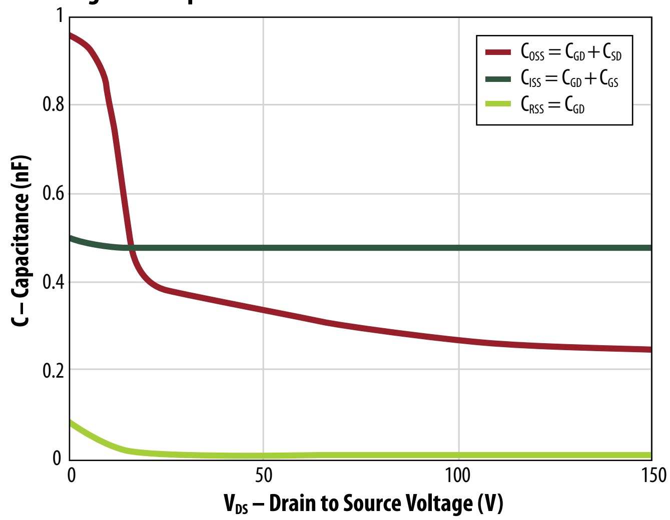


Figure 6: Gate Charge

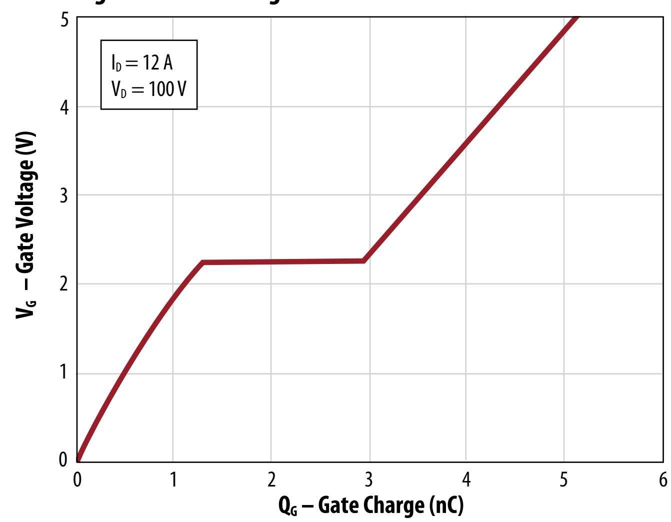


Figure 7: Reverse Drain-Source Characteristics

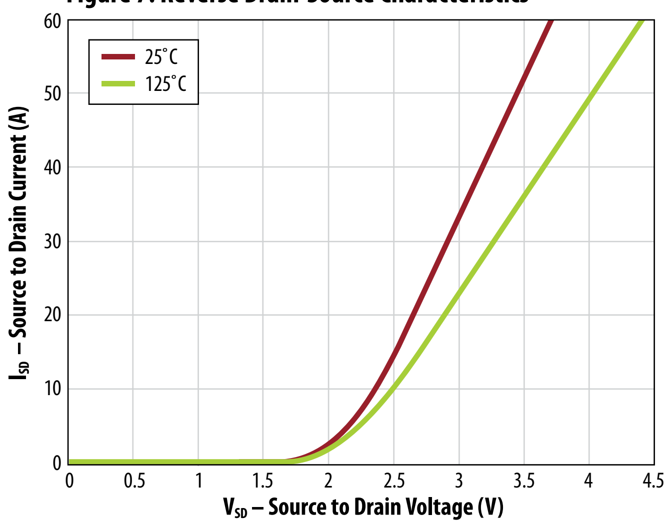


Figure 8: Normalized On Resistance vs Temperature

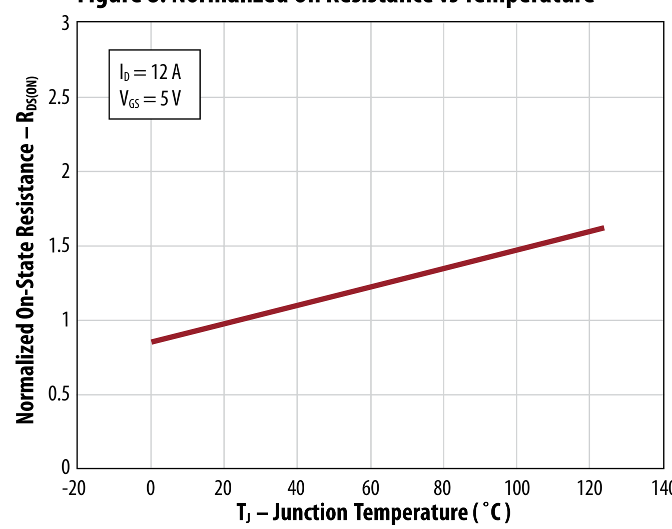


Figure 9: Normalized Threshold Voltage vs Temperature

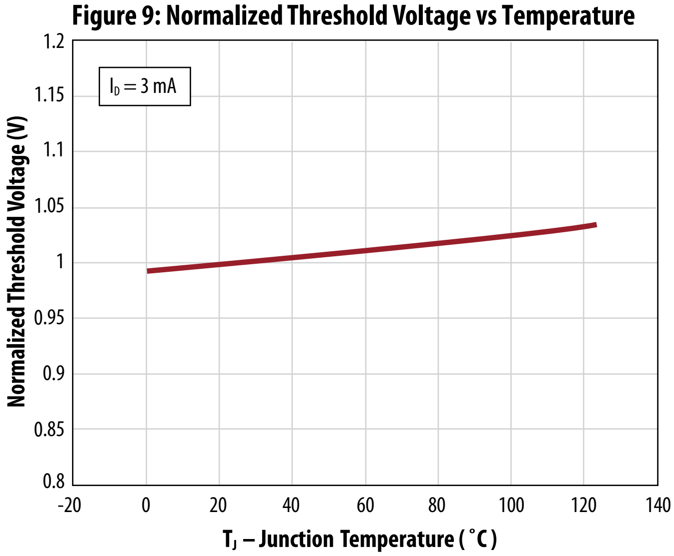
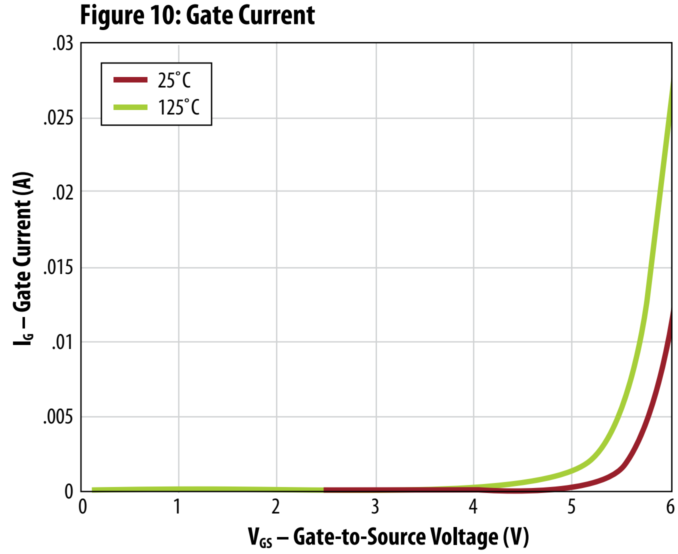
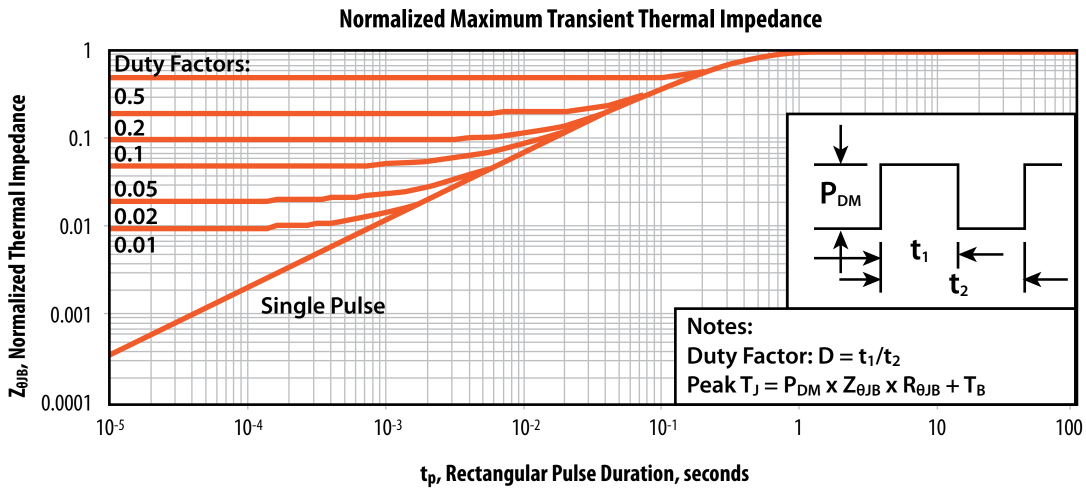


Figure 10: Gate Current



All measurements were done with substrate shortened to source.

Figure 11: Transient Thermal Response Curves



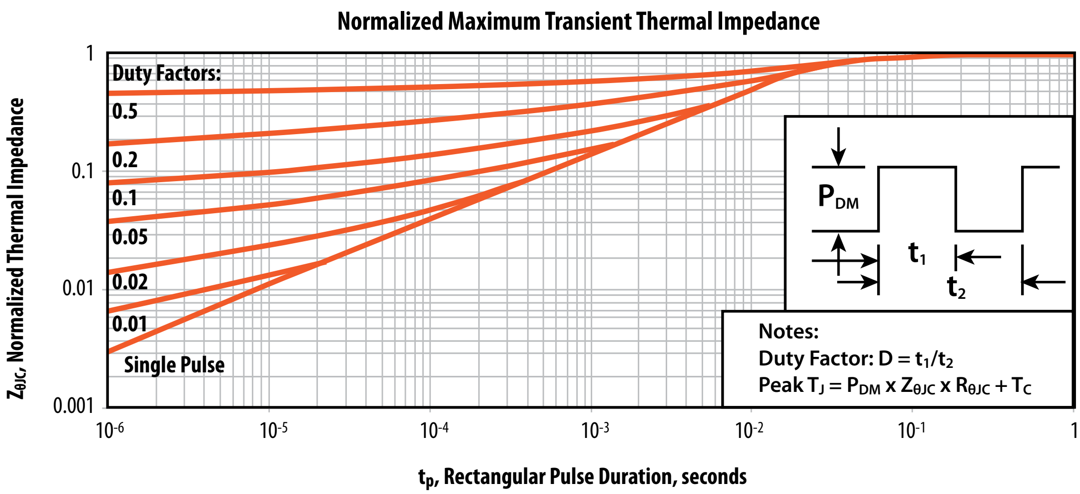
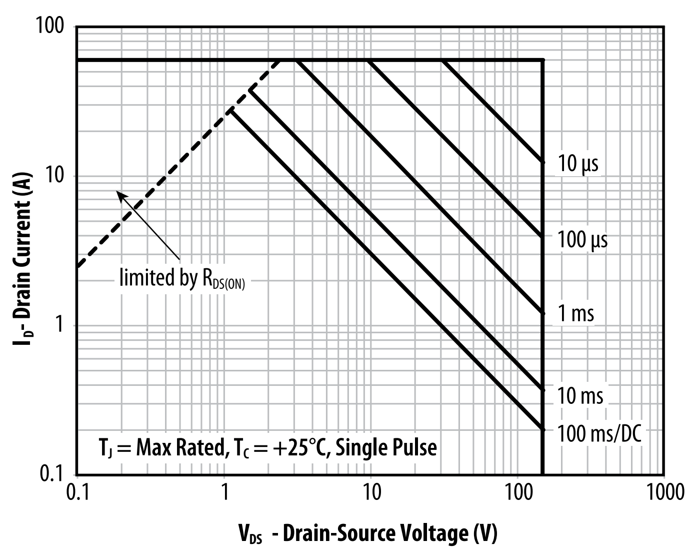
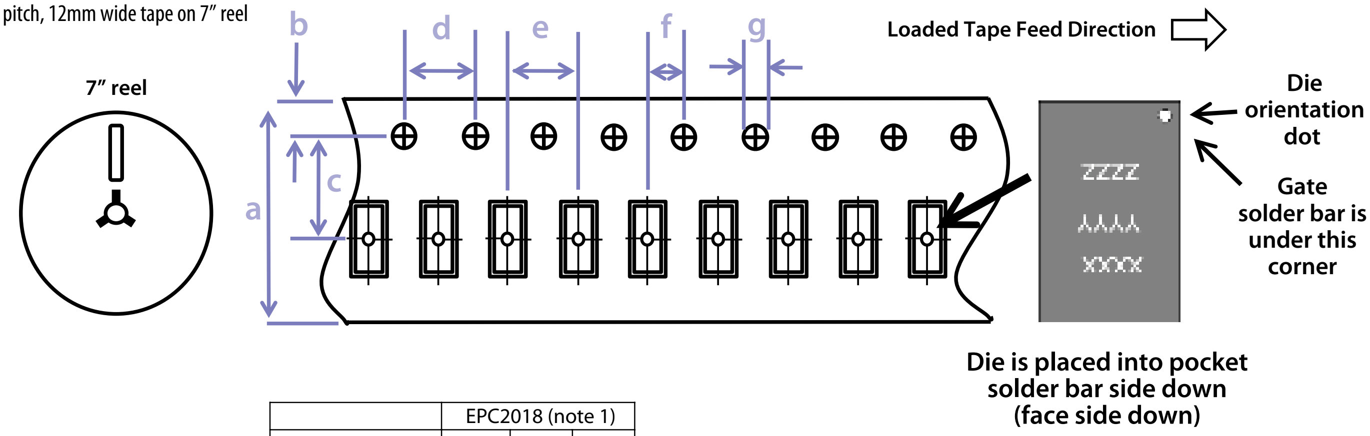


Figure 12: Safe Operating Area



TAPE AND REEL CONFIGURATION

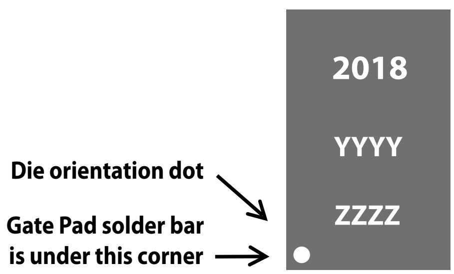
4mm pitch, 12mm wide tape on 7" reel



	EPC2018 (note 1)		
Dimension (mm)	target	min	max
a	12.0	11.9	12.3
b	1.75	1.65	1.85
c (note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (note 2)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

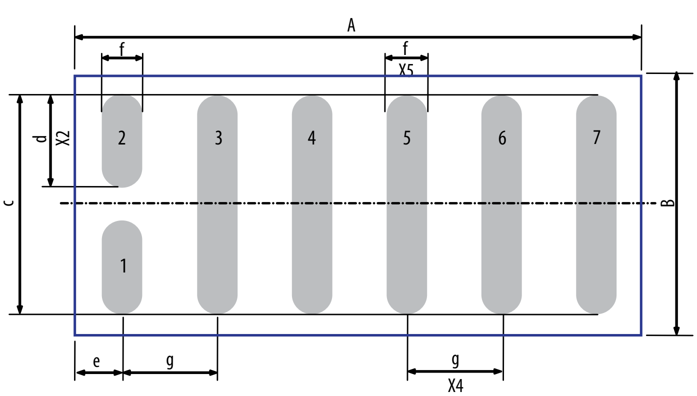
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2018	2018	YYYY	ZZZZ

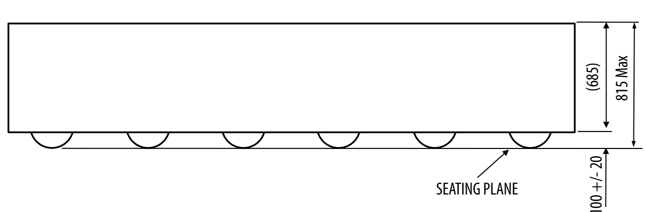
DIE OUTLINE

Solder Bar View



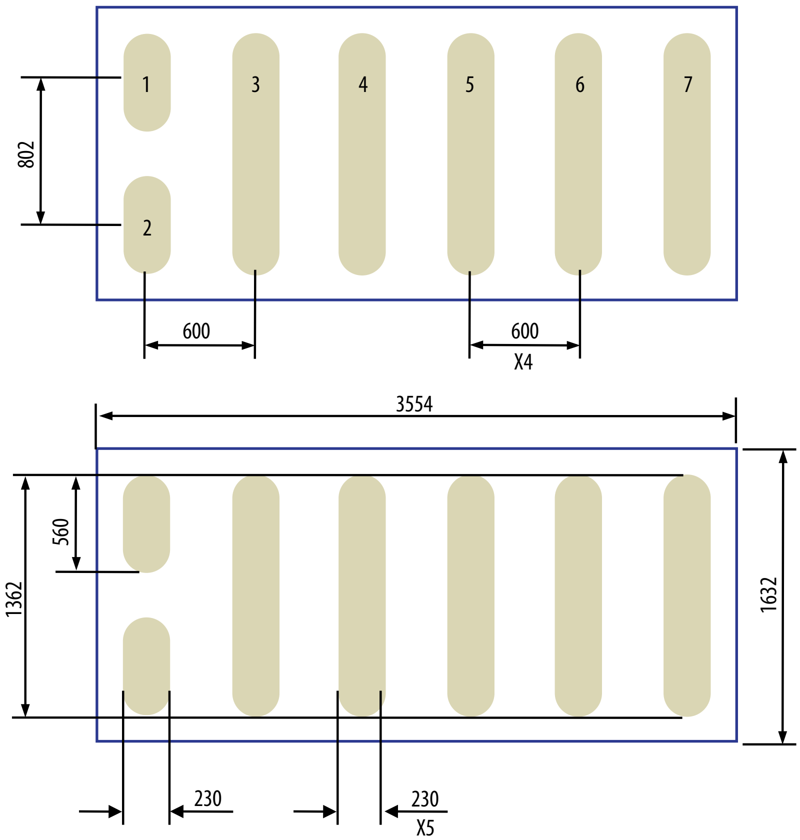
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	3524	3554	3584
B	1602	1632	1662
c	1379	1382	1385
d	577	580	583
e	262	277	292
f	245	250	255
g	600	600	600

Side View



RECOMMENDED LAND PATTERN
(units in µm)

The land pattern is solder mask defined.



Pad no. 1 is Gate;
Pads no. 3, 5, 7 are Drain;
Pads no. 4, 6 are Source;
Pad no. 2 is Substrate

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