Quick Start Procedure

Development board EPC9004 is easy to set up to evaluate the performance of the EPC1012 *eGaN* FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to +VIN (J5, J6) and ground / return to –VIN (J7, J8).
2. With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required.
3. With power off, connect the gate drive input to +VDD (J1, Pin-1) and ground return to –VDD (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 200 V on V_{OUT}).
7. Turn on the controller / PWM input source and probe switching node to see switching operation.
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

THERMAL CONSIDERATIONS

The EPC9004 development board showcases the EPC1012 *eGaN* FET. Although the electrical performance surpasses that for traditional Si devices, their relatively smaller size does magnify the thermal management requirements. The EPC9004 is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.

NOTE. The EPC9004 development board does not have any current or thermal protection on board.

Figure 1: Block Diagram of EPC9004 Development Board

Figure 4: Waveforms for VIN = 150 V to 5 V/2 A (100kHz) Buck converter
CH1: VPWM Input voltage – CH2: (IOUT) Switch node current – CH4: (VOUT) Switch node voltage

Figure 2: Proper Connection and Measurement Setup

Figure 3: Proper Measurement of Switch Node – OUT

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EFFICIENT POWER CONVERSION

Development Board / Demonstration Board Notification

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Development Board EPC9004 Quick Start Guide

200 V Half-Bridge with Gate Drive, Using EPC2012

EFFICIENT POWER CONVERSION

The EPC9004 development board is a 200 V maximum device voltage, 2 A maximum output current, half bridge with onboard gate drives, featuring the EPC2012 enhancement mode (*eGaN*®) field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2012 *eGaN* FET by including all the critical components on a single board that can be easily connected into any existing converter.

The EPC9004 development board is 2" x 1.5" and contains not only two EPC2012 *eGaN* FET in a half bridge configuration using two Texas Instruments UCC27611 gate drivers as well as supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1.

For more information on the EPC2012 *eGaN* FET please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (TA = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{DD}	Gate Drive Input Supply Range		7	12	V
V_{IN}	Bus Input Voltage Range			150	V
V_{OUT}	Switch Node Output Voltage			200	V
I_{OUT}	Switch Node Output Current			2*	A
V_{PWM}	PWM Logic Input Voltage Threshold	'Input 'High'	3.5	6	V
		'Input 'Low'	0	1.5	V
	Minimum 'High' State Input Pulse Width	VPWM rise and fall time < 10ns	100		ns
	Minimum 'Low' State Input Pulse Width	VPWM rise and fall time < 10ns	500#		ns

* Assumes inductive load, maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermals.
\# Dependent on time needed to 'refresh' high side bootstrap supply voltage.

Quick Start Procedure

Development board EPC9004 is easy to set up to evaluate the performance of the EPC1012 *eGaN* FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to +VIN (J5, J6) and ground / return to –VIN (J7, J8).
2. With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required.
3. With power off, connect the gate drive input to +VDD (J1, Pin-1) and ground return to –VDD (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 200 V on V_{OUT}).
7. Turn on the controller / PWM input source and probe switching node to see switching operation.
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

THERMAL CONSIDERATIONS

The EPC9004 development board showcases the EPC1012 *eGaN* FET. Although the electrical performance surpasses that for traditional Si devices, their relatively smaller size does magnify the thermal management requirements. The EPC9004 is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.

NOTE. The EPC9004 development board does not have any current or thermal protection on board.

Figure 1: Block Diagram of EPC9004 Development Board

Figure 4: Waveforms for VIN = 150 V to 5 V/2 A (100kHz) Buck converter
CH1: VPWM Input voltage – CH2: (IOUT) Switch node current – CH4: (VOUT) Switch node voltage

Figure 2: Proper Connection and Measurement Setup

Figure 3: Proper Measurement of Switch Node – OUT

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EFFICIENT POWER CONVERSION

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Development Board EPC9004 Quick Start Guide

200 V Half-Bridge with Gate Drive, Using EPC2012

EFFICIENT POWER CONVERSION

The EPC9004 development board is a 200 V maximum device voltage, 2 A maximum output current, half bridge with onboard gate drives, featuring the EPC2012 enhancement mode (*eGaN*®) field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2012 *eGaN* FET by including all the critical components on a single board that can be easily connected into any existing converter.

The EPC9004 development board is 2" x 1.5" and contains not only two EPC2012 *eGaN* FET in a half bridge configuration using two Texas Instruments UCC27611 gate drivers as well as supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1.

For more information on the EPC2012 *eGaN* FET please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (TA = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{DD}	Gate Drive Input Supply Range		7	12	V
V_{IN}	Bus Input Voltage Range			150	V
V_{OUT}	Switch Node Output Voltage			200	V
I_{OUT}	Switch Node Output Current			2*	A
V_{PWM}	PWM Logic Input Voltage Threshold	'Input 'High'	3.5	6	V
		'Input 'Low'	0	1.5	V
	Minimum 'High' State Input Pulse Width	VPWM rise and fall time < 10ns	100		ns
	Minimum 'Low' State Input Pulse Width	VPWM rise and fall time < 10ns	500#		ns

* Assumes inductive load, maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermals.
\# Dependent on time needed to 'refresh' high side bootstrap supply voltage.

Quick Start Procedure

Development board EPC9004 is easy to set up to evaluate the performance of the EPC2012 *eGaN* FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to $+V_{IN}$ (J5, J6) and ground / return to $-V_{IN}$ (J7, J8).
2. With power off, connect the switch node of the half bridge V_{OUT} (J3, J4) to your circuit as required.
3. With power off, connect the gate drive input to $+V_{DD}$ (J1, Pin-1) and ground return to $-V_{DD}$ (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 200 V on V_{OUT}).
7. Turn on the controller / PWM input source and probe switching node to see switching operation.
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

THERMAL CONSIDERATIONS

The EPC9004 development board showcases the EPC2012 *eGaN* FET. Although the electrical performance surpasses that for traditional Si devices, their relatively smaller size does magnify the thermal management requirements. The EPC9004 is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.

NOTE. The EPC9004 development board does not have any current or thermal protection on board.

Figure 1: Block Diagram of EPC9004 Development Board

Figure 4: Waveforms for V_{IN} = 150 V to 5 V/2 A (100kHz) Buck converter
CH1: VPWM Input voltage – CH2: (I_{OUT}) Switch node current – CH4: (V_{OUT}) Switch node voltage

Figure 2: Proper Connection and Measurement Setup

Figure 3: Proper Measurement of Switch Node – V_{OUT}

The EPC9004 development board is a 200 V maximum device voltage, 2 A maximum output current, half bridge with onboard gate drives, featuring the EPC2012 enhancement mode (*eGaN*®) field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2012 *eGaN* FET by including all the critical components on a single board that can be easily connected into any existing converter.

The EPC9004 development board is 2" x 1.5" and contains not only two EPC2012 *eGaN* FET in a half bridge configuration using two Texas Instruments UCC27611 gate drivers as well as supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1.

For more information on the EPC2012 *eGaN* FET please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{DD}	Gate Drive Input Supply Range		7	12	V
V_{IN}	Bus Input Voltage Range			150	V
V_{OUT}	Switch Node Output Voltage			200	V
I_{OUT}	Switch Node Output Current			2*	A
V_{PWM}	PWM Logic Input Voltage Threshold	'Input 'High'	3.5	6	V
		'Input 'Low'	0	1.5	V
	Minimum 'High' State Input Pulse Width	VPWM rise and fall time < 10ns	100		ns
	Minimum 'Low' State Input Pulse Width	VPWM rise and fall time < 10ns	500#		ns

* Assumes inductive load, maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermals.
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Development Board EPC9004 Quick Start Guide

200 V Half-Bridge with Gate Drive, Using EPC2012

EFFICIENT POWER CONVERSION

Quick Start Procedure

Development board EPC9004 is easy to set up to evaluate the performance of the EPC2012 *eGaN* FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to $+V_{IN}$ (J5, J6) and ground / return to $-V_{IN}$ (J7, J8).
2. With power off, connect the switch node of the half bridge V_{OUT} (J3, J4) to your circuit as required.
3. With power off, connect the gate drive input to $+V_{DD}$ (J1, Pin-1) and ground return to $-V_{DD}$ (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 200 V on V_{OUT}).
7. Turn on the controller / PWM input source and probe switching node to see switching operation.
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

THERMAL CONSIDERATIONS

The EPC9004 development board showcases the EPC2012 *eGaN* FET. Although the electrical performance surpasses that for traditional Si devices, their relatively smaller size does magnify the thermal management requirements. The EPC9004 is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.

NOTE. The EPC9004 development board does not have any current or thermal protection on board.

Figure 1: Block Diagram of EPC9004 Development Board

Figure 4: Waveforms for V_{IN} = 150 V to 5 V/2 A (100kHz) Buck converter
CH1: VPWM Input voltage – CH2: (I_{OUT}) Switch node current – CH4: (V_{OUT}) Switch node voltage

Figure 2: Proper Connection and Measurement Setup

Figure 3: Proper Measurement of Switch Node – V_{OUT}

The EPC9004 development board is a 200 V maximum device voltage, 2 A maximum output current, half bridge with onboard gate drives, featuring the EPC2012 enhancement mode (*eGaN*®) field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2012 *eGaN* FET by including all the critical components on a single board that can be easily connected into any existing converter.

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For more information on the EPC2012 *eGaN* FET please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{DD}	Gate Drive Input Supply Range		7	12	V
V_{IN}	Bus Input Voltage Range			150	V
V_{OUT}	Switch Node Output Voltage			200	V
I_{OUT}	Switch Node Output Current			2*	A
V_{PWM}	PWM Logic Input Voltage Threshold	'Input 'High'	3.5	6	V
		'Input 'Low'	0	1.5	V
	Minimum 'High' State Input Pulse Width	VPWM rise and fall time < 10ns	100		ns
	Minimum 'Low' State Input Pulse Width	VPWM rise and fall time < 10ns	500#		ns

* Assumes inductive load, maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermals.
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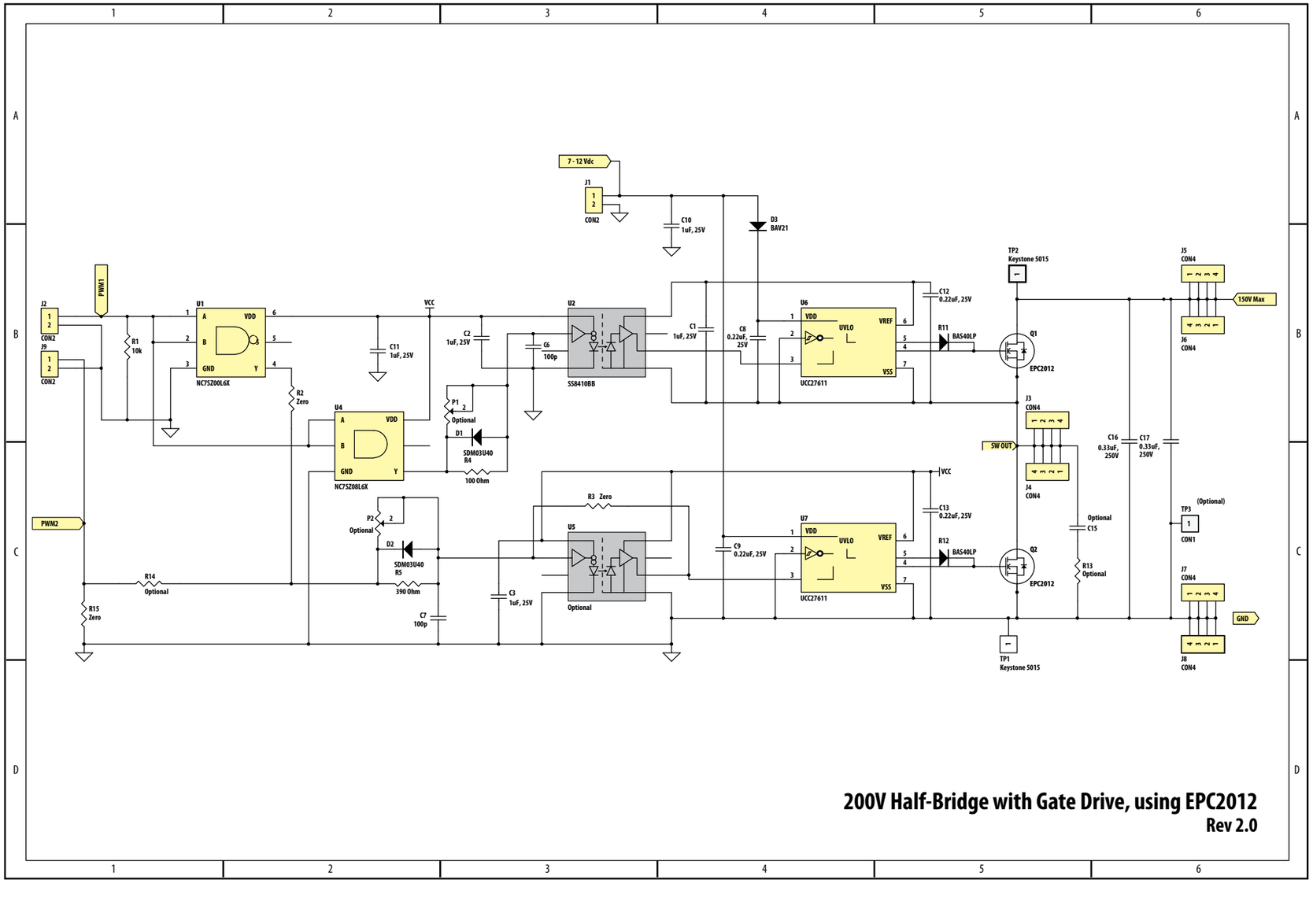
Development Board EPC9004 Quick Start Guide

200 V Half-Bridge with Gate Drive, Using EPC2012

EFFICIENT POWER CONVERSION

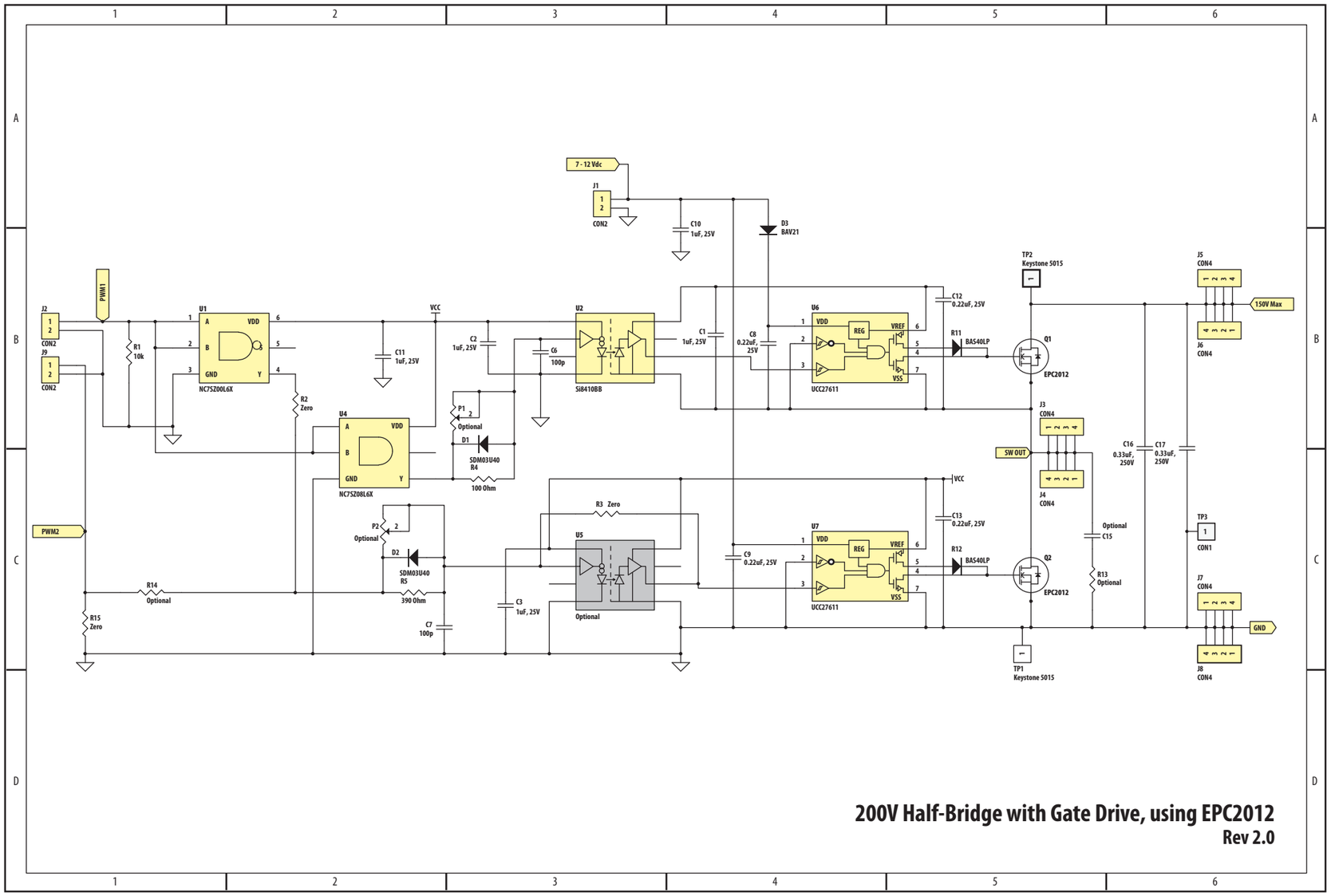
16	2	TP1, TP2	Test Point	Keystone Elect, 5015
17	1	TP3	Connector	1/40th of Tyco, 4-103185-0
18	1	U1	I.C., Logic	Fairchild, NC7SZ00L6X
19	1	U2	I.C., Isolator	Silicon Laboratories, Si8410BB
20	1	U4	I.C., Logic	Fairchild, NC7SZ08L6X
21	2	U6, U7	I.C., Gate driver	Texas Instruments, UCC27611
22	0	C1, C15	Optional capacitor	
23	0	P1, P2	Optional Potentiometer	
24	0	R13, R14	Optional resistor	
25	0	U5	Optional I.C.	



200V Half-Bridge with Gate Drive, using EPC2012

Rev 2.0

16	2	TP1, TP2	Test Point	Keystone Elect, 5015
17	1	TP3	Connector	1/40th of Tyco, 4-103185-0
18	1	U1	I.C., Logic	Fairchild, NC7SZ00L6X
19	1	U2	I.C., Isolator	Silicon Laboratories, Si8410BB
20	1	U4	I.C., Logic	Fairchild, NC7SZ08L6X
21	2	U6, U7	I.C., Gate driver	Texas Instruments, UCC27611
22	0	C1, C15	Optional capacitor	
23	0	P1, P2	Optional Potentiometer	
24	0	R13, R14	Optional resistor	
25	0	U5	Optional I.C.	



200V Half-Bridge with Gate Drive, using EPC2012
Rev 2.0

Quick Start Procedure

Development board EPC9004 is easy to set up to evaluate the performance of the EPC1012 *eGaN* FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to +VIN (J5, J6) and ground / return to –VIN (J7, J8).
2. With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required.
3. With power off, connect the gate drive input to +VDD (J1, Pin-1) and ground return to –VDD (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 200 V on V_{OUT}).
7. Turn on the controller / PWM input source and probe switching node to see switching operation.
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

THERMAL CONSIDERATIONS

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NOTE. The EPC9004 development board does not have any current or thermal protection on board.

Figure 1: Block Diagram of EPC9004 Development Board

Figure 4: Waveforms for VIN = 150 V to 5 V/2 A (100kHz) Buck converter
CH1: VPWM Input voltage – CH2: (IOUT) Switch node current – CH4: (VOUT) Switch node voltage

Figure 2: Proper Connection and Measurement Setup

Figure 3: Proper Measurement of Switch Node – OUT

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Development Board EPC9004 Quick Start Guide

200 V Half-Bridge with Gate Drive, Using EPC2012

EFFICIENT POWER CONVERSION

The EPC9004 development board is a 200 V maximum device voltage, 2 A maximum output current, half bridge with onboard gate drives, featuring the EPC2012 enhancement mode (*eGaN*®) field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2012 *eGaN* FET by including all the critical components on a single board that can be easily connected into any existing converter.

The EPC9004 development board is 2" x 1.5" and contains not only two EPC2012 *eGaN* FET in a half bridge configuration using two Texas Instruments UCC27611 gate drivers as well as supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1.

For more information on the EPC2012 *eGaN* FET please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (TA = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{DD}	Gate Drive Input Supply Range		7	12	V
V_{IN}	Bus Input Voltage Range			150	V
V_{OUT}	Switch Node Output Voltage			200	V
I_{OUT}	Switch Node Output Current			2*	A
V_{PWM}	PWM Logic Input Voltage Threshold	'Input 'High'	3.5	6	V
		'Input 'Low'	0	1.5	V
	Minimum 'High' State Input Pulse Width	VPWM rise and fall time < 10ns	100		ns
	Minimum 'Low' State Input Pulse Width	VPWM rise and fall time < 10ns	500#		ns

* Assumes inductive load, maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermals.
\# Dependent on time needed to 'refresh' high side bootstrap supply voltage.

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