Demonstration Board EPC9101 Quick Start Guide

EPC2014 + EPC2015 1 MHz Buck Converter

EFFICIENT POWER CONVERSION

DESCRIPTION

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The EPC9101 demonstration board is a 1.2 V output, 1 MHz buck converter with an 20 A maximum output current and 8 V to 24 V input voltage range. The demonstration board features the EPC2014 and EPC2015 enhancement mode (*eGaN*®) field effect transistors (FETs), as well as the first *eGaN* FET specific integrated circuit driver – the Texas Instruments LM5113. The EPC9101 board is not intended as a reference design, but to showcase the performance that can be achieved using the *eGaN* FETs and *eGaN* driver together.

The EPC9101 demonstration board is 3" square and contains a fully closed loop buck converter.

There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1. For more information on the EPC2014/5 *eGaN* FETs or LM5113 driver, please refer to the datasheet available from EPC at www.epc-co.com and www.TI.com. These datasheets, as well that of the LT3833 controller should be read in conjunction with this quick start guide.

Table 1: Performance Summary (TA = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Bus Input Voltage Range		8		24	V
V_{OUT}	Switch Node Output Voltage			1.2		V
I_{OUT}	Switch Node Output Current				20*	A
f_{SW}	Switching frequency			1000		kHz
	Peak Efficiency	12 V_{IN}, = 10 A I_{OUT}		89.5		%
	Full Load Efficiency	12 V_{IN}, = 20 A I_{OUT}		86.4		%
	Full Load Efficiency	24 V_{IN}, = 20 A I_{OUT}		83.3		%

*Maximum limited by thermal considerations and requires 200 LFM forced air cooling

Quick Start Procedure

Demonstration board EPC9101 is easy to set up to evaluate the performance of the EPC2014 and EPC2015 *eGaN* FETs and LM5113 driver. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus between V_{IN} and GND banana jacks as shown.
2. With power off, connect the active (constant current) load as desired between V_{OUT} and GND banana jacks as shown.
3. Turn on the supply voltage to the required value (do not exceed the absolute maximum voltage of 24 V on V_{IN}).
4. Measure the output voltage to make sure the board is fully functional and operating no-load.
5. Turn on active load to the desired load current while staying below the maximum current (20 A)
6. Once operational, adjust the bus voltage and load current within the allowed operating range and observe the output switching behavior, efficiency and other parameters.
7. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node of gate voltage, care must be taken to avoid long ground leads. Measure these by placing the oscilloscope probe tip on the top pad of D3 and grounding the probe directly across D3 on the bottom pad provided for switch node and using the bottom pad of R20 and the GND pad below it for gate voltage. See Figure 3 for proper scope probe technique. Measuring the switch node with a high bandwidth (≥ 500MHz) probe and high bandwidth scope (≥ 1GHz) is recommended.

NOTE. The dead-times for both the leading and trailing edges have been set for optimum full load efficiency. Adjustment is not recommended, but can be done at own risk by replacing R21 and R22 with potentiometers P1 and P2. This should be done while monitoring both the input current and switch-node voltage to determine the effect of these adjustments. Under no circumstance should the input pins to the LM5113 be probed during operation as the added probe capacitance will change the device timing.

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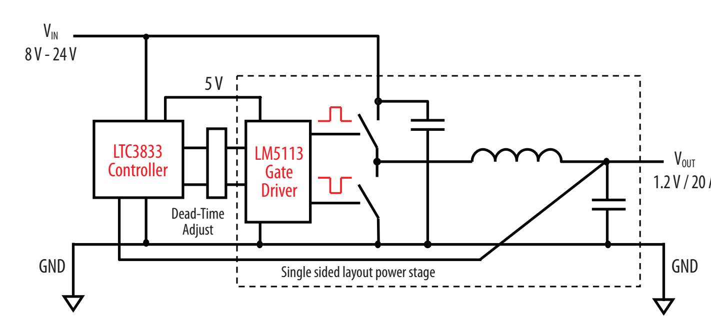


Figure 1: Block Diagram of EPC9101 Demonstration Board

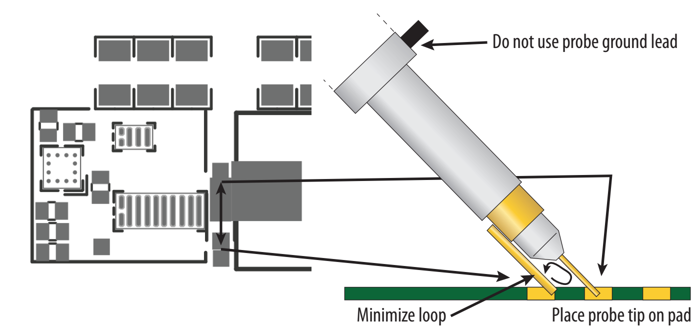


Figure 3: Proper Measurement of Switch Node or Gate Voltage

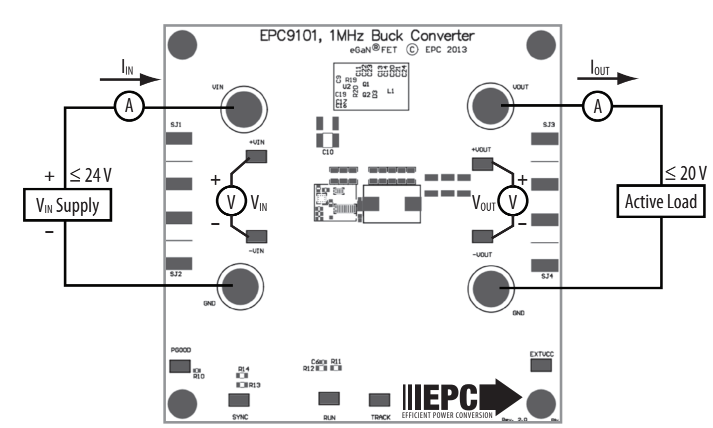
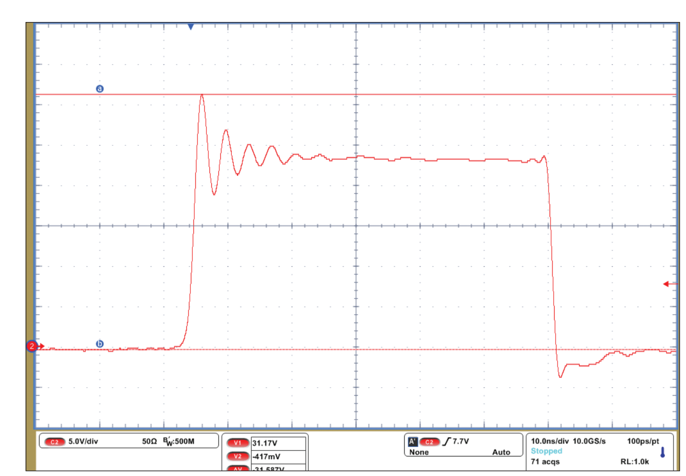


Figure 2: Proper Connection and Measurement Setup



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The EPC9101 demonstration board is 3" square and contains a fully closed loop buck converter. The power stage is a single sided design and is contained within 20mm x 11mm area and includes driver, *eGaN* FETs, bus capacitors and output inductor.

There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1. For more information on the EPC2014/5 *eGaN* FETs or LM5113 driver, please refer to the datasheet available from EPC at www.epc-co.com and www.TI.com. These datasheets, as well that of the LT3833 controller should be read in conjunction with this quick start guide.

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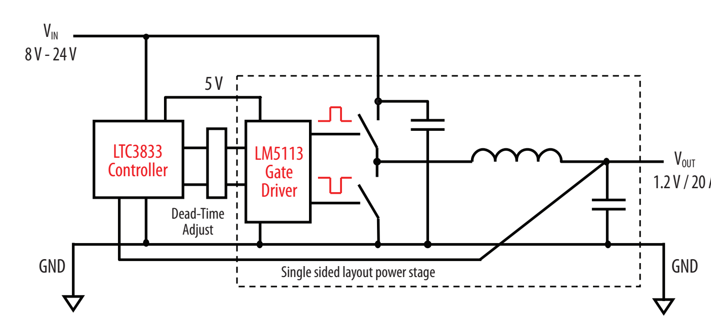

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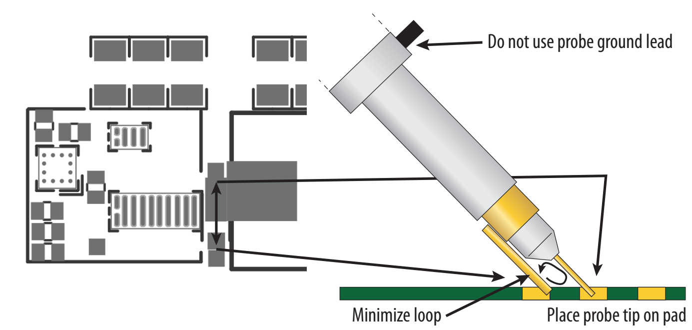

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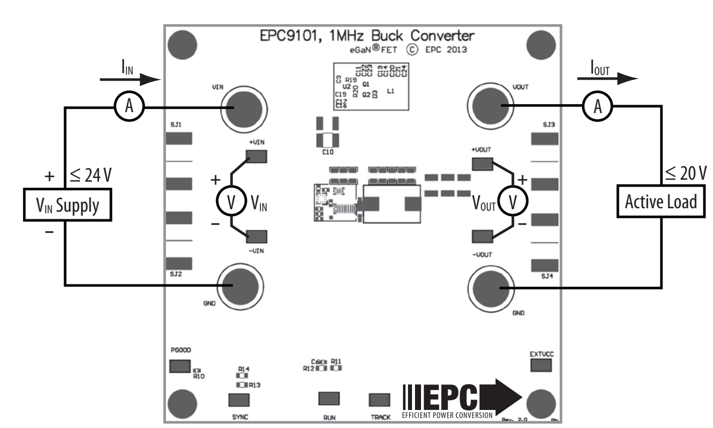

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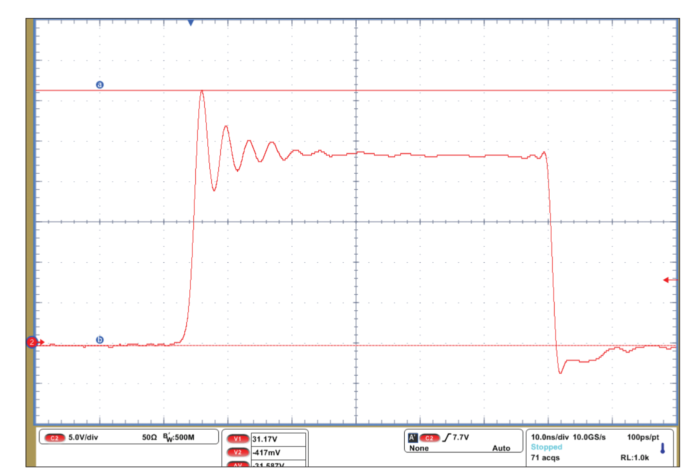

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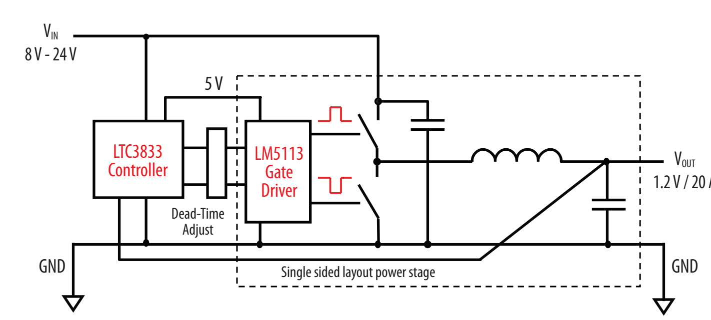

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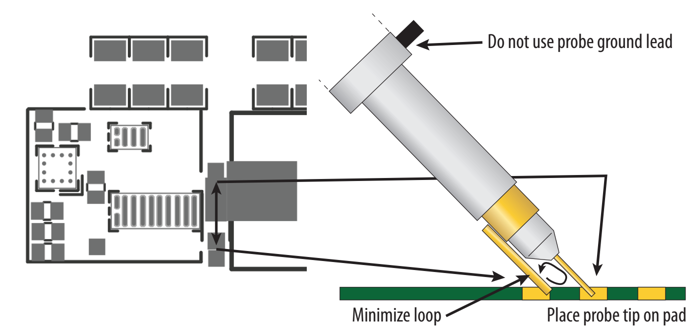

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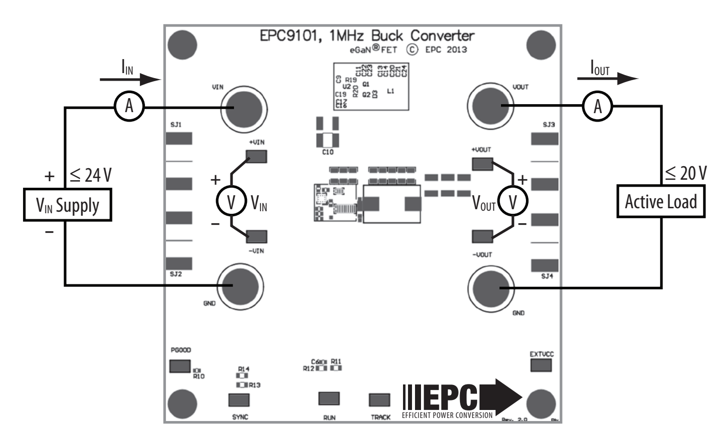

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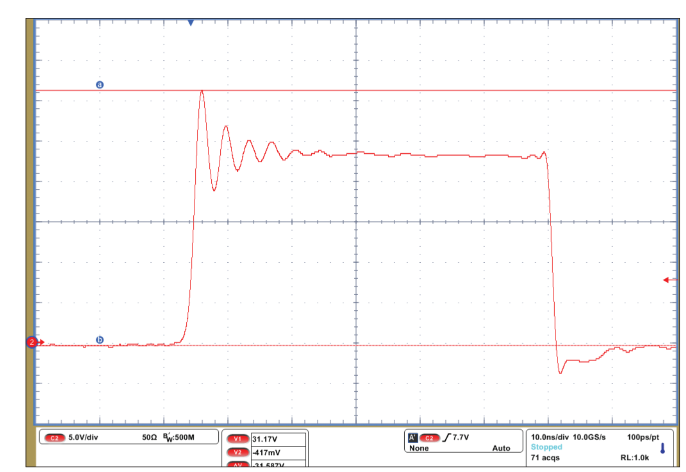

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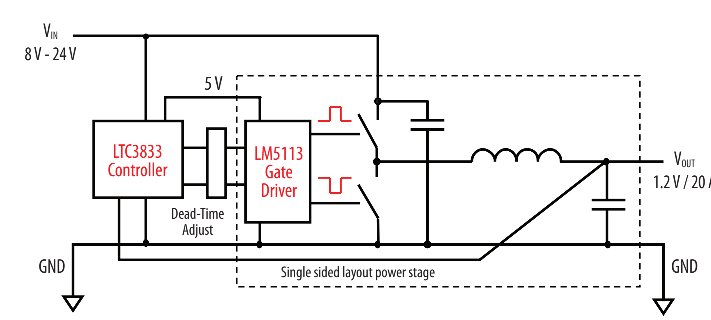

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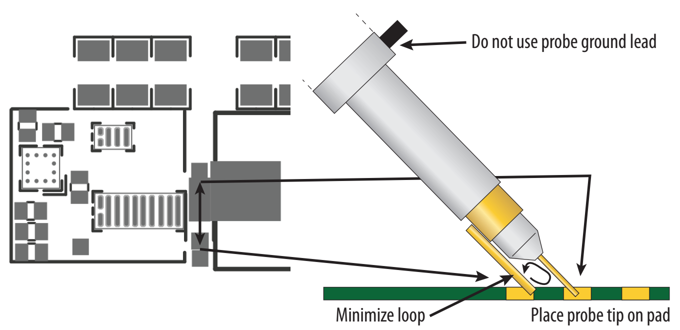

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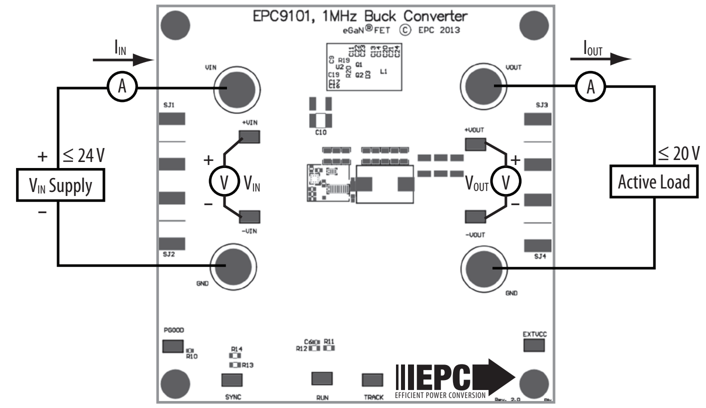

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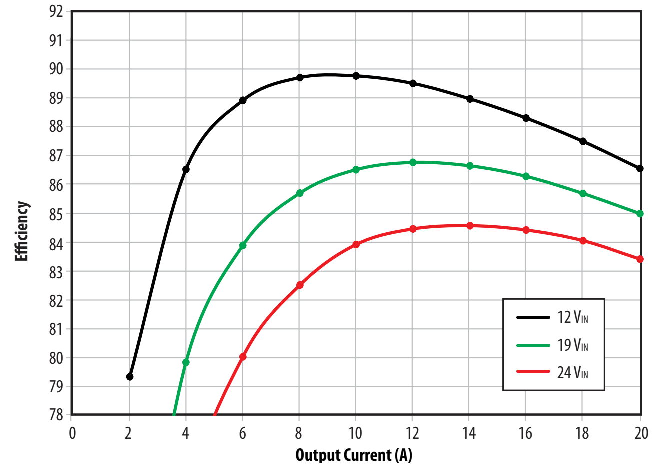
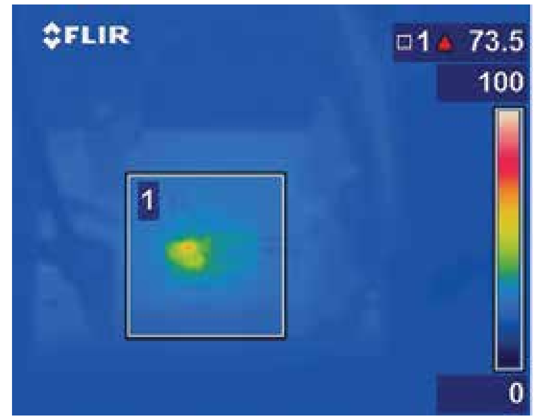


Figure 5: Typical efficiency curves for 24 V, 19 V and 12 V input including controller and LDO losses

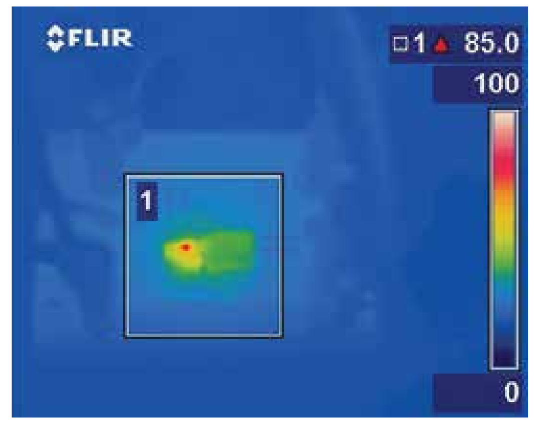
THERMAL CONSIDERATIONS

The EPC9101 demonstration board thermal images for steady state full load operation are shown in Figure 6. The EPC9101 is intended for bench evaluation with low ambient temperature and forced air cooling for higher currents. Care must be taken to not exceed the absolute maximum die temperature of 125°C and stay within the constraints of the other components within the circuit.

NOTE. The EPC9101 demonstration board does not have any current or thermal protection on board.



$12\ V_{IN}$, $20\ A_{OUT}$, 200LFM

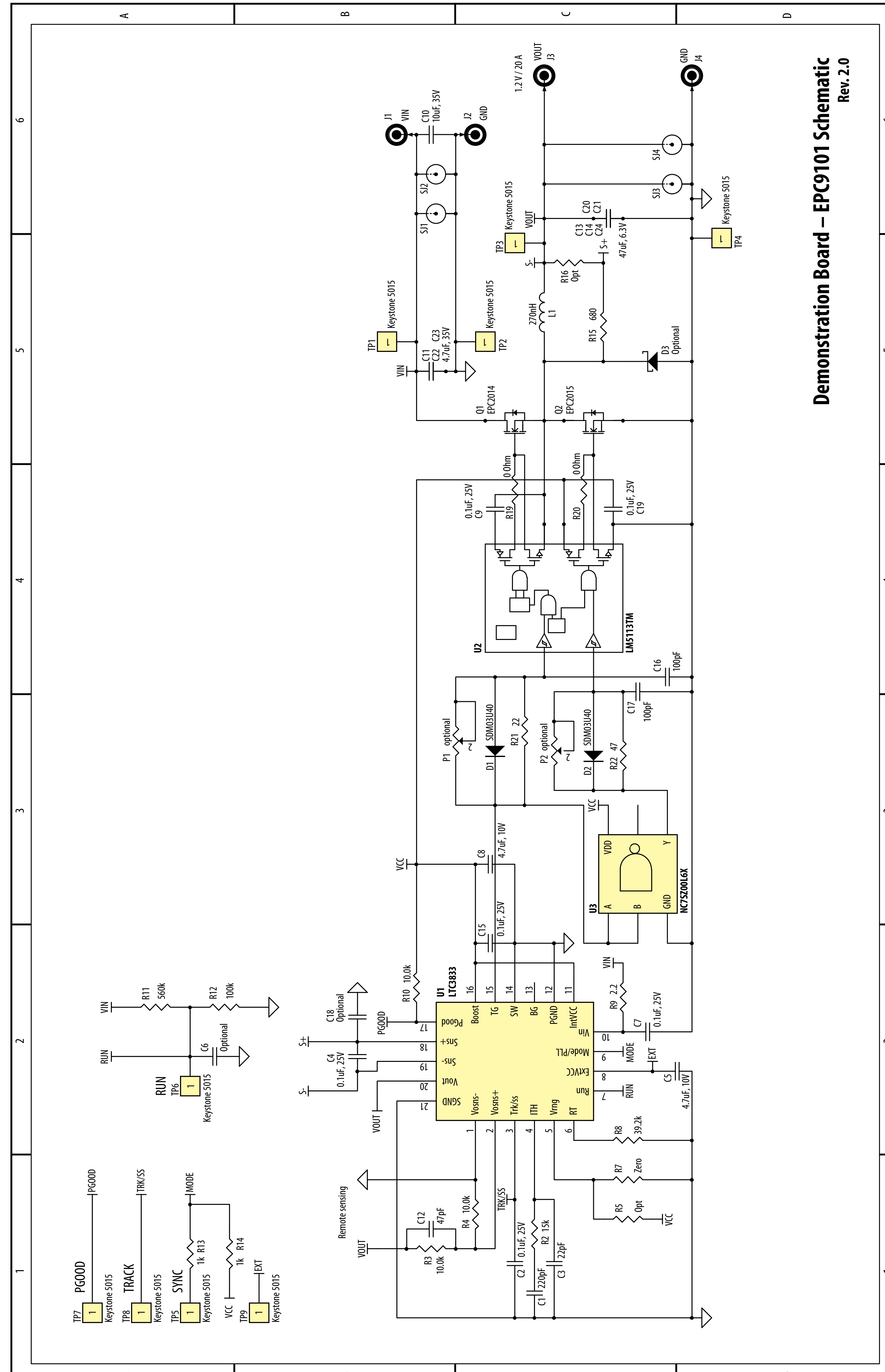


$24\ V_{IN}$, $20\ A_{OUT}$, 200LFM

Figure 6: Thermal images of EPC9101 under full load conditions

Table 2 : Bill of Material

Item	Qty	Reference	Part Description	Manufacturer / Part #
1	1	C1	Capacitor, 220pF, 5%, 50V, NP0	Murata, GRM1885C1H221JA01D
2	1	C3	Capacitor, 22pF, 5%, 50V, NP0	Murata, GRM1885C1H220JA01D
3	6	C2, C4, C7, C9, C15, C19	Capacitor, 0.1uF, 10%, 25V, X5R	TDK, C1005X5R1E104K
4	2	C5, C8	Capacitor, 4.7uF, 10%, 10V, X5R	TDK, C1608X5R1A475K
5	1	C10	Capacitor, 10uF, 20%, 35V, X5R	Taiyo Yuden, GMK325BJ106KN
6	2	C11, C22, C23	Capacitor, 4.7uF, 10%, 35V, X7R	TDK, C2012X6S1V475K125AB
7	5	C13, C14, C20, C21, C24	Capacitor, 47uF, 20%, 10V, X5R	TDK, C2012X5R1A476M
8	2	C16, C17	Capacitor, 100pF, 5%, 50V, NP0	Kemet, C0402C101K5GACTU
9	3	D1, D2, D4	Schottky Diode, 30V	Diodes Inc., SDM03U40-7
10	4	J1, J2, J3, J4	Banana Jack	Keystone, 575-4
11	1	L1	Inductor, 270nH	Coilcraft, SLC1175-271ME
12	1	Q1	eGaN® FET	EPC, EPC2014
13	1	Q2	eGaN® FET	EPC, EPC2015
14	1	R2	Resistor, 15.0K, 1%, 1/8W	Stackpole, RMCF0603FT15K0
15	3	R3, R4, R10	Resistor, 10.0K, 1%, 1/10W	Stackpole, RMCF0603FT10K0
16	3	R7, R19, R20	Resistor, 0 Ohm, 1/16W	Stackpole, RMCF0402ZT0R00
17	1	R8	Resistor, 39.2K, 1%, 1/8W	Stackpole, RMCF0603FT39K2
18	1	R9	Resistor, 2.2 Ohm, 5%, 1/16W	Yageo, RC0402FR-072R2L
19	1	R11	Resistor, 560K, 1%, 1/8W	Stackpole, RMCF0603FT560K
20	1	R12	Resistor, 100K, 1%, 1/8W	Stackpole, RMCF0603FT100K
21	2	R13, R14	Resistor, 1.00K, 5%, 1/10W	Rohm, MCR03EZPJ102
22	1	R15	Resistor, 680 Ohm, 5%, 1/8W	Stackpole, RMCF0603FT680R
23	1	R21	Resistor, 22 Ohm, 5%, 1/8W	Stackpole, RMCF0603JT22R0
24	1	R22	Resistor, 47 Ohm, 5%, 1/8W	Stackpole, RMCF0603JT47R0
25	9	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	Measurement Point	Keystone Elect, 5015
26	1	U1	I.C., Buck Regulator	Linear Technology, LTC3833EUDC#PBF
27	1	U2	I.C., Gate driver	Texas Instruments, LM5113
28	1	U3	I.C., Logic	Fairchild, NC7SZ00L6X
29	4		Nylon Stand-offs	Keystone, 8834
30	0	R5, R16	Optional Resistors	
31	0	C6, C12, C18	Optional Capacitors	
32	0	D3	Optional Diode	
33	0	P1, P2	Potentiometer, 500 Ohm, 0.25W	Murata, PV37Y501C01B00
34	0	SJ1, SJ2, SJ3, SJ4	Optional SMA Connectors	



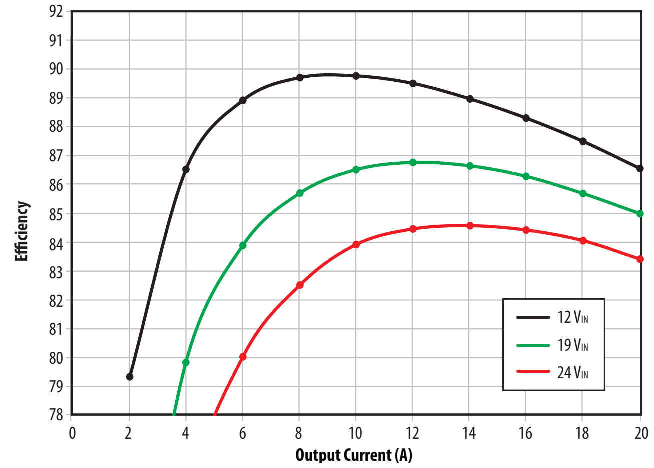
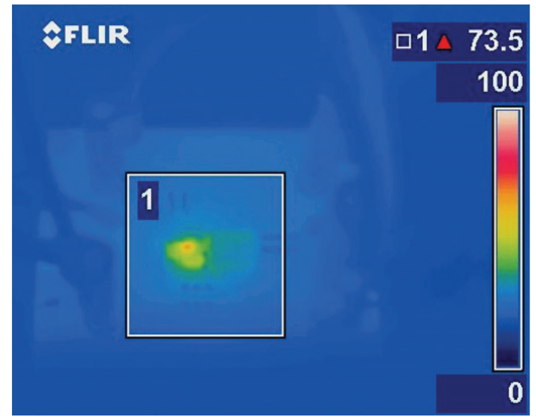


Figure 5: Typical efficiency curves for 24 V, 19 V and 12 V input including controller and LDO losses



12 VIN, 20 AOUT, 200LFM

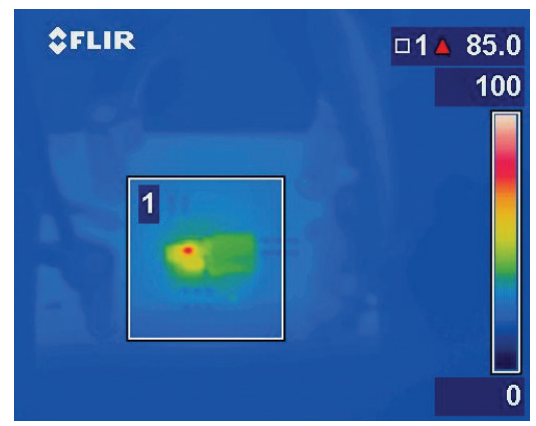


Figure 6: Thermal images of EPC9101 under full load conditions

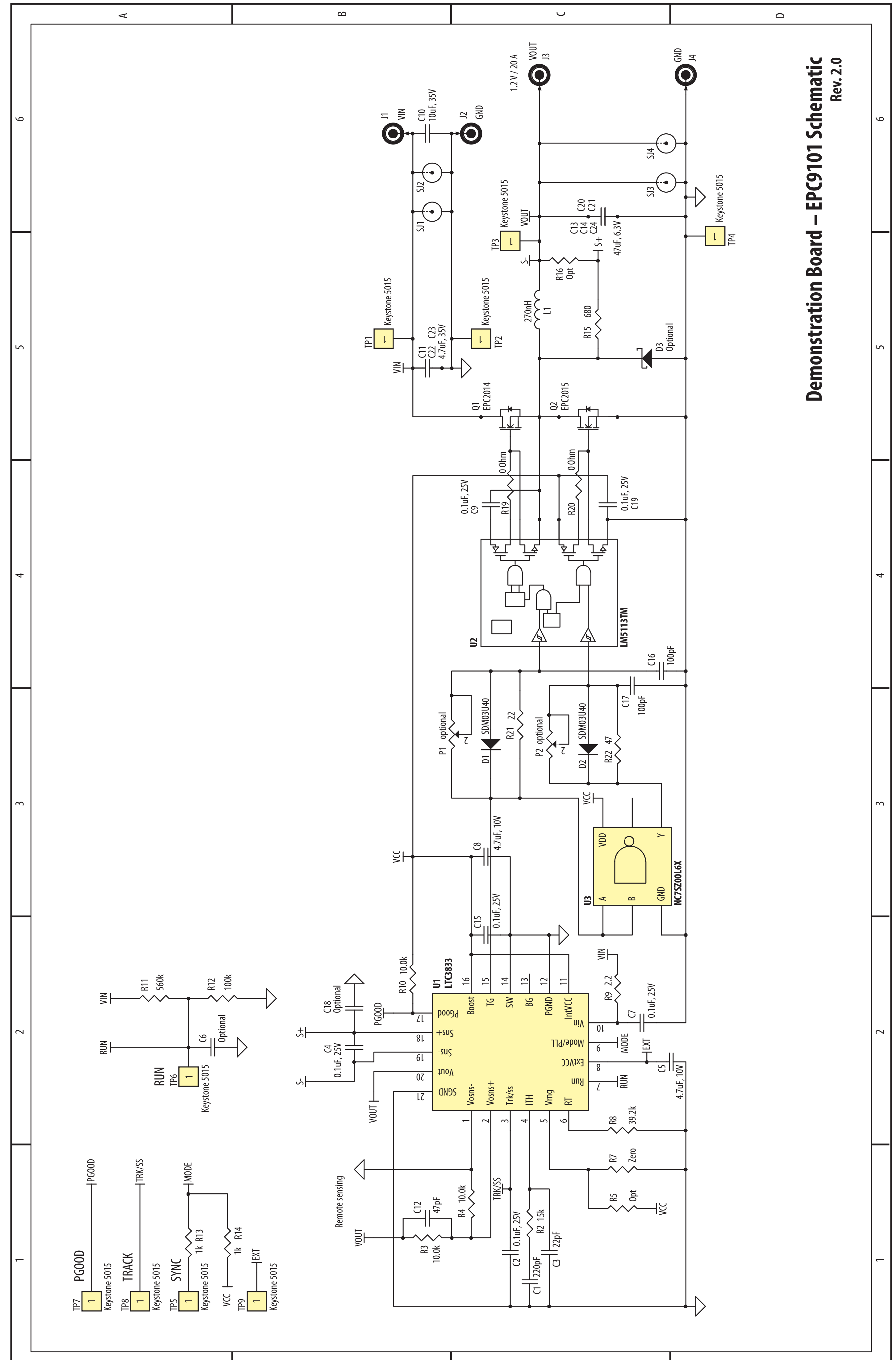
THERMAL CONSIDERATIONS

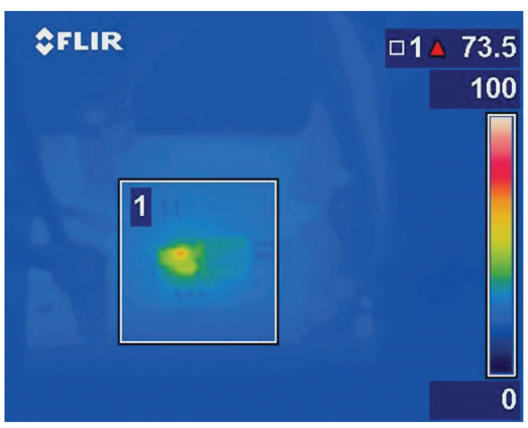
The EPC9101 demonstration board thermal images for steady state full load operation are shown in Figure 6. The EPC9101 is intended for bench evaluation with low ambient temperature and forced air cooling for higher currents. Care must be taken to not exceed the absolute maximum die temperature of 125°C and stay within the constraints of the other components within the circuit.

NOTE. The EPC9101 demonstration board does not have any current or thermal protection on board.

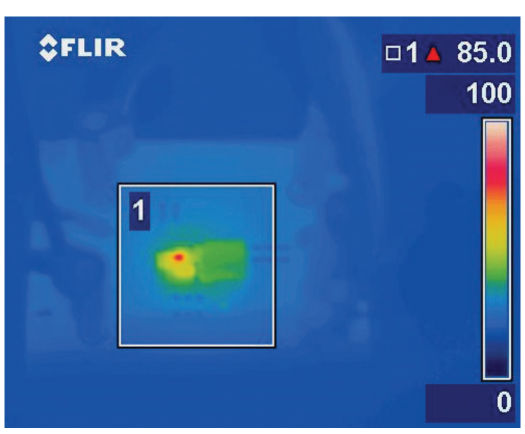
Table 2 : Bill of Material

Item	Qty	Reference	Part Description	Manufacturer / Part #
1	1	C1	Capacitor, 220pF, 5%, 50V, NP0	Murata, GRM1885C1H221JA01D
2	1	C3	Capacitor, 22pF, 5%, 50V, NP0	Murata, GRM1885C1H220JA01D
3	6	C2, C4, C7, C9, C15, C19	Capacitor, 0.1uF, 10%, 25V, X5R	TDK, C1005X5R1E104K
4	2	C5, C8	Capacitor, 4.7uF, 10%, 10V, X5R	TDK, C1608X5R1A475K
5	1	C10	Capacitor, 10uF, 20%, 35V, X5R	Taiyo Yuden, GMK325BJ106KN
6	2	C11, C22, C23	Capacitor, 4.7uF, 10%, 35V, X7R	TDK, C2012X6S1V475K125AB
7	5	C13, C14, C20, C21, C24	Capacitor, 47uF, 20%, 10V, X5R	TDK, C2012X5R1A476M
8	2	C16, C17	Capacitor, 100pF, 5%, 50V, NP0	Kemet, C0402C101K5GACTU
9	3	D1, D2, D4	Schottky Diode, 30V	Diodes Inc., SDM03U40-7
10	4	J1, J2, J3, J4	Banana Jack	Keystone, 575-4
11	1	L1	Inductor, 270nH	Coilcraft, SLC1175-271ME
12	1	Q1	eGaN® FET	EPC, EPC2014
13	1	Q2	eGaN® FET	EPC, EPC2015
14	1	R2	Resistor, 15.0K, 1%, 1/8W	Stackpole, RMCF0603FT15K0
15	3	R3, R4, R10	Resistor, 10.0K, 1%, 1/10W	Stackpole, RMCF0603FT10K0
16	3	R7, R19, R20	Resistor, 0 Ohm, 1/16W	Stackpole, RMCF0402ZT0R00
17	1	R8	Resistor, 39.2K, 1%, 1/8W	Stackpole, RMCF0603FT39K2
18	1	R9	Resistor, 2.2 Ohm, 5%, 1/16W	Yageo, RC0402FR-072R2L
19	1	R11	Resistor, 560K, 1%, 1/8W	Stackpole, RMCF0603FT560K
20	1	R12	Resistor, 100K, 1%, 1/8W	Stackpole, RMCF0603FT100K
21	2	R13, R14	Resistor, 1.00K, 5%, 1/10W	Rohm, MCR03EZPJ102
22	1	R15	Resistor, 680 Ohm, 5%, 1/8W	Stackpole, RMCF0603FT680R
23	1	R21	Resistor, 22 Ohm, 5%, 1/8W	Stackpole, RMCF0603JT22R0
24	1	R22	Resistor, 47 Ohm, 5%, 1/8W	Stackpole, RMCF0603JT47R0
25	9	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	Measurement Point	Keystone Elect, 5015
26	1	U1	I.C., Buck Regulator	Linear Technology, LTC3833EUDC#PBF
27	1	U2	I.C., Gate driver	Texas Instruments, LM5113
28	1	U3	I.C., Logic	Fairchild, NC7SZ00L6X
29	4		Nylon Stand-offs	Keystone, 8834
30	0	R5, R16	Optional Resistors	
31	0	C6, C12, C18	Optional Capacitors	
32	0	D3	Optional Diode	
33	0	P1, P2	Potentiometer, 500 Ohm, 0.25W	Murata, PV37Y501C01B00
34	0	SJ1, SJ2, SJ3, SJ4	Optional SMA Connectors	





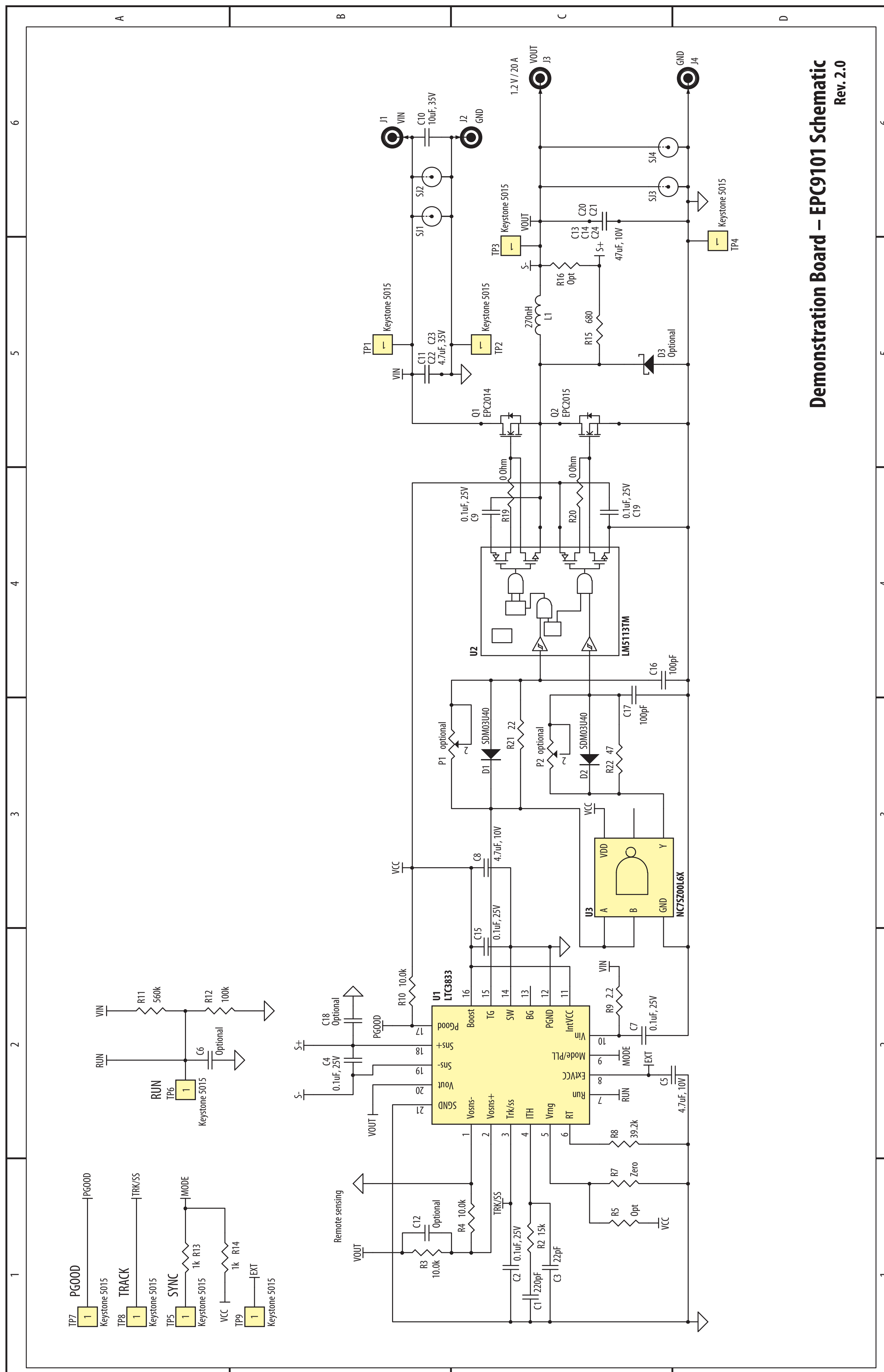
12 V_{IN}, 20 A_{OUT}, 200LFM



24 V_{IN}, 20 A_{OUT}, 200LFM

Figure 6: Thermal images of EPC9101 under full load conditions

iption	Manufacturer / Part #
220pF, 5%, 50V, NP0	Murata, GRM1885C1H221JA01D
22pF, 5%, 50V, NP0	Murata, GRM1885C1H220JA01D
0.1uF, 10%, 25V, X5R	TDK, C1005X5R1E104K
4.7uF, 10%, 10V, X5R	TDK, C1608X5R1A475K
10uF, 20%, 35V, X5R	Taiyo Yuden, GMK325BJ106KN
4.7uF, 10%, 35V, X7R	TDK, C2012X6S1V475K125AB
47uF, 20%, 10V, X5R	TDK, C2012X5R1A476M
100pF, 5%, 50V, NP0	Kemet, C0402C101K5GACTU
iode, 30V	Diodes Inc., SDM03U40-7
k	Keystone, 575-4
70nH	Coilcraft, SLC1175-271ME
	EPC, EPC2014
	EPC, EPC2015
5.0K, 1%, 1/8W	Stackpole, RMCF0603FT15K0
0.0K, 1%, 1/10W	Stackpole, RMCF0603FT10K0
Ohm, 1/16W	Stackpole, RMCF0402ZT0R00
9.2K, 1%, 1/8W	Stackpole, RMCF0603FT39K2
2 Ohm, 5%, 1/16W	Yageo, RC0402FR-072R2L
60K, 1%, 1/8W	Stackpole, RMCF0603FT560K
00K, 1%, 1/8W	Stackpole, RMCF0603FT100K
00K, 5%, 1/10W	Rohm, MCR03EZPJ102
80 Ohm, 5%, 1/8W	Stackpole, RMCF0603FT680R
2 Ohm, 5%, 1/8W	Stackpole, RMCF0603JT22R0
7 Ohm, 5%, 1/8W	Stackpole, RMCF0603JT47R0
ent Point	Keystone Elect, 5015
egulator	Linear Technology, LTC3833EUDC#PBF
river	Texas Instruments, LM5113
	Fairchild, NC7SZ00L6X
d-offs	Keystone, 8834
esistors	
apacitors	
iode	
eter, 500 Ohm, 0.25W	Murata, PV37Y501C01B00
MA Connectors	



Quick Start Procedure

Demonstration board EPC9101 is easy to set up to evaluate the performance of the EPC2014 and EPC2015 *eGaN* FETs and LM5113 driver. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus between V_{IN} and GND banana jacks as shown.
2. With power off, connect the active (constant current) load as desired between V_{OUT} and GND banana jacks as shown.
3. Turn on the supply voltage to the required value (do not exceed the absolute maximum voltage of 24 V on V_{IN}).
4. Measure the output voltage to make sure the board is fully functional and operating no-load.
5. Turn on active load to the desired load current while staying below the maximum current (20 A)
6. Once operational, adjust the bus voltage and load current within the allowed operating range and observe the output switching behavior, efficiency and other parameters.
7. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node of gate voltage, care must be taken to avoid long ground leads. Measure these by placing the oscilloscope probe tip on the top pad of D3 and grounding the probe directly across D3 on the bottom pad provided for switch node and using the bottom pad of R20 and the GND pad below it for gate voltage. See Figure 3 for proper scope probe technique. Measuring the switch node with a high bandwidth (≥ 500MHz) probe and high bandwidth scope (≥ 1GHz) is recommended.

NOTE. The dead-times for both the leading and trailing edges have been set for optimum full load efficiency. Adjustment is not recommended, but can be done at own risk by replacing R21 and R22 with potentiometers P1 and P2. This should be done while monitoring both the input current and switch-node voltage to determine the effect of these adjustments. Under no circumstance should the input pins to the LM5113 be probed during operation as the added probe capacitance will change the device timing.

CIRCUIT PERFORMANCE

The EPC9101 demonstration circuit was designed to showcase the size and performance that can readily be achieved at 1 MHz operation using *eGaN* FETs for supply voltages up to 24V or more. Since a closed loop controller is included on board, the associated losses must also be lumped into any efficiency measurement that is performed. It is possible to supply a separate regulated 5V supply to the EXTVCC pin to further improve efficiency. In that case, the controller and gate drive losses are still included, but the associated conversion loss from the input supply (LDO loss) is removed.

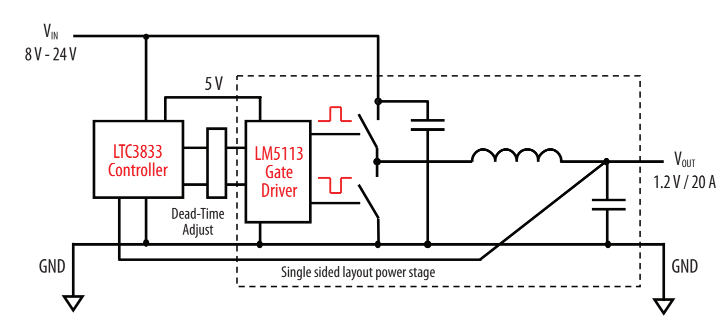


Figure 1: Block Diagram of EPC9101 Demonstration Board

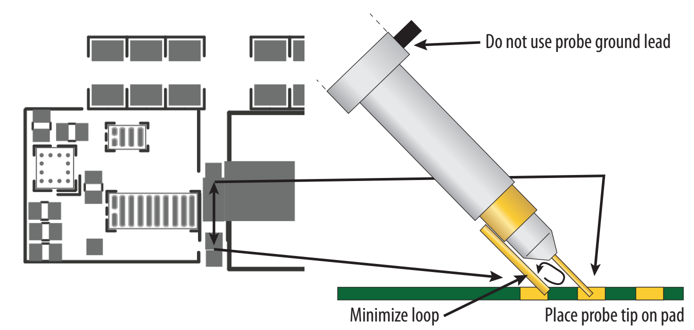


Figure 3: Proper Measurement of Switch Node or Gate Voltage

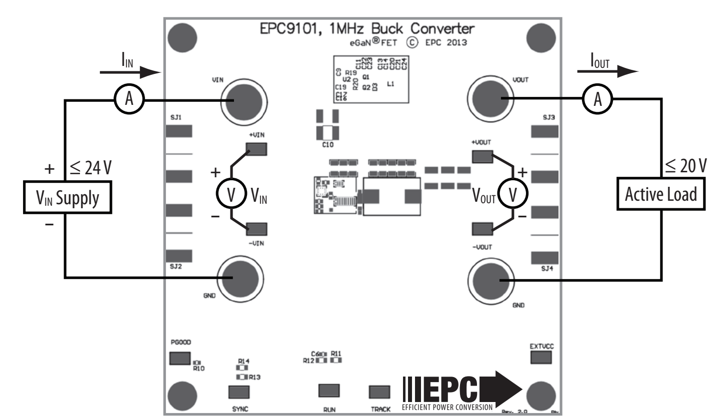


Figure 2: Proper Connection and Measurement Setup

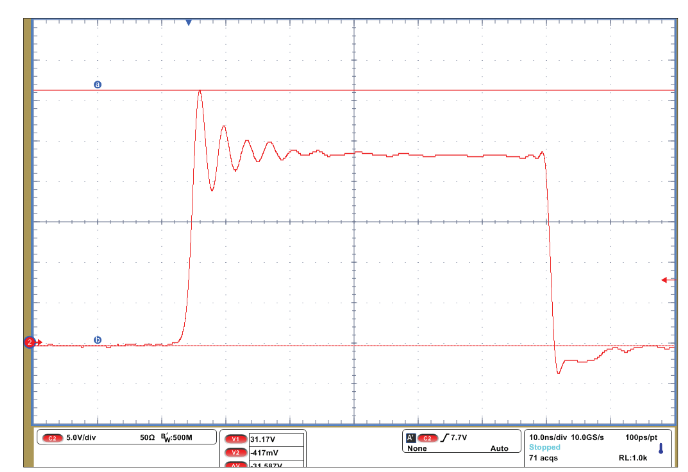


Figure 4: Typical Switch node voltage for a 24 V to 1.2 V/20 A (1 MHz) Buck converter

DESCRIPTION

www.epc-co.com

The EPC9101 demonstration board is a 1.2 V output, 1 MHz buck converter with an 20 A maximum output current and 8 V to 24 V input voltage range. The demonstration board features the EPC2014 and EPC2015 enhancement mode (*eGaN*®) field effect transistors (FETs), as well as the first *eGaN* FET specific integrated circuit driver – the Texas Instruments LM5113. The EPC9101 board is not intended as a reference design, but to showcase the performance that can be achieved using the *eGaN* FETs and *eGaN* driver together.

The EPC9101 demonstration board is 3" square and contains a fully closed loop buck converter.

There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1. For more information on the EPC2014/5 *eGaN* FETs or LM5113 driver, please refer to the datasheet available from EPC at www.epc-co.com and www.TI.com. These datasheets, as well that of the LT3833 controller should be read in conjunction with this quick start guide.

Table 1: Performance Summary (TA = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Bus Input Voltage Range		8		24	V
V_{OUT}	Switch Node Output Voltage			1.2		V
I_{OUT}	Switch Node Output Current				20*	A
f_{SW}	Switching frequency			1000		kHz
	Peak Efficiency	$12\ V_{IN}$, = $10\ A\ I_{OUT}$		89.5		%
	Full Load Efficiency	$12\ V_{IN}$, = $20\ A\ I_{OUT}$		86.4		%
	Full Load Efficiency	$24\ V_{IN}$, = $20\ A\ I_{OUT}$		83.3		%

*Maximum limited by thermal considerations and requires 200 LFM forced air cooling

Demonstration Board EPC9101 Quick Start Guide

EPC2014 + EPC2015 1 MHz Buck Converter

EFFICIENT POWER CONVERSION

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