

SYMBOL		PARAMETER		CONDITIONS		MIN		TYP		MAX		UNITS	
V_{IN}		Bus Input Voltage Range		9		28							V
V_{OUT}		Switch Node Output Voltage		3.3									V
I_{OUT}		Switch Node Output Current		15*									A
f_{SW}		Switching Frequency		1000									KHz
		Peak Efficiency		12 V _{IN} , 10 A _{OUT}		96.1							%
		Peak Efficiency		28 V _{IN} , 12 A _{OUT}		93.5							%
		Full Load Efficiency		12 V _{IN} , 15 A _{OUT}		95.6							%
		Full Load Efficiency		28 V _{IN} , 15 A _{OUT}		93.3							%

* Maximum limited by inductor saturation

Table 1: Performance Summary (TA = 25 °C)

The EPC9107 demonstration board is a 3.3 V output, 1 MHz buck converter with an 15 A maximum output current and 9 V to 28 V input voltage range. The demonstration board features the EPC2015 enhancement mode (eGaN®) field effect transistor (FET), as well as the Texas Instruments LM5113 gate driver. The EPC9107 board contains the complete power stage (including eGaN FETs, driver, inductor and input/output caps) in a compact 1/2" x 1/2" layout to showcase the performance that can be achieved using the eGaN FETs and eGaN driver together.

There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1. For more information on the EPC2015 eGaN FETs or LM5113 driver, please refer to the datasheet available from EPC at www.epc-co.com and www.ti.com. These datasheets, as well as that of the LT3833 controller should be read in conjunction with this quick start guide.

DESCRIPTION

www.epc-co.com

Quick Start Procedure

Demonstration board EPC9107 is easy to set up to evaluate the performance of the EPC2015 eGaN FETs and LM5113 driver. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus between V_{IN} and GND banana jacks as shown.
2. With power off, connect the active (constant current) load as desired between V_{OUT} and GND banana jacks as shown.
3. Turn on the supply voltage to the required value (more than 9V, but do not exceed the absolute maximum voltage of 28 V on V_{IN}).
4. Measure the output voltage to make sure the board is fully functional and operating no-load.
5. Turn on active load to the desired load current while staying below the maximum current (15 A)
6. Once operational, adjust the bus voltage and load current within the allowed operating range and observe the output switching behavior, efficiency and other parameters.
7. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node or gate voltage, care must be taken to avoid long ground leads. Measure these by placing the oscilloscope probe tip on the top pad of D3 and grounding the probe directly across D3 on the bottom pad provided for switch node and using the right hand pad of R24 and the GND pad below it for gate voltage. See Figure 3 for proper scope probe technique. Measuring the switch node with a high bandwidth ($\geq 500\text{MHz}$) probe and high bandwidth scope ($\geq 1\text{GHz}$) is recommended.

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CIRCUIT PERFORMANCE

The EPC9107 demonstration circuit was designed to showcase the size and performance that can readily be achieved at 1 MHz operation using eGaN FETs for supply voltages up to 28V or more. Since a closed loop controller is included on board, the associated losses must also be lumped into any efficiency measurement that is performed. In an effort to mitigate these losses and focus on the efficiency of the power stage, the controller is powered from the output through an unregulated charge pump supplied from the output. Thus the controller and gate drive losses are still included, but the associated conversion loss from the input supply is improved.

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Demonstration Board EPC9107

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28 V Buck Converter featuring EPC2015

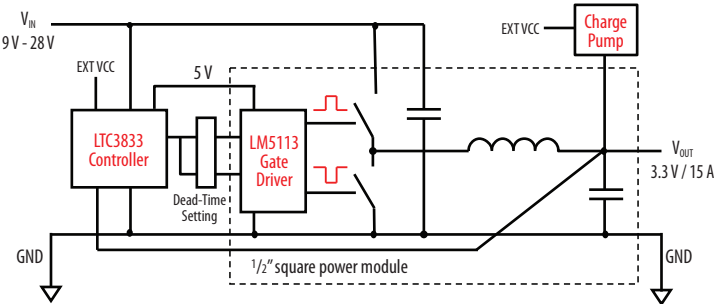


Figure 1: Block Diagram of EPC9107 Demonstration Board

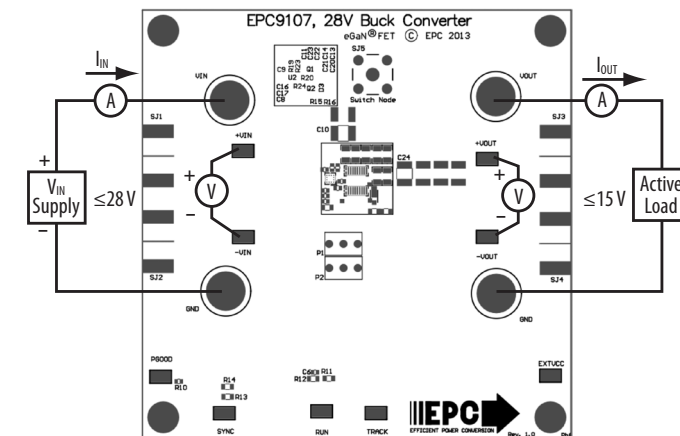


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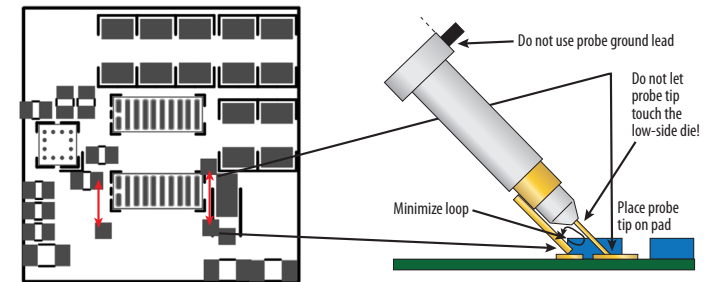


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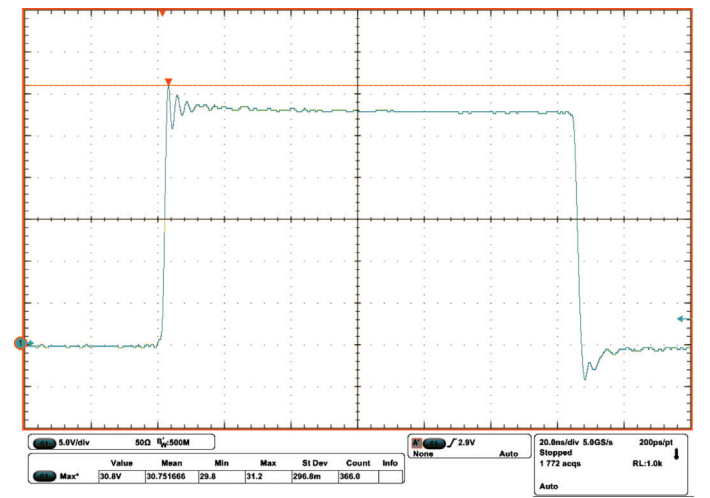


Figure 4: Typical waveforms for 28 V to 3.3 V / 15 A (1 MHz) CH1: Switch node voltage

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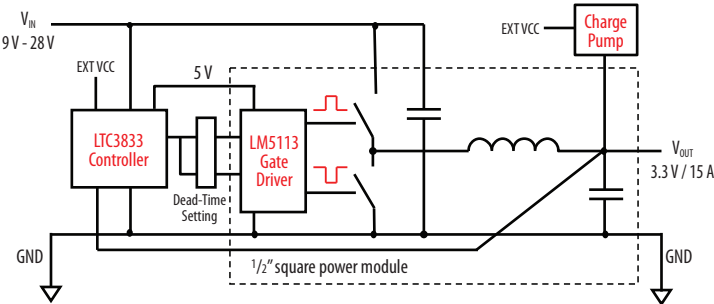


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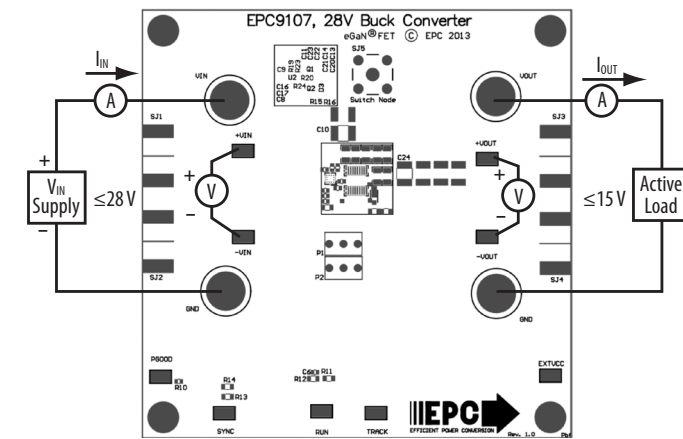


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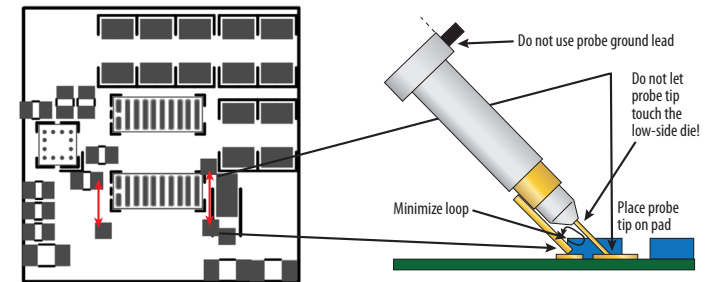


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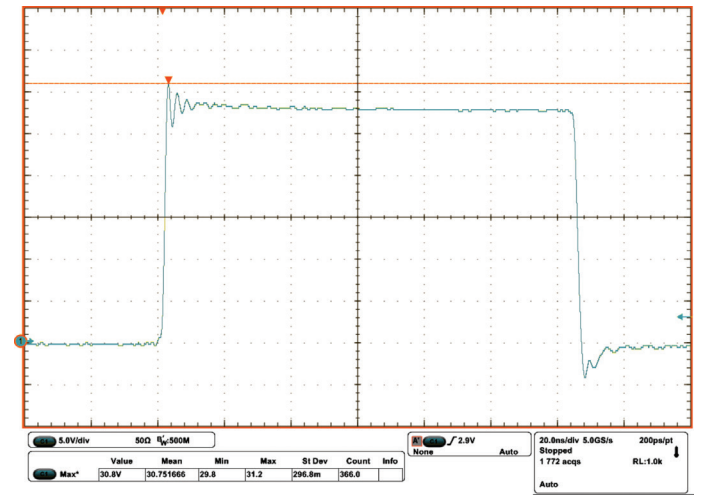


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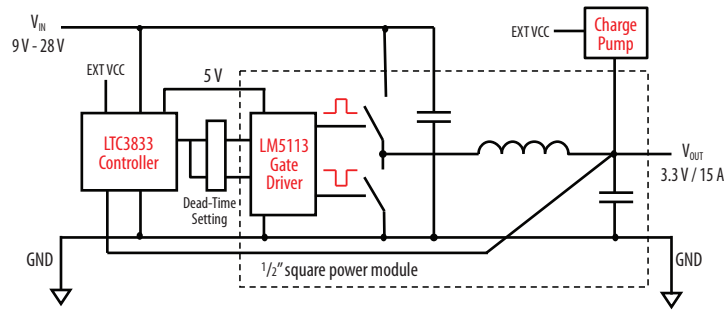


Figure 1: Block Diagram of EPC9107 Demonstration Board

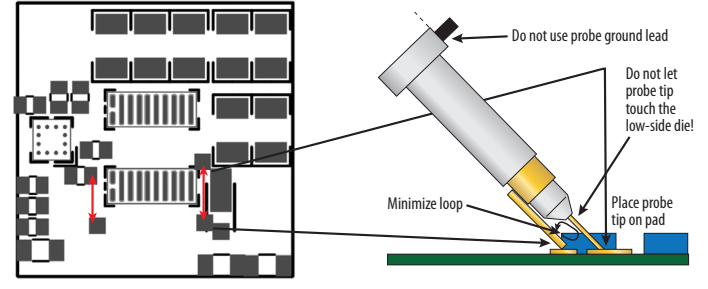


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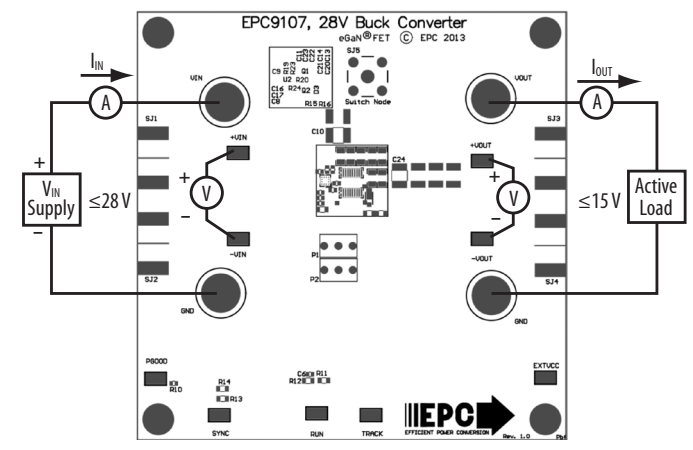


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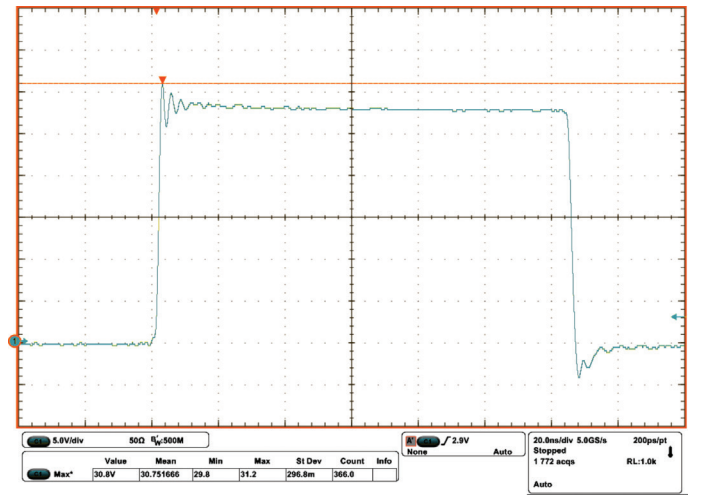


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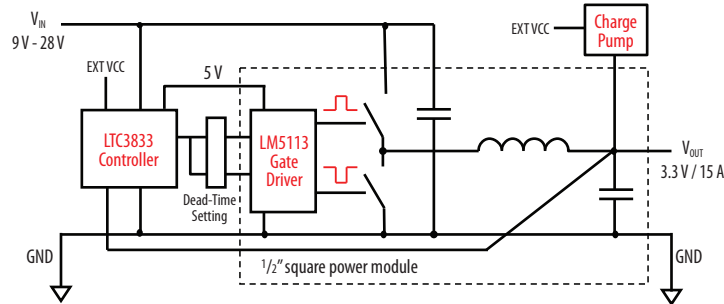


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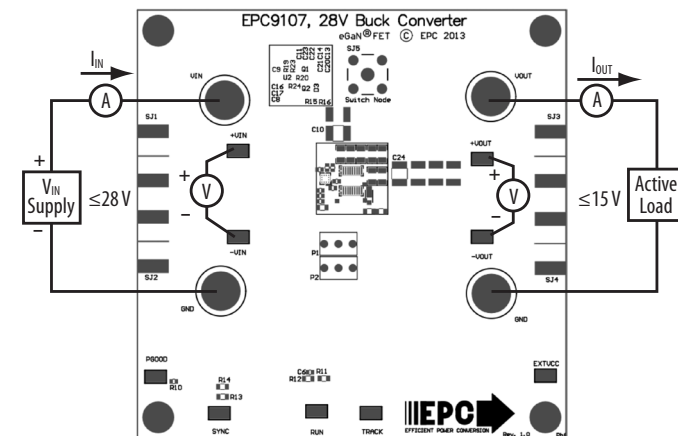


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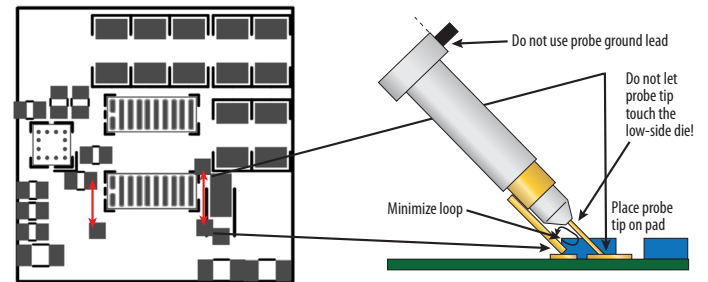


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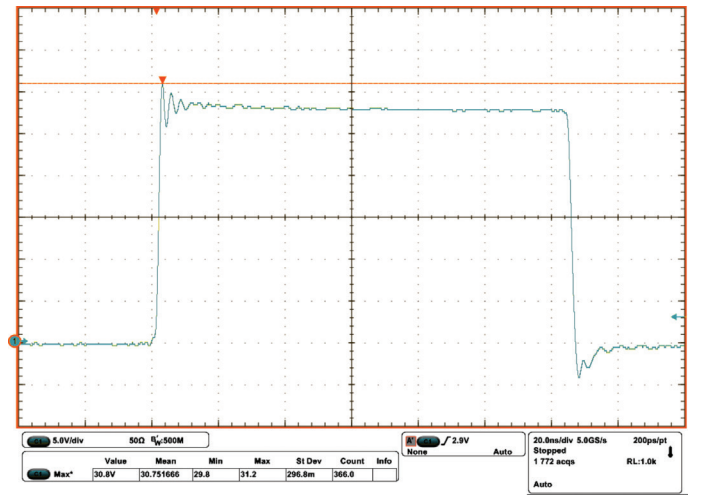


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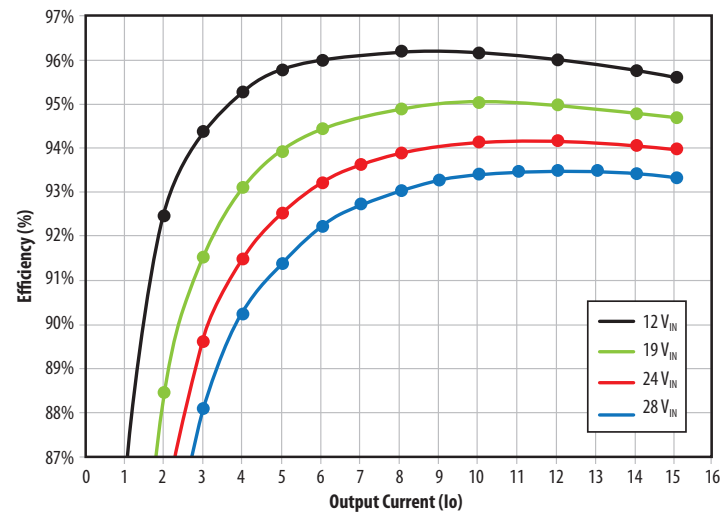


Figure 5: Typical efficiency and power loss curves for 12V, 19V, 24V and 28V input

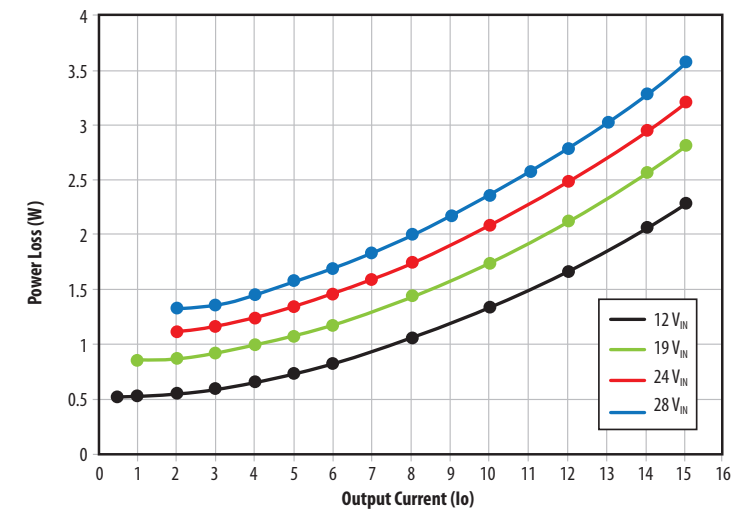


Figure 6: Thermal image of EPC9107 under full load condition: 28 Vin, 15 Aout with convection cooling

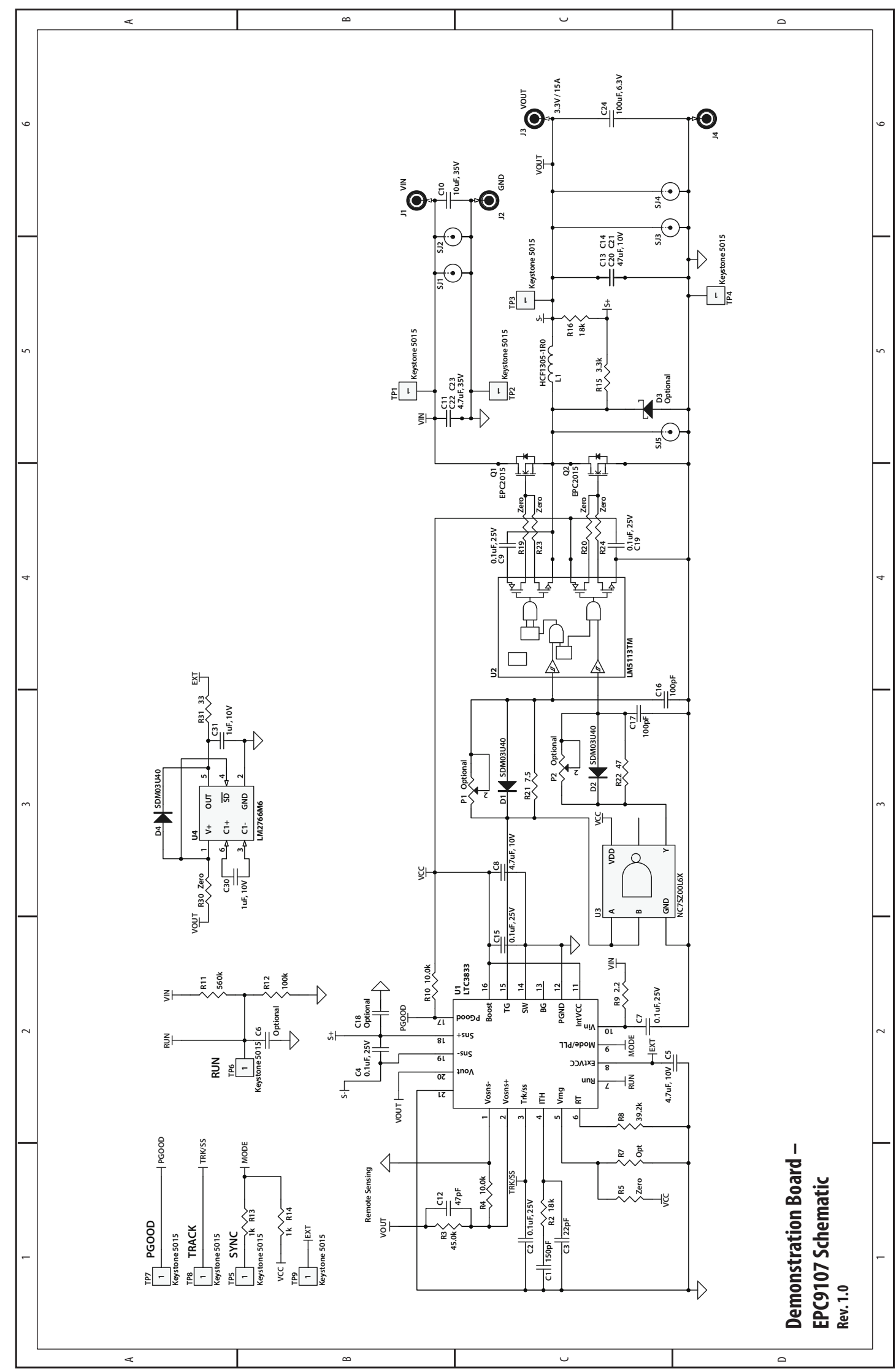
THERMAL CONSIDERATIONS

The EPC9107 demonstration board thermal image for steady state full load operation is shown in Figure 6. The EPC9107 is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling could increase the current capability of the demonstration circuit, but care must be taken to not exceed the absolute maximum die temperature of 125°C and stay within the constraints of the other components within the circuit, most notably the saturation of the output inductor.

NOTE: The EPC9107 demonstration board does not have any thermal protection on board.

Table 2 : Bill of Material

Item	Qty	Reference	Part Description	Manufacturer / Part #
1	1	C1	Capacitor, 150pF, 5%, 50V, NP0	Murata, GRM1885C1H151JA01D
2	1	C3	Capacitor, 22pF, 5%, 50V, NP0	Murata, GRM1885C1H220JA01D
3	1	C12	Capacitor, 47pF, 5%, 50V, NP0	TDK, C1608C0G1H470J
4	6	C2, C4, C7, C9, C15, C19	Capacitor, 0.1uF, 10%, 25V, X5R	TDK, C1005X5R1E104K
5	2	C5, C8	Capacitor, 4.7uF, 10%, 10V, X5R	TDK, C1608X5R1A475K
6	1	C10	Capacitor, 10uF, 20%, 35V, X5R	Taiyo Yuden, GMK325BJ106KN
7	2	C11, C22, C23	Capacitor, 4.7uF, 10%, 35V, X7R	TDK, C2012X6S1V475K125AB
8	4	C13, C14, C20, C21	Capacitor, 47uF, 20%, 10V, X5R	TDK, C2012X5R1A476M
9	2	C16, C17	Capacitor, 100pF, 5%, 50V, NP0	Kemet, C0402C101K5GACTU
10	1	C24	Capacitor, 100uF, 20%, 6.3V, X5R	Kemet, C1206C107M9PACTU
11	2	C30, C31	Capacitor, 1uF, 20%, 10V, X5R	TDK, C1005X5R1A105K050BB
12	2	D1, D2, D4	Schottky Diode, 30V	Diodes Inc., SDM03U40-7
13	4	J1, J2, J3, J4	Banana Jack	Keystone, 575-4
14	1	L1	Inductor, 1.0uH, 22A	Cooper Bussman, HCF1305-1R0-R
15	2	Q1, Q2	eGaN® FET	EPC, EPC2015
16	1	R3	Resistor, 45.0k, 1%, 1/8W	Stackpole, RMCF0603FT45K3
17	2	R4, R10	Resistor, 10.0k, 1%, 1/10W	Panasonic, ERJ-2RKF1002X
18	6	R5, R19, R20, R23, R24, R30	Resistor, 0 Ohm, 1/16W	Stackpole, RMCF0402ZT0R00
19	1	R31	Resistor, 39 Ohm, 1%, 1/16W	Stackpole, RMCF0402FT39R0
20	1	R8	Resistor, 39.2k, 1%, 1/8W	Stackpole, RMCF0603FT39K2
21	1	R2	Resistor, 18.0k, 1%, 1/8W	Stackpole, RMCF0603FT18K0
22	1	R9	Resistor, 2.2 Ohm, 5%, 1/16W	Yageo, RC0402FR-072R2L
23	1	R11	Resistor, 560k, 1%, 1/8W	Stackpole, RMCF0603FT560K
24	1	R12	Resistor, 100k, 1%, 1/8W	Stackpole, RMCF0603FT100K
25	2	R13, R14	Resistor, 1.00k, 5%, 1/10W	Rohm, MCR03EZPJ102
26	1	R15	Resistor, 3.3k, 5%, 1/8W	Stackpole, RMCF0603JT3K30
27	1	R21	Resistor, 7.5 Ohm, 5%, 1/16W	Stackpole, RMCF0603JT7R50
28	1	R22	Resistor, 47 Ohm, 5%, 1/16W	Stackpole, RMCF0603JT47R0
29	9	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	Measurement Point	Keystone Elect, 5015
30	1	U1	I.C., Buck Regulator	Linear Technology, LTC3833EUDC#PBF
31	1	U2	I.C., Gate Driver	Texas Instruments, LM5113
32	1	U3	I.C., Logic	Fairchild, NC7SZ00L6X
33	1	U4	I.C., Charge Pump	Texas Instruments, LM2766M6
34	4		Nylon Stand-offs	Keystone, 8834
35	0	P1, P2	Optional Potentiometer, 500 Ohm, 0.25W	
36	0	R7, R16	Optional Resistors	
37	0	C6, C18	Optional Capacitors	
38	0	SJ5	Optional Scope Jack	
39	0	D3	Optional Diode	
40	0	SJ1, SJ2, SJ3, SJ4	Optional SMA connectors	



Demonstration Board - EPC9107 Schematic Rev. 1.0

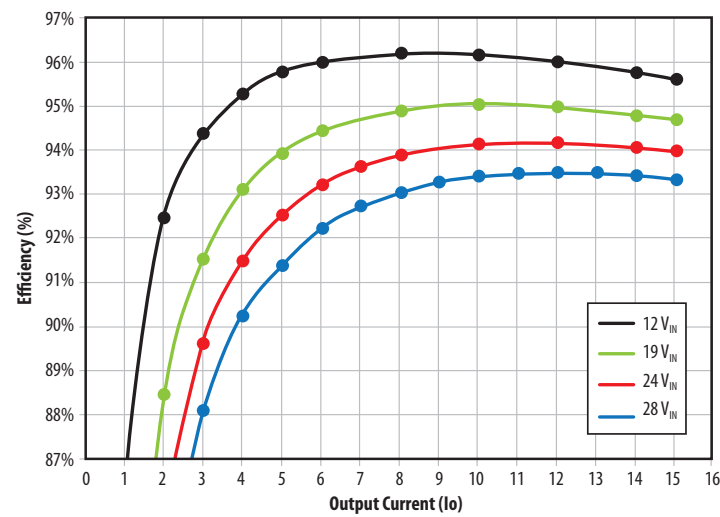


Figure 5: Typical efficiency and power loss curves for 12V, 19V, 24V and 28V input

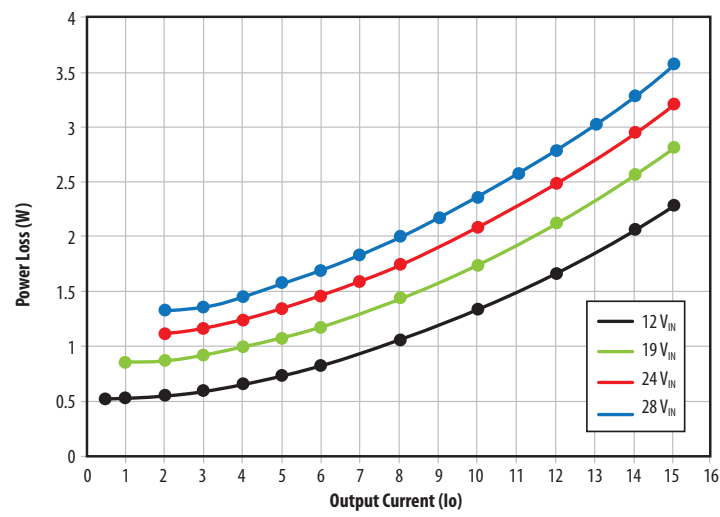


Figure 6: Thermal image of EPC9107 under full load condition: 28 V_{in} , 15 A_{out} with convection cooling

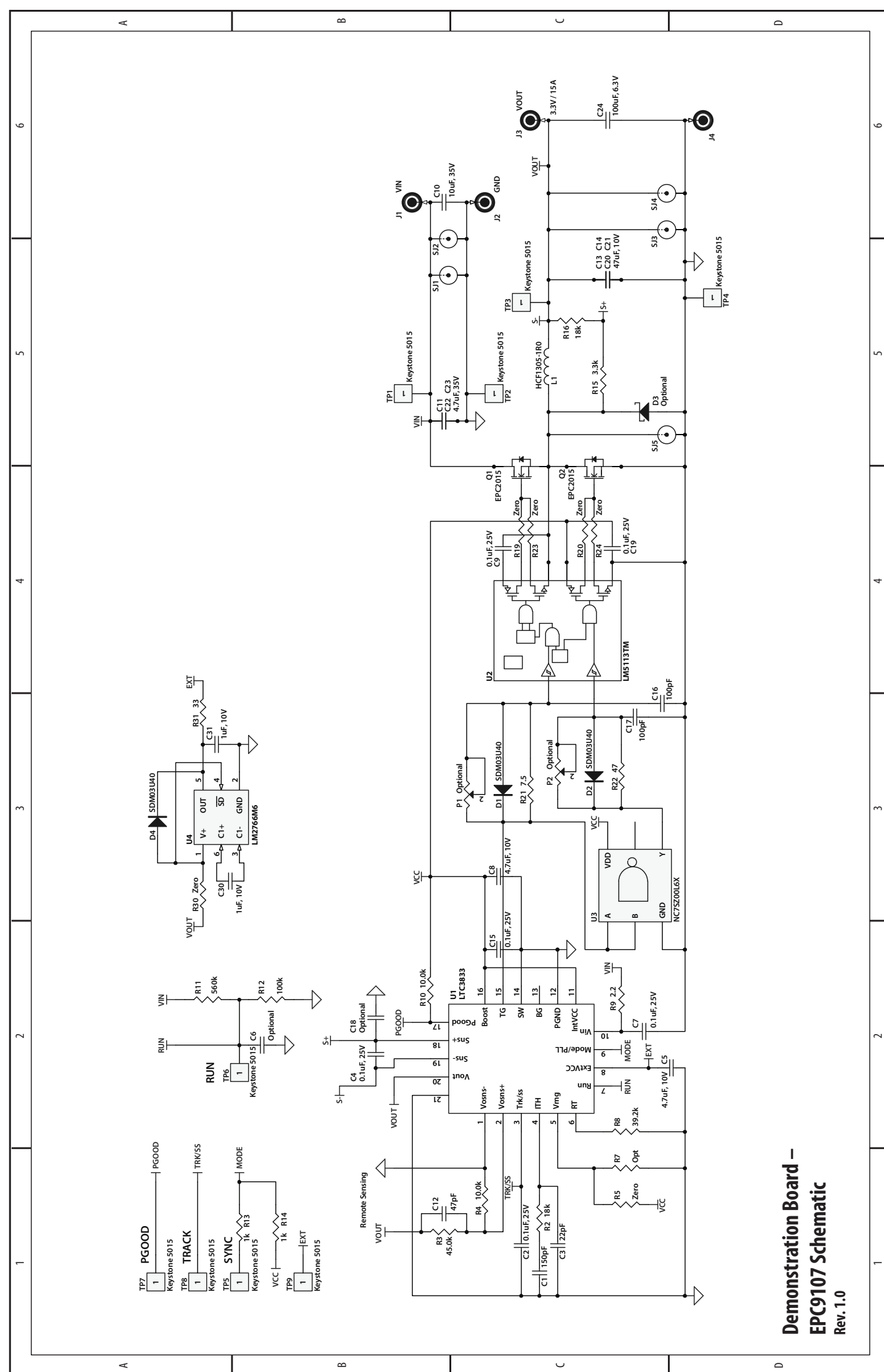
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5	2	C5, C8	Capacitor, 4.7uF, 10%, 10V, X5R	TDK, C1608X5R1A475K
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10	1	C24	Capacitor, 100uF, 20%, 6.3V, X5R	Kemet, C1206C107M9PACTU
11	2	C30, C31	Capacitor, 1uF, 20%, 10V, X5R	TDK, C1005X5R1A105K050BB
12	2	D1, D2, D4	Schottky Diode, 30V	Diodes Inc., SDM03U40-7
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39	0	D3	Optional Diode	
40	0	SJ1, SJ2, SJ3, SJ4	Optional SMA connectors	



SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Bus Input Voltage Range		9	28		V
V_{OUT}	Switch Node Output Voltage		3.3			V
I_{OUT}	Switch Node Output Current		15*			A
f_{SW}	Switching Frequency		1000			KHz
	Peak Efficiency	$12 V_{IN}, 10 A_{OUT}$	96.1			%
	Peak Efficiency	$28 V_{IN}, 12 A_{OUT}$	93.5			%
	Full Load Efficiency	$12 V_{IN}, 15 A_{OUT}$	95.6			%
	Full Load Efficiency	$28 V_{IN}, 15 A_{OUT}$	93.3			%

* Maximum limited by inductor saturation

Table 1: Performance Summary (TA = 25 °C)

The EPC9107 demonstration board is a 3.3 V output, 1 MHz buck converter with an 15 A maximum output current and 9 V to 28 V input voltage range. The demonstration board features the EPC2015 enhancement mode (eGaN®) field effect transistor (FET), as well as the Texas Instruments LM5113 gate driver. The EPC9107 board contains the complete power stage (including eGaN FETs, driver, inductor and input/output caps) in a compact 1/2" x 1/2" layout to showcase the performance that can be achieved using the eGaN FETs and eGaN driver together.

There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1. For more information on the EPC2015 eGaN FETs or LM5113 driver, please refer to the datasheet available from EPC at www.epc-co.com and www.ti.com. These datasheets, as well as that of the LT3833 controller should be read in conjunction with this quick start guide.

DESCRIPTION

www.epc-co.com

Quick Start Procedure

Demonstration board EPC9107 is easy to set up to evaluate the performance of the EPC2015 eGaN FETs and LM5113 driver. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus between V_{IN} and GND banana jacks as shown.
2. With power off, connect the active (constant current) load as desired between V_{OUT} and GND banana jacks as shown.
3. Turn on the supply voltage to the required value (more than 9V, but do not exceed the absolute maximum voltage of 28 V on V_{IN}).
4. Measure the output voltage to make sure the board is fully functional and operating no-load.
5. Turn on active load to the desired load current while staying below the maximum current (15 A)
6. Once operational, adjust the bus voltage and load current within the allowed operating range and observe the output switching behavior, efficiency and other parameters.
7. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node of gate voltage, care must be taken to avoid long ground leads. Measure these by placing the oscilloscope probe tip on the top pad of D3 and grounding the probe directly across D3 on the bottom pad provided for switch node and using the right hand pad of R24 and the GND pad below it for gate voltage. See Figure 3 for proper scope probe technique. Measuring the switch node with a high bandwidth ($\geq 500\text{MHz}$) probe and high bandwidth scope ($\geq 1\text{GHz}$) is recommended.

NOTE. The dead-times for both the leading and trailing edges have been set for optimum full load efficiency. Adjustment is not recommended, but can be done at own risk by replacing R21 and R22 with potentiometers P1 and P2. This should be done while monitoring both the input current and switch-node voltage to determine the effect of these adjustments. Under no circumstance should the input pins to the LM5113 be probed during operation as the added probe capacitance will change the device timing.

CIRCUIT PERFORMANCE

The EPC9107 demonstration circuit was designed to showcase the size and performance that can readily be achieved at 1 MHz operation using eGaN FETs for supply voltages up to 28V or more. Since a closed loop controller is included on board, the associated losses must also be lumped into any efficiency measurement that is performed. In an effort to mitigate these losses and focus on the efficiency of the power stage, the controller is powered from the output through an unregulated charge pump supplied from the output. Thus the controller and gate drive losses are still included, but the associated conversion loss from the input supply is improved.

EPC

EFFICIENT POWER CONVERSION

Demonstration Board EPC9107

Quick Start Guide

28 V Buck Converter featuring EPC2015

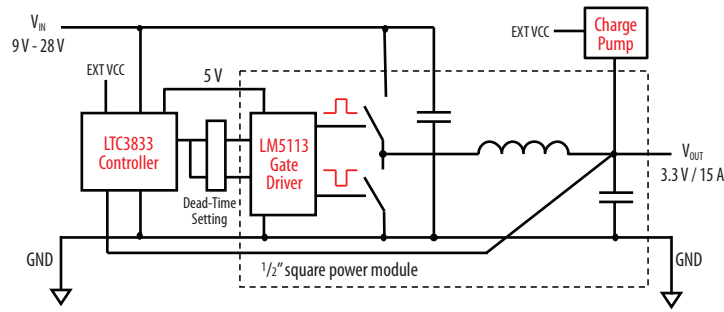


Figure 1: Block Diagram of EPC9107 Demonstration Board

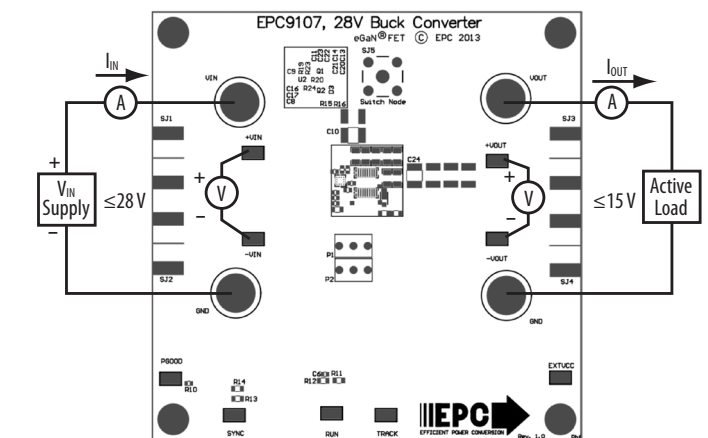


Figure 2: Proper Connection and Measurement Setup

EPC

EFFICIENT POWER CONVERSION

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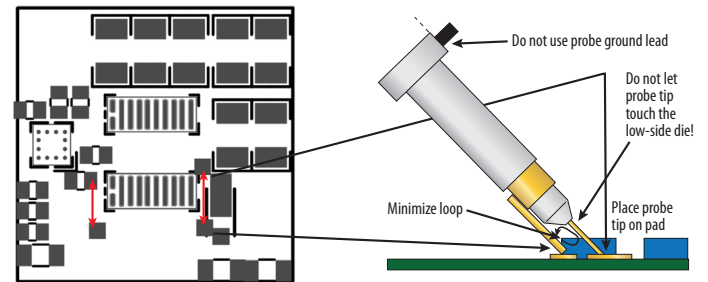


Figure 3: Proper Measurement of Switch Node or Gate Voltage

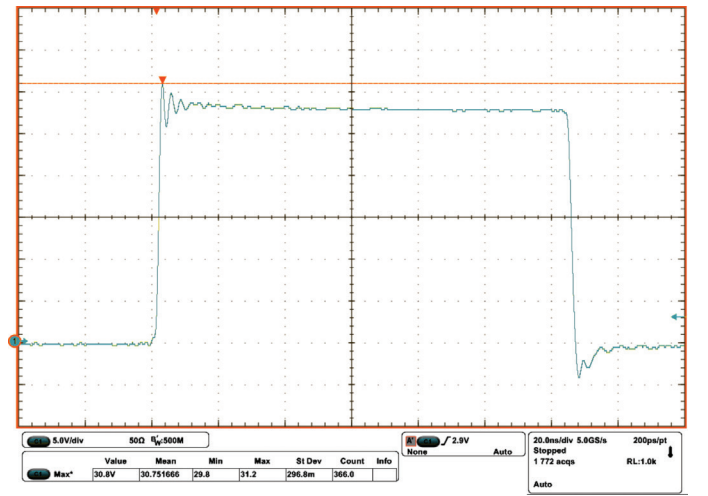


Figure 4: Typical waveforms for 28V to 3.3V / 15A (1 MHz) CH1: Switch node voltage

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