Highly Versatile Buck-Boost Ambient Energy Manager Battery Charger with Source Voltage Level Configuration

Feature

Ultra-low power start-up

- Cold start from 275 mV input voltage and 3 µW input power (typical).

Constant input voltage regulation

- Optimized for intermittent and pulse power.
- Selectable operating input voltage from 140 mV to 4.5 V.

Adaptive and smart energy management

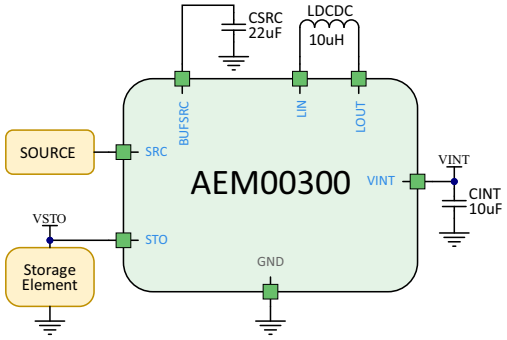
- DCDC switches automatically between boost, buck-boost and buck operation, according to input and output voltages, to maximize energy transfer.

Battery protection features

- Selectable over-charge and over-discharge protection for any type of rechargeable battery or (super-)capacitor.
- Fast super-capacitor charging.
- Dual cell super-capacitor balancing circuit.

Smallest footprint, smallest BOM

- Only three external components are required.
- One 10 µH inductor.
- Two capacitors: one 10 µF and one 22 µF.



Description

The AEM00300 is an integrated energy management circuit that extracts DC power from an ambient energy harvesting source to store energy in a storage element. The AEM00300 allows to extend battery lifetime and ultimately eliminates the primary energy storage element in a large range of applications.

Thanks to its selectable operating input voltage, it is possible to set a voltage at which the AEM00300 operates. This voltage is between 140 mV and 4.5 V.

With its unique cold start circuit, the AEM00300 can start harvesting with an input voltage as low as 275 mV and from an input power of 3 µW. The preset protection levels determine the storage element voltages protection thresholds to avoid over-charging and over-discharging the storage element and thus avoiding damaging it. Those are set through configuration pins. Moreover, custom threshold voltages can be obtained at the expense of a few configuration resistors.

The chip integrates all active elements for powering a typical wireless sensor. Only two capacitors and one inductor are required.

Applications

Door access systems	Smart wearable sensors
Smart switches home/building	Point-of-sales (POS)

Device Information

Part Number	Package	Body size [mm]
10AEM00300C0000	QFN 28-pin	4x4mm

Evaluation Board

Part Number
2AAEM00300C001

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1. Introduction

Figure 1: Simplified Schematic View

The AEM00300 is a full-featured energy efficient power management circuit able to harvest energy from an energy source (connected to SRC) to charge a storage element (connected to STO). This is done with a minimal bill of material: only 2 capacitors and one inductor are needed for a basic setup.

The heart of the AEM00300 is a regulated switching DCDC converter with high power conversion efficiency.

At first start-up, as soon as a required cold-start voltage of 275 mV and a sparse amount of power of at least 3 µW is available at the source, the AEM00300 coldstarts. After the cold start, the AEM extracts the power available from the source if the working input voltage is higher than $V_{SRC,REG}$.

Through four configuration pins (STO_CFG[3:0]), the user can select a specific operating mode out of 15 modes that cover most application requirements without any dedicated external component. Those operating modes define the protection levels of the storage element. If none of those 15 modes fit the user's storage element, a custom mode is also available to allow the user to define a mode with custom specifications.

Status pin ST_STO provides information about the voltage levels of the storage element. ST_STO is HIGH when the voltage of the storage element V_{STO} is above V_{CHRDY} and is reset when the voltage drops below V_{OVDIS}.

Depending on the harvester and the application, the source regulation voltage, $V_{SRC,REG}$, can be configured thanks to six configuration pins (SRC_LVL_CFG[5:0]).

The AEM00300's DCDC converter can work in two modes: LOW POWER MODE and HIGH POWER MODE, each one of these being optimized for a power range on SRC.

The charging of the storage element can be prevented by pulling EN_STO_CH to GND, typically to protect the storage element if the temperature is too low/high to safely charge it.

2. Pin Configuration and Functions

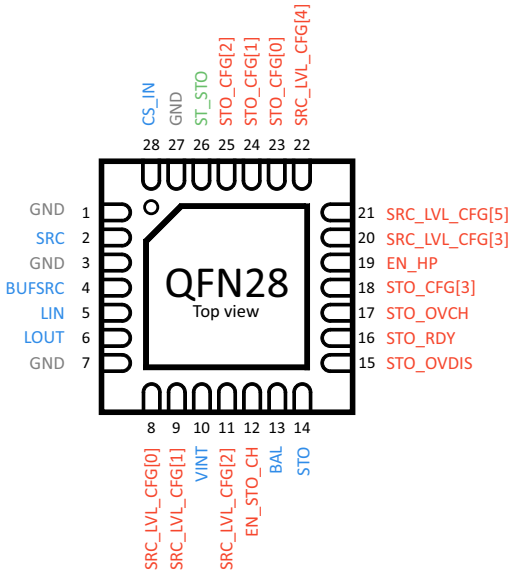

Figure 2: Pinout Diagram QFN 28-pin

NAME	PIN NUMBER	FUNCTION		
Power Pins				
CS_IN	28	Input for the eternal cold start circuit.		
SRC	2	Connection to the harvested energy source.		
BUFSRC	4	Connection to an external capacitor buffering the DCDC converter input.		
LIN	5	DCDC inductance connection.		
LOUT	6	DCDC inductance connection.		
VINT	10	Internal voltage supply.		
BAL	13	Connection to mid-point of a dual-cell supercapacitor (optional). Must be connected to GND if not used.		
STO	14	Connection to the energy storage element - battery or (super-)capacitor. Cannot be left floating. Must be connected to a minimum capacitance of 100 µF or to a rechargeable battery.		
Status Pins				
ST_STO	26	Logic Output	HIGH: V_{STO}	HIGH when the storage device voltage V_{STO} rises above V_{CHRDY} threshold. LOW when V_{STO} drops below the V_{OVDIS} threshold.

Table 1: Power and Status Pins

NAME	PIN NUMBER	HIGH LEVEL	FLOATING STATE	FUNCTION
Configuration Pins				
SRC_LVL_CFG[0]	8	V_{VINT}	HIGH	Used for the configuration of the source voltage level. Read as HIGH when left floating.
SRC_LVL_CFG[1]	9			
SRC_LVL_CFG[2]	11			
SRC_LVL_CFG[3]	20			
SRC_LVL_CFG[4]	22			
SRC_LVL_CFG[5]	21			
STO_CFG[0]	23	V_{VINT}	HIGH	Used for the configuration of the threshold voltages for the energy storage element V_{OVDIS}, V_{CHRDY} and V_{OVCH}. Read as HIGH when left floating.
STO_CFG[1]	24			
STO_CFG[2]	25			
STO_CFG[3]	18			
STO_OVCH	17	Used for the configuration of the threshold voltages (V_{OVDIS}, V_{CHRDY} and V_{OVCH}) for the energy storage element when STO_CFG[3:0] are set to custom mode (optional). Must be left floating if not used.		
STO_RDY	16			
STO_OVDIS	15			
EN_STO_CH	12	V_{LOAD}	HIGH	- Pulled up to LOAD or floating: enables the charging of the battery - Pulled down to GND: disables the charging of the battery
EN_HP	19	V_{VINT}	HIGH	- Pulled up to VINTor floating: HIGH POWER MODE enabled - Pulled down to GND: HIGH POWER MODE disabled
Other				
GND	1, 3, 7, 27 Exposed pad	Ground connection, best possible connection to PCB ground plane.		

Table 2: Configuration and Ground Pins

3. Absolute Maximum Ratings

Parameter	Value
Voltage on STO, SRC, BUFSRC, LIN, LOUT, BAL, CS_IN	-0.3 V to 5.5 V
Voltage on VINT, SRC_LVL_CFG[5:0], STO_CFG[3:0], STO_OVCH, STO_OVDIS, STO_RDY, EN_HP, EN_STO_CH	-0.3 V to 2.75 V
Operating junction temperature	-40 °C to 125 °C
Storage temperature	-65 °C to 150 °C
ESD HBM voltage	> 2000 V
ESD CDM voltage	> 500 V

Table 3: Absolute Maximum Ratings

4. Thermal Resistance

Package	θJA	θJC	Unit
QFN 28-pin	TBD	TBD	°C/W

Table 4: Thermal Resistance

ESD CAUTION	
	ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper EESD precautions should be taken to avoid performance degradation or loss of functionality

5. Typical Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Conversion						
$P_{SRC,CS}$	Source power required for cold start	V_{STO} > Vchrdy		3		µW
		V_{STO} < Vchrdy		6		µW
V_{SRC}	Input voltage of the energy source	During cold start		0.275	4.5	V
		After cold start	0.14		4.5	V
$V_{SRC,REG}V_{SRC,REG}$	Regulation voltage of the source	See Table 9	Depends on SRC_LVL_CFG[5:0] configuration			V
Storage element						
V_{OVCH}	Maximum voltage accepted on the storage element before disabling its charging	see Table 8	Depends on STO_CFG[3:0] configuration			V
V_{CHRDY}	Minimum voltage required on the storage element before asserting the ST_STO					V
V_{OVDIS}	Minimum voltage accepted on the storage element before reseting ST_STO					V
Internal supply & Quiescent Current						
V_{VINT}	Internal voltage supply			2.2		V
I_Q	Quiescent current on STO	V_{STO} = 3.7V V_{LOAD} = 2.5V EN_SLEEP = L EN_HP = L		5.9		nA
Symbol	Logic Level		LOW		HIGH	
Logic output pins						
ST_STO	Logic output levels on the status STO pin		GND		V_{STO}	

Table 5: Typical Electrical Characteristics

6. Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
External Components					
L_{DCDC}	Inductor of the DCDC converter		10		µH
C_{SRC}	Capacitor decoupling the SRC terminal	13[1]	22		µF
C_{INT}	Capacitor decoupling the VINT terminal	5[1]	10		µF
C_{STO}	Optional - Capacitor on STO if no storage element is connected (see Section 9.6.1)	100[1]			µF
STO_OVCH	Configuration of V_{OVCH} in custom mode	1	Section 9.3	100	MΩ
STO_OVDIS	Configuration of V_{OVDIS} in custom mode				
STO_RDY	Configuration of V_{CHRDY} in custom mode				
Symbol	Logic Level	LOW		HIGH	
Logic input pins					
SRC_LVL_CFG[5:0]	Configuration pins for the SRC voltage level	GND		VINT	
STO_CFG[3:0]	Configuration pins for the STO voltage	GND		VINT	
EN_STO_FT	Configuration pin for the controller	GND		VINT	
EN_STO_CH	Configuration pin for the controller	GND		VINT	
EN_HP	Configuration pin for the controller	GND		VINT	

Table 6: Recommended Operation Conditions

1.Consider all component tolerance and deratings. Typically, DC-bias derating has a major impact on capacitance on ceramic capacitors.

7. Functional Block Diagram

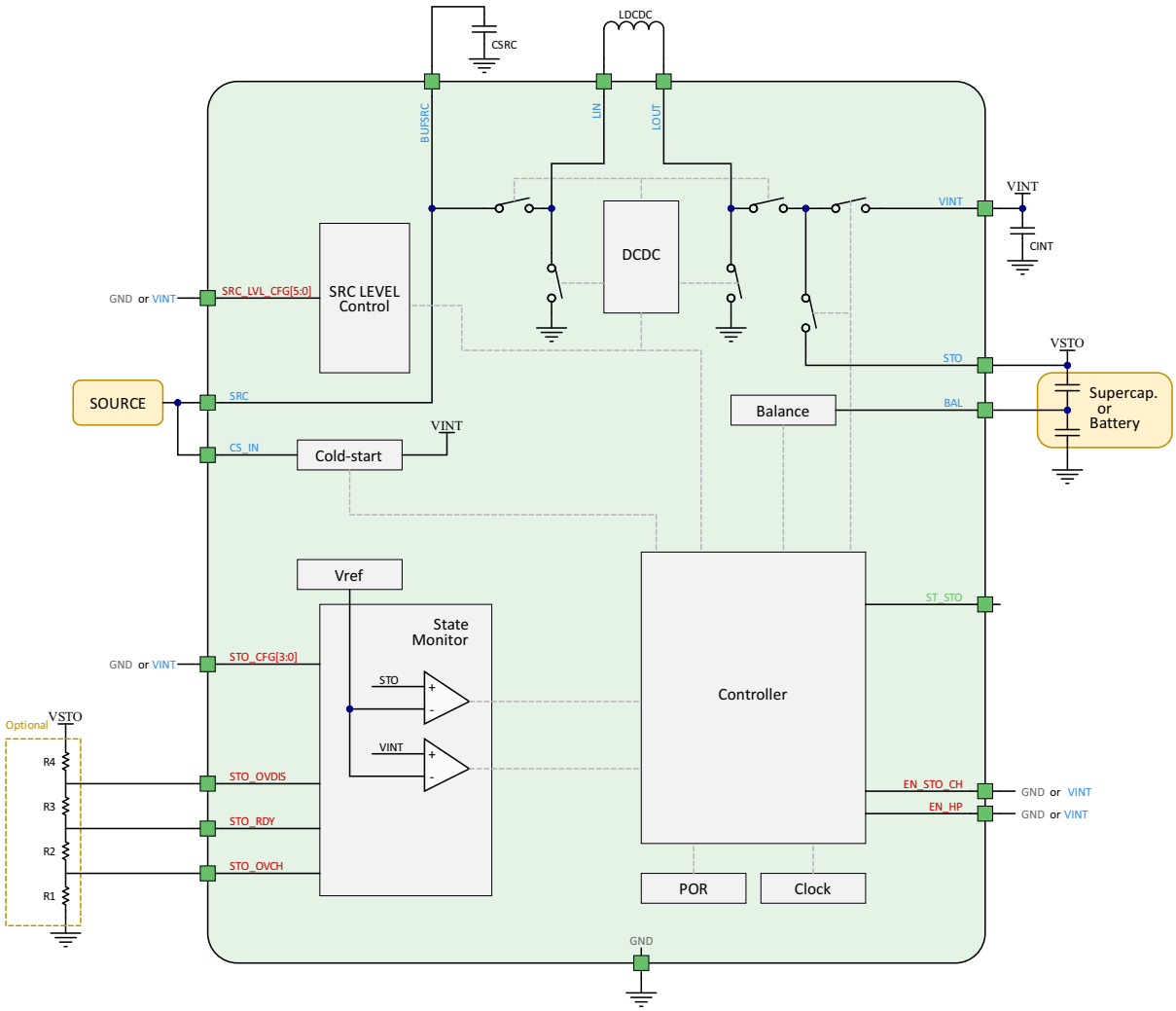

Figure 3: Functional Block Diagram

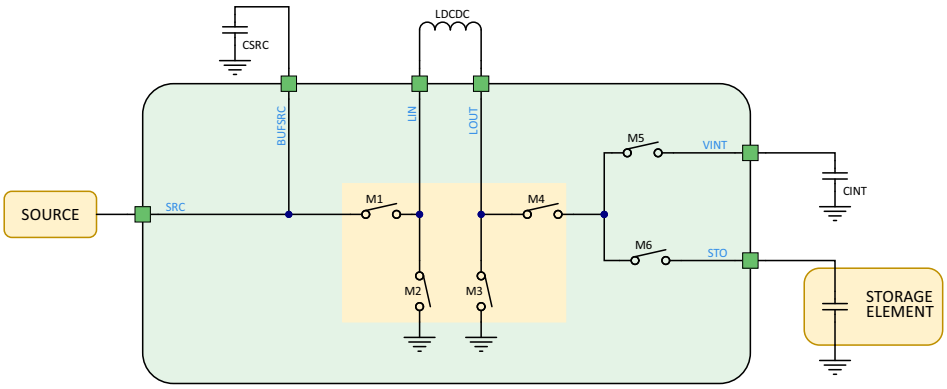

Figure 4: Simplified Schematic View of the AEM00300

8. Theory of Operation

8.1. DCDC Converter

The DCDC converter converts the voltage available at BUFSRC to a level suitable for charging the storage element STO or to regulate the internal supply VINT. The switching transistors of the DCDC converter are M1, M2, M3 and M4. Thanks to M5 and M6, the controller selects between VINT and STO respectively as the converter output. STO is selected as an output only when VINT does not need to be supplied.

The reactive power component of this converter is the external inductor L_{DCDC}. V_{SRC} is regulated to $V_{SRC,REG}$ configured by SRC_LVL_CFG[5:0]. BUFSRC is decoupled by the capacitor C_{SRC}, which smooths the voltage against the current pulses pulled by the DCDC converter. The storage element is connected to the STO pin.

Depending on its input voltage and its output voltage, the DCDC converter will work as a boost converter, a buck converter or a buck-boost converter. The maximum power that can be harvested and supplied to the output depends on the power mode (HIGH POWER MODE or LOW POWER MODE), which is configured through the EN_HP pin (see Section 9.1).

DCDC Converter Mode	Input Voltage / Output Voltage
Boost	$V_{IN} < V_{OUT}$ - 250 mV
Buck	$V_{IN} > V_{OUT}$ + 250 mV
Buck - Boost	V_{OUT} - 250 mV < V_{IN} < V_{OUT} + 250 mV

Table 7: DCDC Converter Modes

8.2. Cold-Start Circuit

The AEM00300 is able to coldstart if the voltage on CS_IN is above 0.275 V. The minimum available power is:

- 3 µW if V_{STO} is above V_{CHRDY}.
- 6 µW if V_{STO} is below V_{CHRDY}.

CS_IN is typically connected to SRC to allow the AEM00300 to coldstart from the energy available on the harvester. Nevertheless, any other energy source can be connected to CS_IN as long as it meets the electrical specifications constraints described in Sections 5 and 6.

8.3. AEM00300 States Description

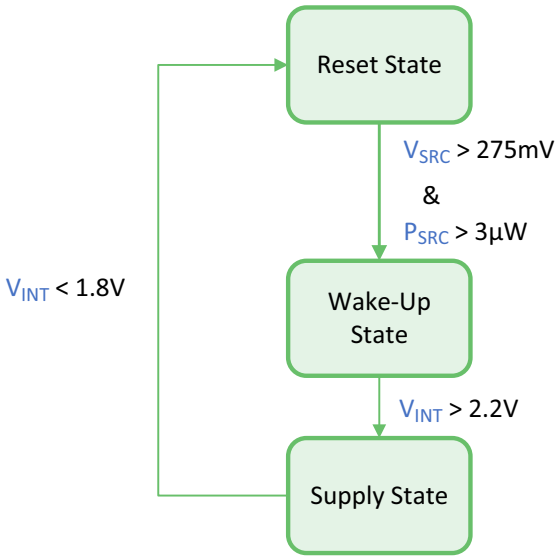

Figure 5: Diagram of the AEM00300 States

8.3.1. Reset and Wake Up States

The RESET STATE is a state where all nodes are deeply discharged and there is no available energy to be harvested. As soon as the required cold start voltage of 275 mV and a sparse amount of power of just 3 µW become available on CS_IN (usually connected to SRC), the AEM00300 switches to WAKE-UP STATE, and energy is extracted from SRC to make V_{VINT} rise to 2.2 V. When V_{VINT} reaches those 2.2 V, the AEM00300 switches to SUPPLY STATE.

8.3.2. Supply State

In SUPPLY STATE, three scenarios are possible:

- There is enough power provided by the source (SRC) to keep V_{VINT} at 2.2 V. The excessive power is used to charge the storage element on STO. In that case, the circuit remains in SUPPLY STATE. If STO is fully charged, the DCDC converter is disabled to prevent over-charging the storage element, and the SRC pin is set to high impedance.
- Due to a lack of power from the source, V_{STO} falls below V_{OVDIS}. In this case, the circuit enters RESET STATE as explained in Section 8.3.1.
- There is no power on SRC. It is therefore not possible to maintain VINT to 2.2 V. In this case, the circuit enters in RESET STATE.

The AEM00300 internal circuit current consumption causes C_{INT} to discharge. When the voltage on VINT falls below its 2.2 V regulation set point, the DCDC converter switches its output to recharge C_{INT} from SRC, thus keeping VINT regulated. If no sufficient power is available on SRC to keep VINT regulated, the AEM00300 switches to RESET STATE.

8.4. Source Voltage Regulation

During SUPPLY STATE, the voltage on SRC is regulated to a voltage configured by the user. The AEM00300 offers a choice of fifty-nine values for the source voltage. If the open-circuit voltage of the harvester is lower than $V_{SRC,REG}$, the AEM00300 does not extract the power from the source. If the SRC voltage is higher, the AEM00300 regulates V_{SRC} to $V_{SRC,REG}$ and extracts power.

8.5. Balancing for Dual-Cell Supercapacitor

The balancing circuit allows the user to balance the internal voltage of the dual-cell supercapacitor connected to STO in order to avoid damaging the supercapacitor because of excessive voltage on one cell.

If BAL is connected to GND, the balancing circuit is disabled. This configuration must be used if a battery, a capacitor or a single-cell supercapacitor is connected on STO.

If BAL is connected to the node between both cells of a supercapacitor, the balancing circuit compensates for any mismatch of the two cells that could lead to the over-charge of one of two cells. The balancing circuit ensures that BAL remains close to V_{STO} / 2. This configuration must be used if a dual-cell supercapacitor is connected to STO, and that this supercapacitor requires cells balancing.

The balancing circuit works as follows, with V_{BAL} the voltage on the BAL pin:

- $V_{BAL} > \frac{V_{STO}}{2}$: the AEM00300 enables a switch between BAL and GND to discharge the bottom supercapacitor cell to GND (up to 20 mA).
- $V_{BAL} < \frac{V_{STO}}{2}$: the AEM00300 enables a switch between STO and BAL to discharge the top supercapacitor cell to the bottom supercapacitor cell (up to 20 mA).

NOTE: the balancing feature is optimized for supercapacitors, for use with other storage elements (batteries, etc.), please contact e-peas support.

9. System Configuration

9.1. High Power / Low Power Mode

When EN_HP is pulled to VINT, the DCDC converter is configured to HIGH POWER MODE. This allows higher currents to be extracted from the DCDC converter input (SRC) to the DCDC converter output (STO).

9.2. Storage Element Configuration

Through four configuration pins (STO_CFG[3:0]), the user can set a particular operating mode from a range that covers most application requirements, without any dedicated external component as shown in Table 8. The three threshold levels are defined as:

- V_{OVCH}: maximum voltage accepted on the storage element before disabling its charging.
- V_{CHRDY}: minimum voltage required on the storage element before ST_STO is HIGH.
- V_{OVDIS}: minimum voltage accepted on the storage element before setting ST_STO LOW.

Configuration pins				Storage element threshold voltages			Typical use
STO_CFG[3:0]				V_{OVDIS}	V_{CHRDY}	V_{OVCH}	
L	L	L	L	3.00 V	3.50 V	4.05 V	$LiCoO_2$ battery, Li-Po battery, Lithium Titanate (3.8 V) battery (long life).
L	L	L	H	2.80 V	3.10 V	3.60 V	$LiFePO_4$ battery, Lithium capacitor (LiC).
L	L	H	L	1.85 V	2.40 V	2.70 V	Dual-cell NiMH battery, Lithium-Titanate (2.4V) battery.
L	L	H	H	0.20 V	1.00 V	4.65 V	Dual-cell supercapacitor.
L	H	L	L	0.20 V	1.00 V	2.60 V	Single-cell supercapacitor.
L	H	L	H	1.00 V	1.20 V	2.95 V	Single-cell supercapacitor.
L	H	H	L	1.85 V	2.30 V	2.60 V	Lithium-Titanate battery (2.4V).
L	H	H	H	Custom Mode (single-cell NiMH battery, LiC, etc.)[1].			
H	L	L	L	1.10 V	1.25 V	1.50 V	Ni-Cd single-cell battery.
H	L	L	H	2.20 V	2.50 V	3.00 V	Ni-Cd dual-cell battery.
H	L	H	L	1.45 V	2.00 V	4.65 V	Dual-cell supercapacitor.
H	L	H	H	1.00 V	1.20 V	2.60 V	Single-cell supercapacitor.
H	H	L	L	2.00 V	2.30 V	2.60 V	Solid State battery.
H	H	L	H	3.00 V	3.50 V	4.35 V	$LiCoO_2$ battery, Li-Po battery, Lithium Titanate (3.8 V) battery.
H	H	H	L	2.60 V	2.70 V	4.00 V	Tadiran TLI.
H	H	H	H	2.60 V	3.50 V	3.90 V	Tadiran HLC.

Table 8: Storage Element Configuration Pins

1. An example of a single-cell NiMH batteries optimized custom mode setting can be found at Section 10.2.

9.3. Custom Mode Configuration

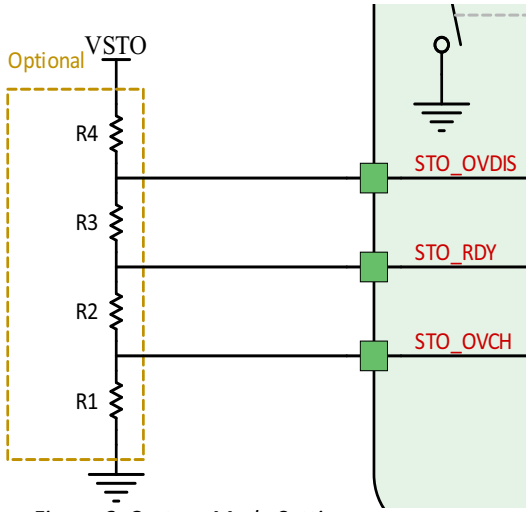

Figure 6: Custom Mode Settings

When STO_CFG[3:0] = LHHH, the custom mode is selected and all four configuration resistors must be wired as shown in Figure 6.

V_{OVCH}, V_{CHRDY} and, V_{OVDIS} are defined thanks to R1, R2, R3 and R4, which can be determined within the following constraints:

- $R_T = R_1 + R_2 + R_3 + R_4$
- $1M\Omega \leq R_T \leq 100M\Omega$
- $R_1 = R_T \cdot \frac{1V}{V_{OVCH}}$
- $R_2 = R_T \cdot \left(\frac{1V}{V_{CHRDY}} - \frac{1V}{V_{OVCH}}\right)$
- $R_3 = R_T \cdot \left(\frac{1V}{V_{OVDIS}} - \frac{1V}{V_{CHRDY}}\right)$
- $R_4 = R_T \cdot \left(1 - \frac{1V}{V_{OVDIS}}\right)$

The resistors should have high values to make the additional power consumption negligible. Moreover, the following constraints must be respected to ensure the functionality of the chip:

- $V_{CHRDY} + 0.05V \leq V_{OVCH} \leq 4.5V$
- $V_{OVDIS} + 0.05V \leq V_{CHRDY} \leq V_{OVCH} - 0.05V$
- $1V \leq V_{OVDIS}$

9.4. Disable Storage Element Charging

Pulling down EN_STO_CH pin to GND disables the charging of the storage element connected to STO. This can be done for example to protect the storage element when the system detects that the environment temperature is too low or too high to safely charge the storage element.

While EN_STO_CH is pulled down, VINT can still be supplied from SRC.

To enable charging the storage element on STO, EN_STO_CH must be pulled up to VINT or left floating (pin is pulled up internally).

9.5. Source Level Configuration

Six dedicated configuration pins, SRC_LVL_CFG[5:0], allow selecting the $V_{SRC,REG}$ at which the source regulates its voltage.

Configuration pins						Voltage Level
SRC_LVL_CFG[5:0]						$V_{SRC,REG}$
L	L	L	L	L	L	0.14 V
L	L	L	L	L	H	0.17 V
L	L	L	L	H	L	0.20 V
L	L	L	L	H	H	0.23 V
L	L	L	H	L	L	0.26 V
L	L	L	H	L	H	0.30 V
L	L	L	H	H	L	0.34 V
L	L	L	H	H	H	0.39 V
L	L	H	L	L	L	0.43 V
L	L	H	L	L	H	0.48 V
L	L	H	L	H	L	0.52 V
L	L	H	L	H	H	0.57 V
L	L	H	H	L	L	0.61 V
L	L	H	H	L	H	0.66 V
L	L	H	H	H	L	0.70 V
L	L	H	H	H	H	0.75 V
L	H	L	L	L	L	0.80 V
L	H	L	L	L	H	0.84 V
L	H	L	L	H	L	0.89 V
L	H	L	L	H	H	0.95 V
L	H	L	H	L	L	1.05 V
L	H	L	H	L	H	1.14 V
L	H	L	H	H	L	1.23 V
L	H	L	H	H	H	1.32 V
L	H	H	L	L	L	1.41 V
L	H	H	L	L	H	1.50 V
L	H	H	L	H	L	1.59 V
L	H	H	L	H	H	1.68 V
L	H	H	H	L	L	1.77 V
L	H	H	H	L	H	1.86 V

Configuration pins						Voltage Level
SRC_LVL_CFG[5:0]						$V_{SRC,REG}$
L	H	H	H	H	L	1.95 V
L	H	H	H	H	H	2.05 V
H	L	L	L	L	L	2.14 V
H	L	L	L	L	H	2.23 V
H	L	L	L	H	L	2.32 V
H	L	L	L	H	H	2.41 V
H	L	L	H	L	L	2.50 V
H	L	L	H	L	H	2.59 V
H	L	L	H	H	L	2.68 V
H	L	L	H	H	H	2.77 V
H	L	H	L	L	L	2.86 V
H	L	H	L	L	H	2.95 V
H	L	H	L	H	L	3.05 V
H	L	H	L	H	H	3.14 V
H	L	H	H	L	L	3.23 V
H	L	H	H	L	H	3.32 V
H	L	H	H	H	L	3.41 V
H	L	H	H	H	H	3.50 V
H	H	L	L	L	L	3.59 V
H	H	L	L	L	H	3.68 V
H	H	L	L	H	L	3.77 V
H	H	L	L	H	H	3.86 V
H	H	L	H	L	L	3.95 V
H	H	L	H	L	H	4.05 V
H	H	L	H	H	L	4.14 V
H	H	L	H	H	H	4.23 V
H	H	H	L	L	L	4.32 V
H	H	H	L	L	H	4.41 V
H	H	H	L	H	L	4.50 V

Table 9: Source regulation configuration pins

9.6. External Components

Refer to Figure 14 to have an illustration of the external components wiring.

9.6.1. Storage Element Information

The energy storage element of the AEM00300 can be a rechargeable battery, a supercapacitor or a capacitor. The size of the storage element must be determined so that its voltage does not fall below V_{OVDIS} even during current peaks pulled by the application. If the internal resistance of the storage element cannot sustain this voltage limit, it is advisable to decouple the battery with a capacitor.

If the application expects a disconnection of the battery (e.g. because of a user removable connector), the PCB should include a capacitor C_{STO} of at least 100 µF connected between STO and GND. The leakage current of the storage element should be small as leakage currents directly impact the quiescent current of the whole subsystem.

9.6.2. External Inductor Information

The AEM00300 operates with one standard miniature inductor. L_{DCDC} must sustain a peak current of at least 1 A and a switching frequency of at least 10 MHz. Low equivalent series resistance (ESR) favors the power conversion efficiency of the DCDC converter. The recommended value is 10 µH.

9.6.3. External Capacitors Information

9.6.3.1. C_{SRC}

This capacitor acts as an energy buffer at the input of the DCDC converter. It prevents large voltage fluctuations when the DCDC converter is switching. The recommended nominal value is 22 µF.

9.6.3.2. C_{INT}

This capacitor acts as an energy buffer for the internal voltage supply. The recommended nominal value is 10 µF.

10. Typical Application Circuits

10.1. Example Circuit 1

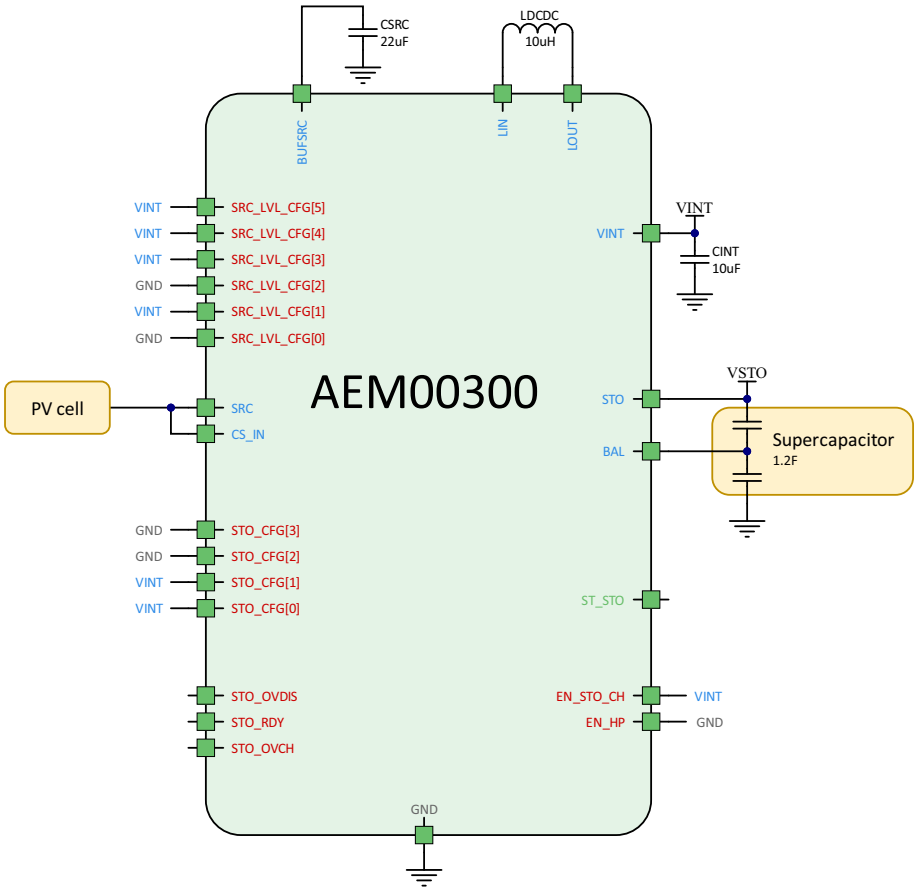

Figure 7: Typical Application Circuit 1

The circuit is an example of a system with solar energy harvesting. It uses a pre-defined operating mode that uses standard components, and a supercapacitor as energy storage.

- Energy source: PV cell.
- SRC_LVL_CFG[5:0] = LLHHHH: the AEM00300 starts to extract power from 0.75 V and regulates V_{SRC} to 0.75 V.
- STO_CFG[3:0] = LLHH: the storage element is a dual-cell supercapacitor, with:
  - V_{OVCH} = 4.65 V
  - V_{CHRDY} = 1.00 V
  - V_{OVDIS} = 0.20 V
- The balancing pin of the dual-cell supercapacitor is connected to BAL.
- EN_STO_CH is connected to VINT: the charging of the storage element on STO is enabled.
- EN_HP is connected to GND: the DCDC converter is in LOW POWER MODE.

10.2. Example Circuit 2

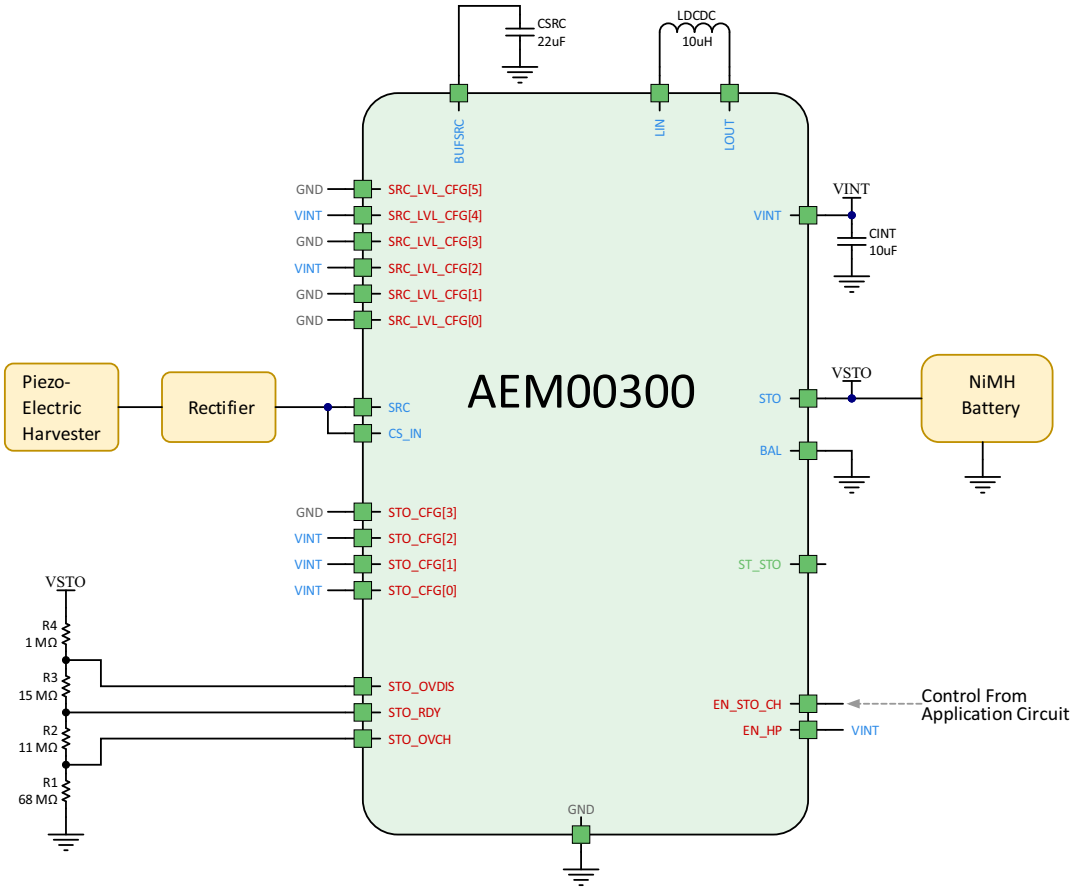

Figure 8: Typical Application Circuit 2

The circuit is an example of a system with vibration energy harvesting. It uses a rechargeable NiMH battery as storage element. The voltage thresholds are set by the custom mode.

- Energy source: piezoelectric vibration harvester.
- SRC_LVL_CFG[5:0] = LHLHLL: the AEM00300 starts to extract power from 1.05 V and regulates V_{SRC} to 1.05 V.
- STO_CFG[3:0] = LHHH: the storage element is a NiMH rechargeable battery, used with custom mode:
  - V_{OVDIS} = 1.00 V
  - V_{CHRDY} = 1.20 V
  - V_{OVCH} = 1.40 V
- Custom mode resistor divider calculations (values have been chosen to match E24 series value):
  - $R_T = 95M\Omega$
  - $R_1 = R_T \cdot \frac{1V}{V_{OVCH}} \approx 68M\Omega$
  - $R_2 = R_T \cdot \left(\frac{1V}{V_{CHRDY}} - \frac{1V}{V_{OVCH}}\right) \approx 11M\Omega$
  - $R_3 = R_T \cdot \left(\frac{1V}{V_{OVDIS}} - \frac{1V}{V_{CHRDY}}\right) \approx 15M\Omega$
  - $R_4 = R_T \cdot \left(1 - \frac{1V}{V_{OVDIS}}\right) \approx 1M\Omega$
- BAL is not used (not a dual-cell storage element) so it is connected to GND.
- EN_STO_CH: the charging of the storage element present on STO is controlled by the application circuit, typically by a micro-controller GPIO output.
- EN_HP is connected to VINT: the DCDC converter is in HIGH POWER MODE.

NOTE: for LiC (Lithium-ion Capacitor) storage elements, or others that would not be covered by STO_CFG[3:0] presets, please apply the same equations as in the above example to determine custom mode resistors values. E24 series values for typical storage elements can be found in the AEM00300 Configuration Tool spreadsheet, to be downloaded on e-peas website.

11. Circuit Behavior

11.1. Wake-up state and Supply state

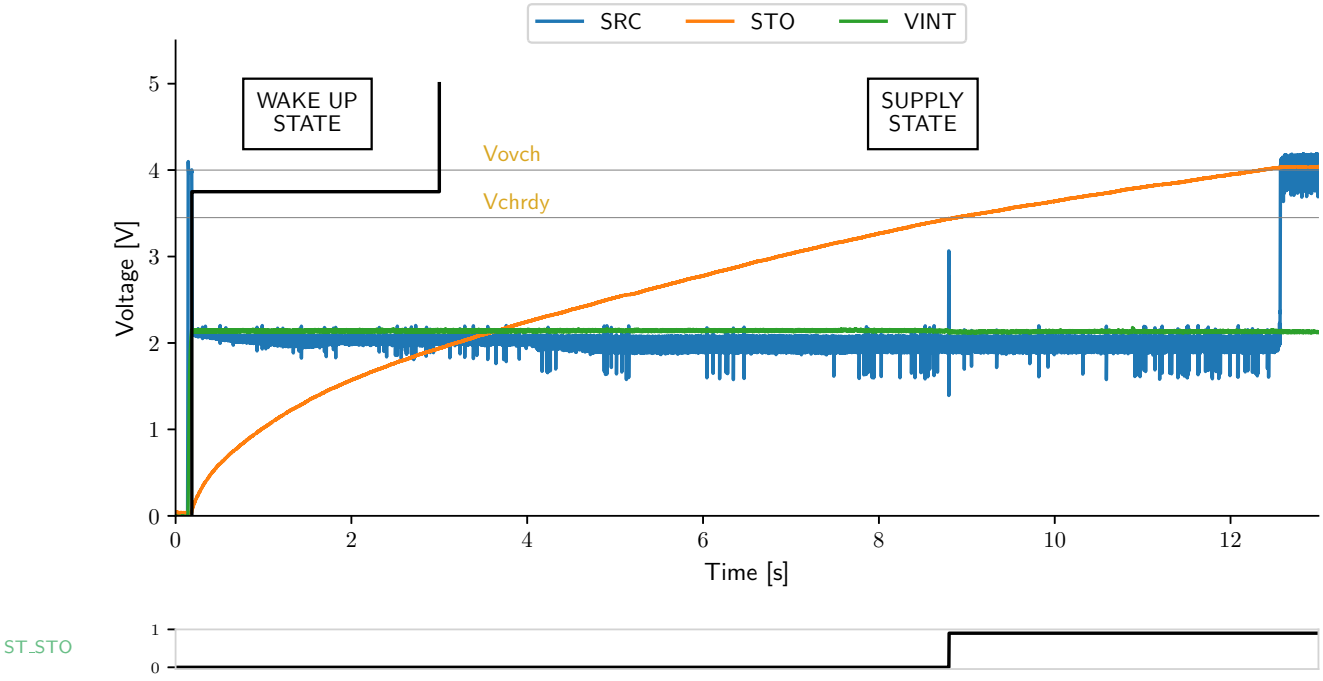

Figure 9: Wake-up state and Supply state

- STO_CFG[3:0] = LLLL
  - V_{OVDIS} = 3.00 V
  - V_{CHRDY} = 3.50 V
  - V_{OVCH} = 4.05 V
- SRC_LVL_CFG[5:0] = LHHHHH ($V_{SRC,REG}$ = 2.05 V)
- C_{STO} = 10 mF
- SRC: 5 mA current source with 4 V voltage compliance
- EN_HP = H (high power mode)
- EN_STO_CH = H (storage element charge enabled)

11.2. Supply state

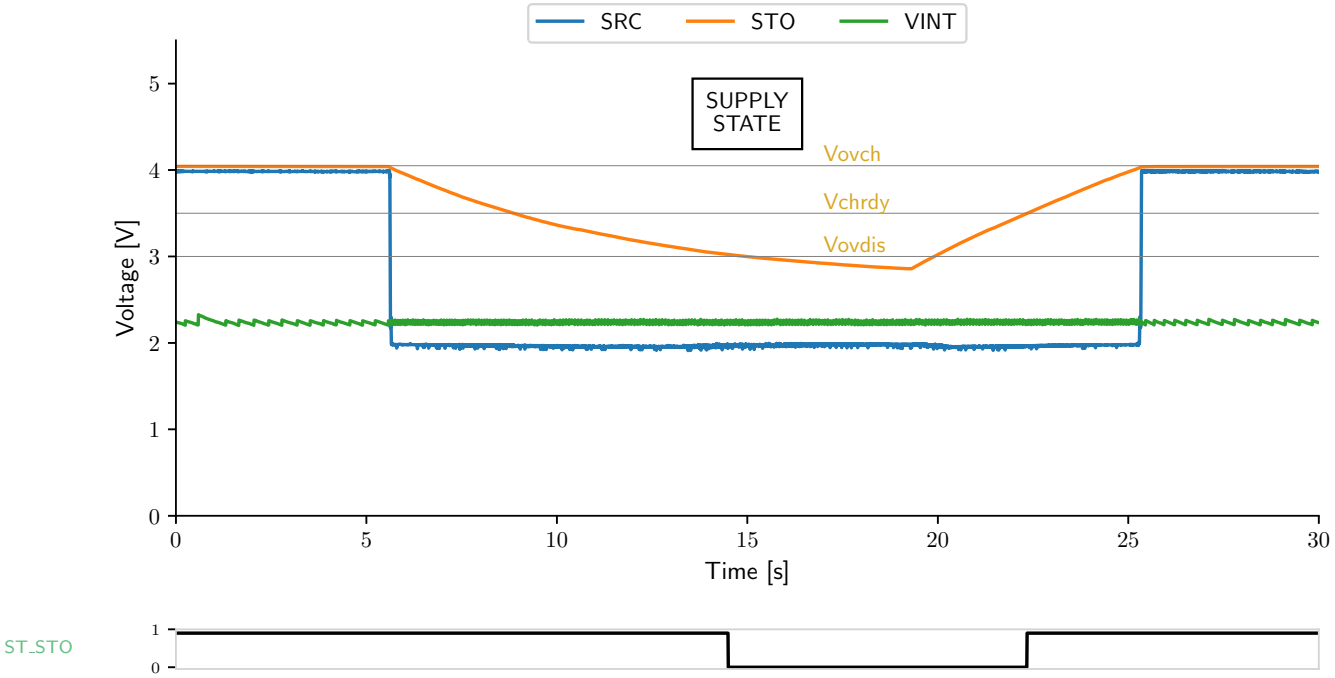

Figure 10: Supply state

- STO_CFG[3:0] = LLLL
  - V_{OVDIS} = 3.00 V
  - V_{CHRDY} = 3.50 V
  - V_{OVCH} = 4.05 V
- SRC_LVL_CFG[5:0] = LHHHHH ($V_{SRC,REG}$ = 2.05 V)
- C_{STO} = 10 mF
- SRC: 5 mA current source with 4 V voltage compliance
- EN_HP = H (high power mode)
- EN_STO_CH = H (storage element charge enabled)
- 1 kΩ between STO and GND, connected between 5.5 s and 19 s (no load on STO the rest of the time)

11.3. Supply state and Reset state

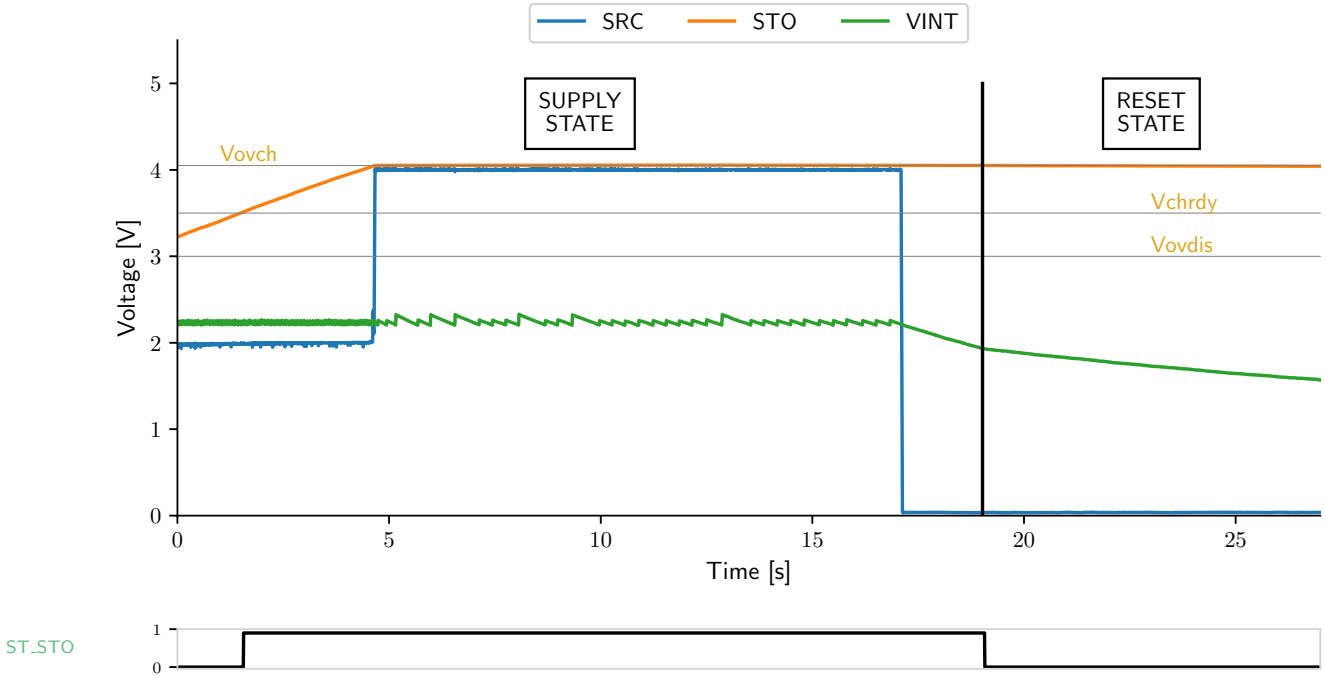

Figure 11: Supply state and Reset state

- STO_CFG[3:0] = LLLL
  - V_{OVDIS} = 3.00 V
  - V_{CHRDY} = 3.50 V
  - V_{OVCH} = 4.05 V
- SRC_LVL_CFG[5:0] = LHHHHH ($V_{SRC,REG}$ = 2.05 V)
- C_{STO} = 10 mF
- SRC: 5 mA current source with 4 V voltage compliance (stopped after 17 seconds)
- EN_HP = H (high power mode)
- EN_STO_CH = H (storage element charge enabled)

12. Performance Data

12.1. DCDC Conversion Efficiency From SRC to STO in Low Power Mode

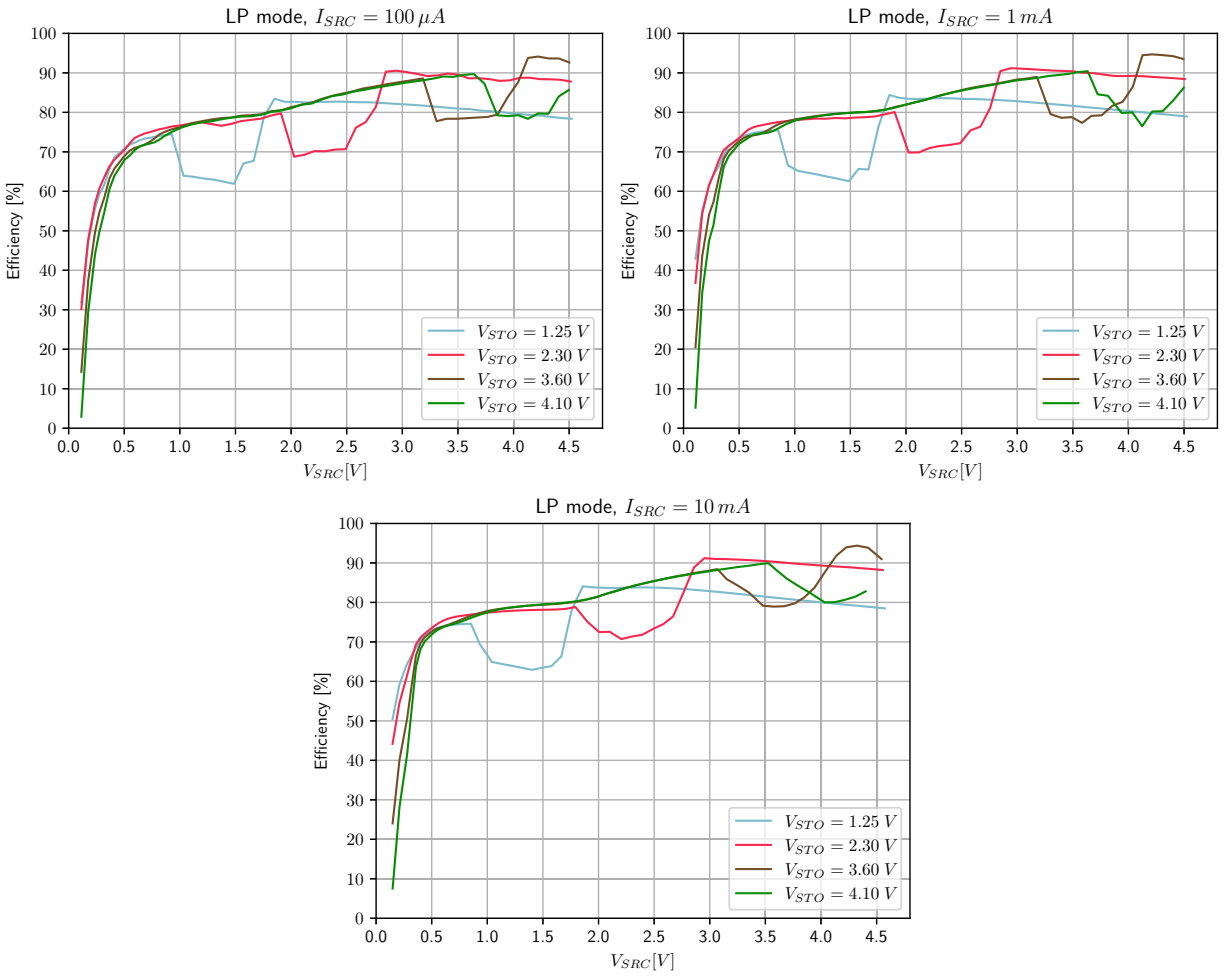

Figure 12: DCDC Efficiency from SRC to STO for 1 mA and 10 mA in Low Power Mode

12.2. DCDC Conversion Efficiency From SRC to STO in High Power Mode

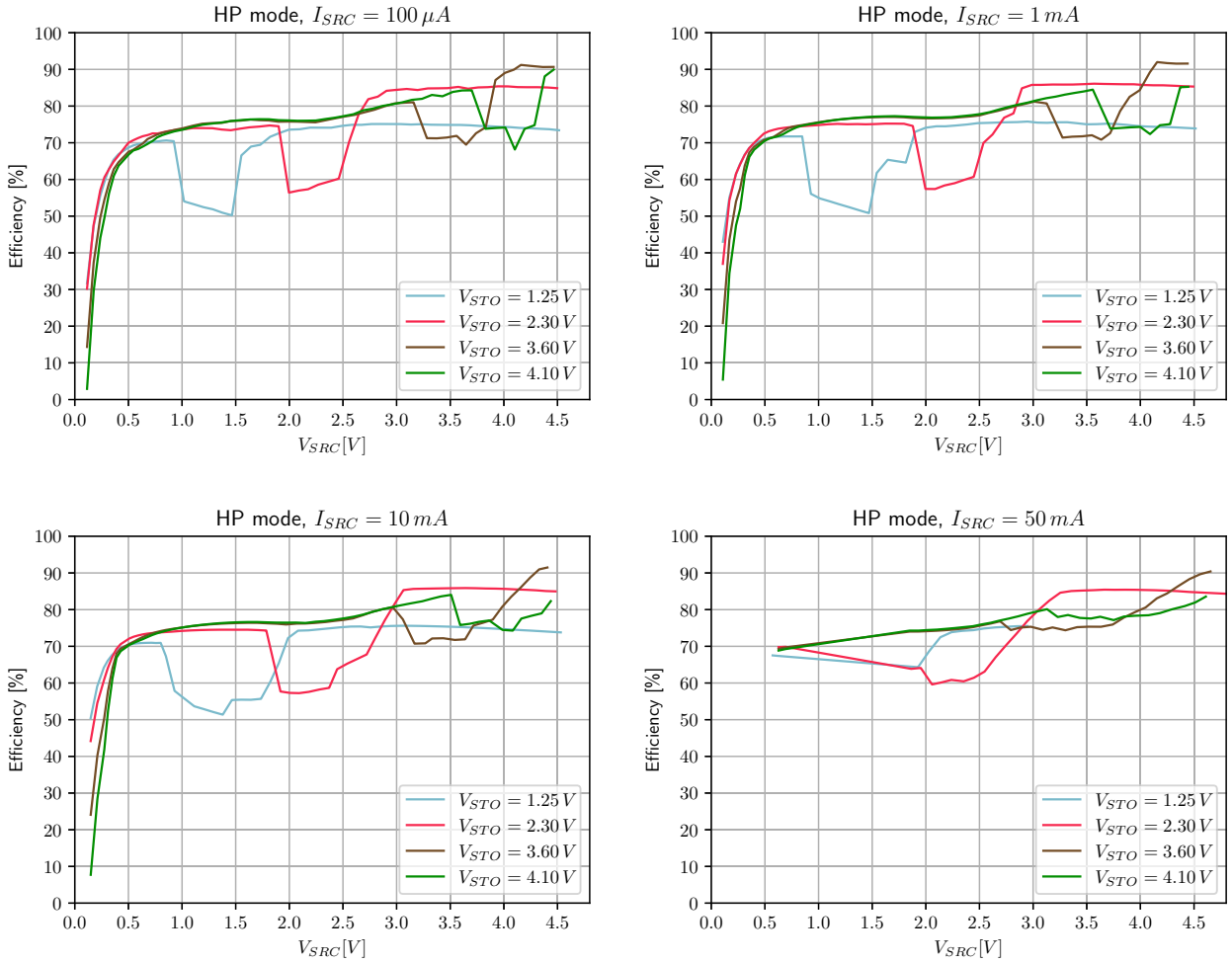

Figure 13: DCDC Efficiency from SRC to STO for 10 mA and 50 mA in High Power Mode

13. Schematic

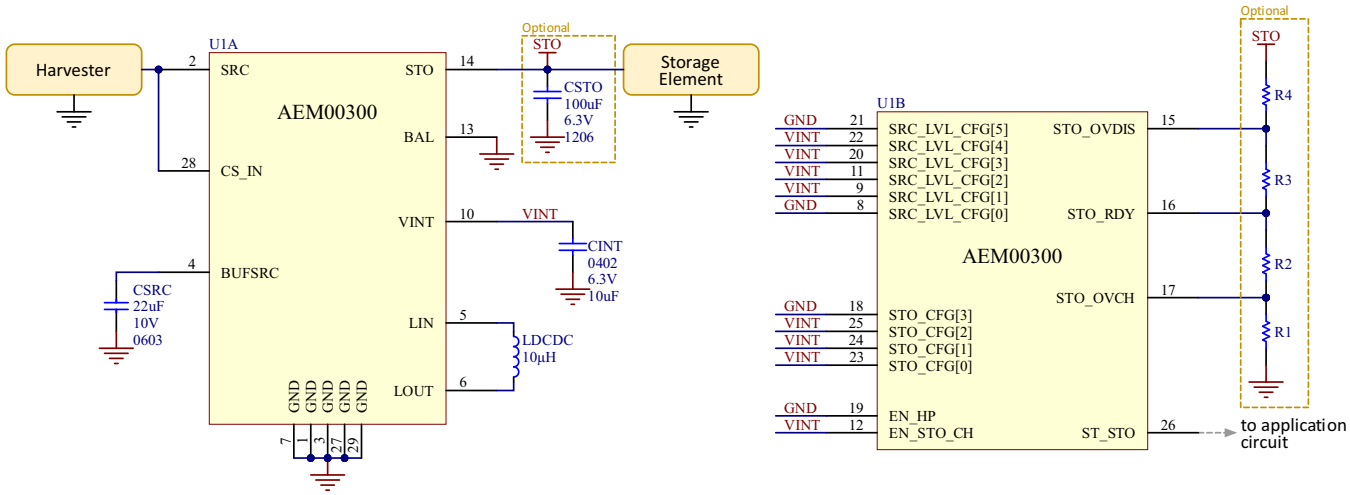

Figure 14: Schematic Example

Designator	Description	Quantity	Manufacturer	Link
U1	AEM00300 - Symbol QFN 28-pin	1	e-peas	order at sales@e-peas.com
L_{DCDC}	Power inductor 10 µH - 1.76A	1	Murata	DFE252010F-100M
C_{INT}	Ceramic Cap 10 µF, 6.3V, 20%, X5R 0402	1	Murata	GRM155R60J106ME15
C_{SRC}	Ceramic Cap 22 µF, 10V, 20%, X5R 0603	1	Murata	GRM188R61A226ME15D
C_{STO} (optional)	Ceramic Cap 100 µF, 6.3V, 20%, X5R 1206	1	TDK	C3216X5R1A107M160AC

Table 10: Minimal Bill of Materials

14. Layout

14.1. Guidelines

Good layout practices are mandatory in order to obtain good stability and best efficiency with the AEM00300. It also allows for minimizing electromagnetic interferences generated by the AEM00300 DCDC converter.

The following list, while not exhaustive, shows the main attention points when routing a PCB with the AEM00300:

- The switching nodes (LIN and LOUT) must be kept as short as possible, with minimal track resistance and minimal track capacitance. Low resistance is obtained by keeping track length as short as possible and track width as large as possible between L_{DCDC} and the AEM00300 pins. Minimal capacitance is obtained by keeping distance between LIN/LOUT and other signals. We recommend removing the ground plane, the power plane and the bottom layer ground pour under L_{DCDC} footprint, as well as adding distance between LIN/LOUT and the top ground pour, as shown on Figure 15.
- The DCDC decoupling capacitors (C_{SRC} - C_{STO}) must be placed as close as possible to the AEM00300, with direct connection and minimum track resistance for the corresponding power nodes (BUFSRC and STO).
- The GND return path between the DCDC decoupling capacitors (C_{SRC} - C_{STO}) and the AEM00300 thermal pad, which is the AEM00300 main GND connection, must be as direct and short as possible. This is preferably done on the top layer when possible, otherwise by internal/bottom plane, using low resistance vias to decrease layer-to-layer connection resistance.
- The external DC power connections (SRC and STO) must be connected to the AEM00300 with low resistance tracks.
- Connection between VINT and C_{INT} must be moderately short for AEM00300 stability, even though this pins does not carry large currents. Same for connection between C_{INT} to GND.
- The BAL pin connection track must be able to handle at least 40 mA.
- The custom mode setting pins STO_OVDIS, STO_RDY and STO_OVCH are high impedance analog inputs typically connected to a resistive divider with high resistor values, making those three nodes prone to pickup noise. Thus it is recommended to keep those as short as possible and as far as possible to noise sources such as DCDC switching nodes.
- The configuration pins and the status pins have minimal layout restrictions. CS_IN maximum current is below 1 mA, so its layout restrictions are minimal as well.

14.2. Example

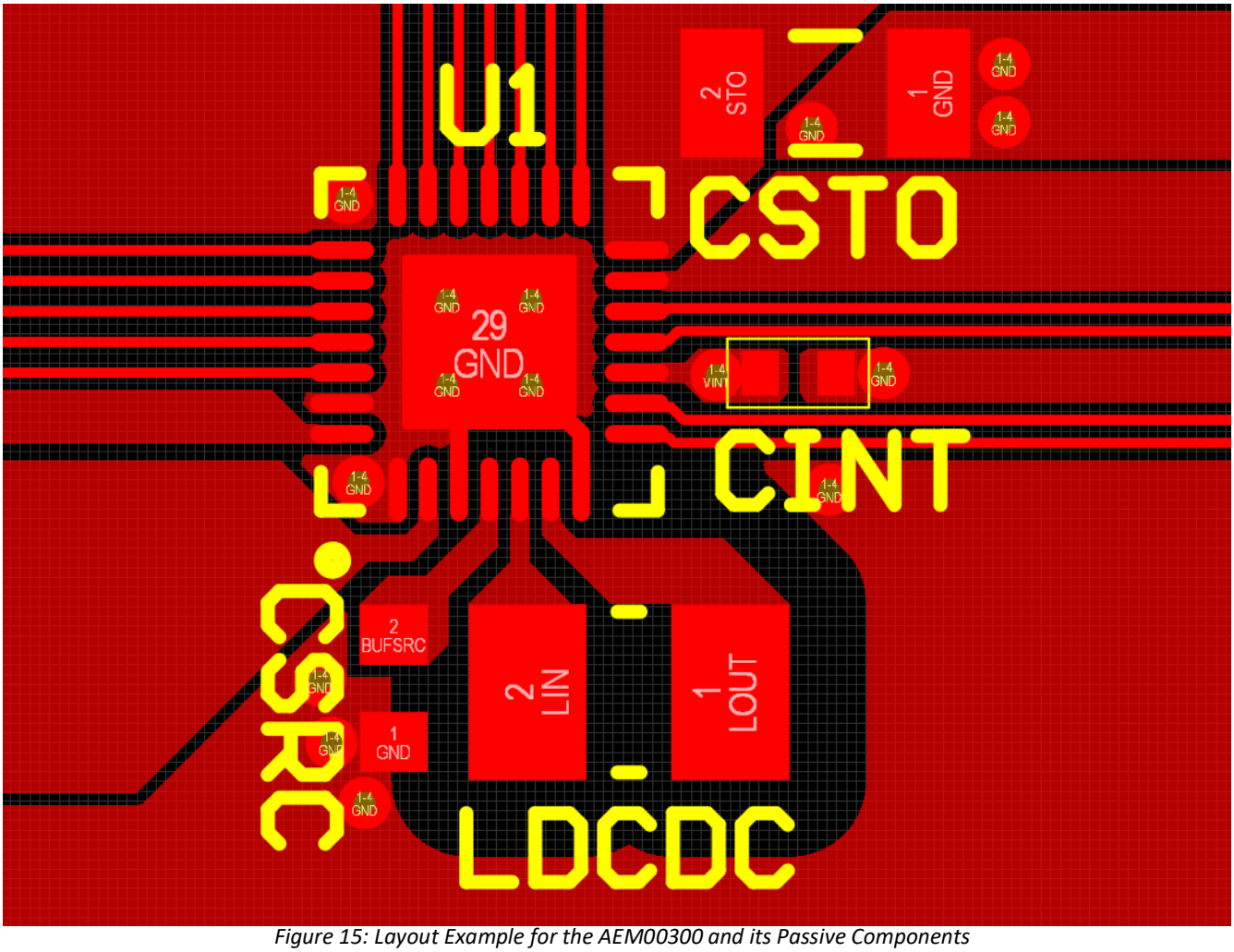

Figure 15: Layout Example for the AEM00300 and its Passive Components

NOTE: schematic, symbol and footprint for the e-peas component can be ordered by contacting e-peas support team at support@e-peas.com

15. Package Information

15.1. Plastic Quad Flatpack No-Lead (QFN 28-pin 4x4mm)

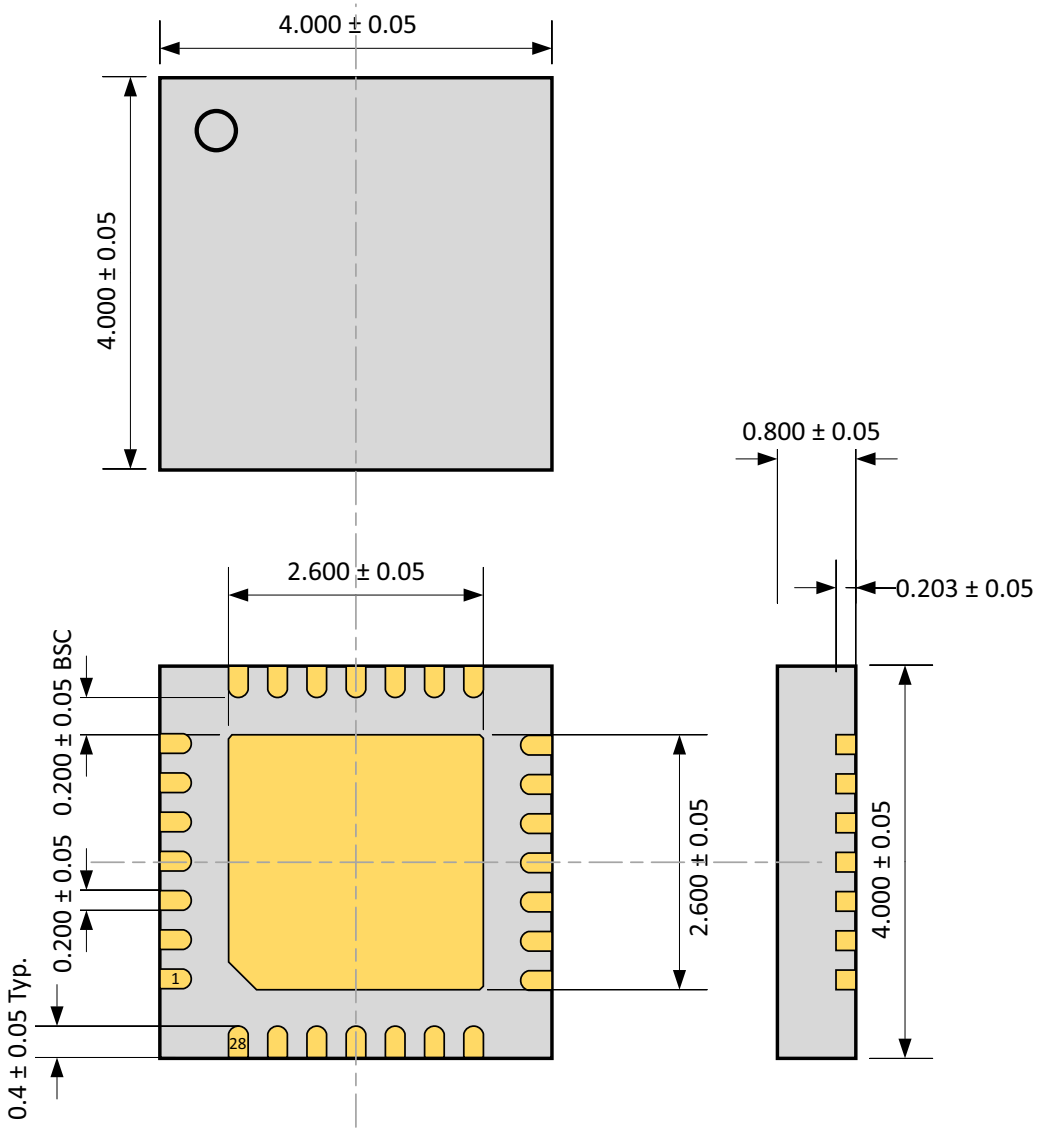

Figure 16: QFN 28-pin 4x4mm Drawing (All Dimensions in mm)

15.2. Board Layout

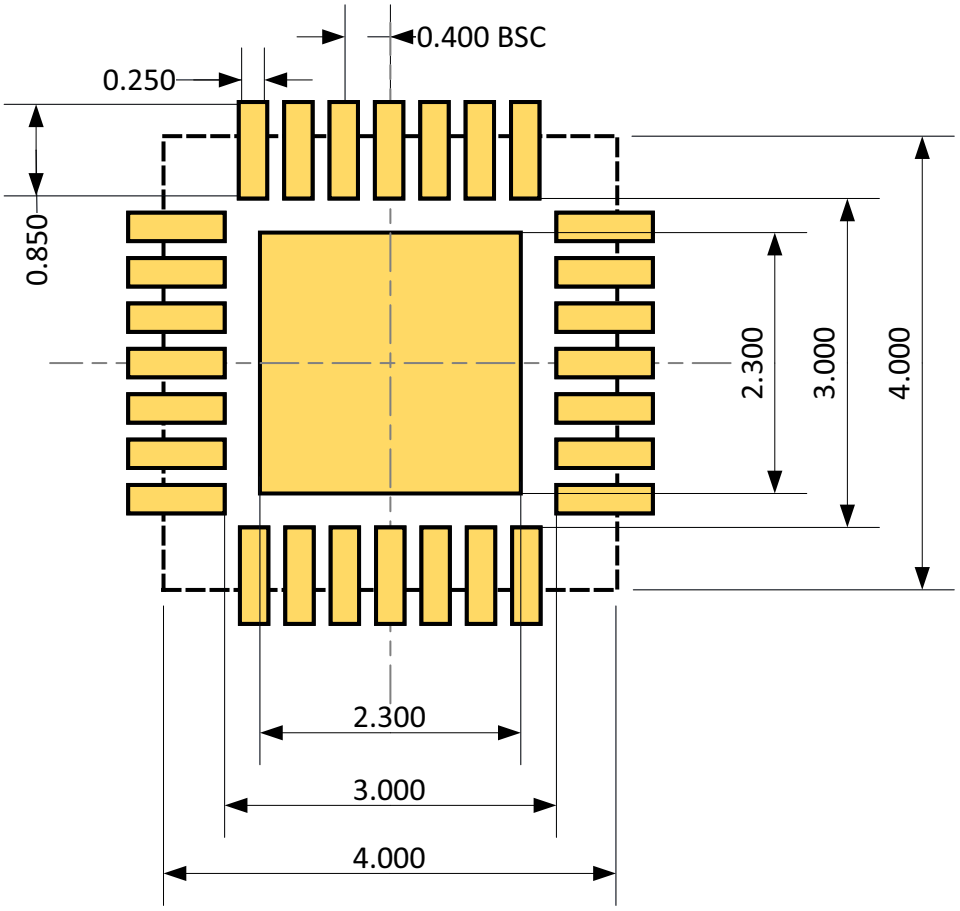

Figure 17: Recommended Board Layout (All Dimensions in mm)

16. Revision History

Revision	Date	Description
0.0	January, 2021	Creation of the document. Preliminary version.
1.0	June, 2021	First version of the document
1.1	August, 2021	Minor modifications
1.2	March, 2023	- Various aesthetic improvements. - Explanations about BAL circuit. - Section with precisions about the use of CS_IN. - Fixed state machine graph. - Fixed footprint dimensions - New “behavior” oscilloscope graphs with improved description. - Moved various states description sections as sub-sections of a global section. - Supply State description: explanation about SRC being set to high impedance when all nodes are fully charged. - Updated "Typical use" of storage element vs STO_CFG[3:0] configuration. - Replaced "asserted/de-asserted" by "HIGH/LOW". - Changed CSRC from 15µF/0402 to 22µF/0603. - Updated "Recommended Operation Conditions" with minimum capacitor values including derating and tolerances. - Source in application example 1: replaced RF by PV cell.
1.3	November, 2023	- Updated efficiency graphs. - Created section for pinout. - Updated schematics with new symbol. - Digital levels High/Low: replaced 0/1 notation by L/H. - Fixed example circuits errors. - Fixed typos and aesthetic issues. - Added layout guidelines with clearer layout examples.
1.4	February, 2024	Fixed wrong HIGH level of ST_STO in “Power and Status Pins” table.

Table 11: Revision History

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Power Management Specialised - PMIC ***category:***

Click to view products by e-peas ***manufacturer:***

Other Similar products are found below :

FAN7710VN LA5657H-N-TLM-E LM10692RMYR SLG7NT4081VTR SLG7NT4192VTR AS3729B-BWLM MB39C831QN-G-EFE2 RT9026GQW LV56841PVD-XH L9781TR P91E0-I5NHGI S6AE102A0DGN1B200 L9916 AP4306BUKTR-G1 SLG7NT4198V NCP392CSFCCT1G LPTM21L-1ABG100I ISL99390FRZ-TR5935 ISL69234IRAZ-T ISL69259IRAZ ISL69228IRAZ ISL69269IRAZ AXP813 FAN53870UC00X FDMF5085 HPM10-W29A100G NCV97311MW50R2G WL2868C-20/TR TLE9263-3BQX TLE9263QX TEA2095T/1J TEA2017AAT/2Y TPS650940A0RSKR TPS65177ARHAR LTC4417IUF#TRPBF AXP313A SQ24806AQSC RK805-2 RK809-2 MFS2633AMBA0AD MFS2613AMDA3AD AD5522JSVUZ-RL LTC4352CMS#TRPBF LTC4359HDCB#TRPBF LT4321IUF#TRPBF TC1017-2.5VLTTR MFS5600AMMA8ES TEA1716T/2 MC33FS8510D3ESR2 MMPF0100NPAZESR2