

## AEM00900 Evaluation Board User Guide

### Description

The AEM00900 evaluation kit (EVK) is a printed circuit board (PCB) featuring all the required components to operate the AEM00900 integrated circuit (IC) in QFN28 package.

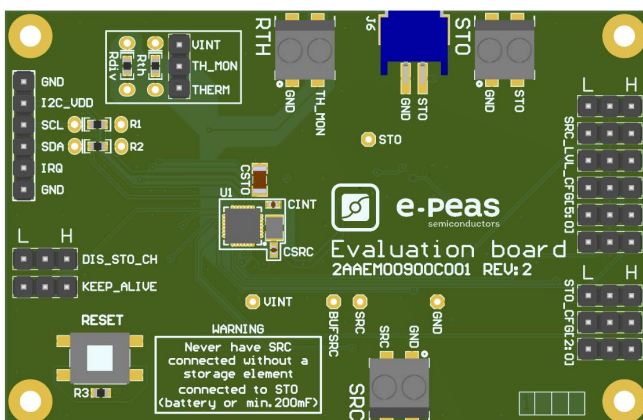
The AEM00900 evaluation board allows users to test the e-peas IC and analyze its performances in a laboratory-like setting or in product mock-ups.

It allows easy connections to an energy harvester (e.g. a single element PV cell) and a storage element. It also provides all the configuration access to set the device in any of the modes described in the datasheet. The control and status signals are available on standard pin headers or through an I<sup>2</sup>C bus communication, allowing users to override preconfigured board settings through host MCU and evaluate the IC performances.

The AEM00900 EVK is a plug and play, intuitive and efficient tool to optimize the AEM00900 configuration, allowing users to design a highly efficient subsystem for the desired target application. Component replacement and operating mode switching is convenient and easy.

More detailed information about AEM00900 features can be found in the datasheet.

### Appearance



### Features

#### Two-way screw terminals

- Source of energy (DC).
- Energy storage element (battery).
- Thermistor used for thermal monitoring.

#### 2-pin "Shrouded Header"

- Alternative connector for the storage element.

#### 3-pin headers

- Constant source voltage (SRC\_LVL\_CFG) configuration.
- Energy storage element threshold configuration.
- Mode configuration.
- Thermal monitoring configuration.

#### 6-pin header

- I<sup>2</sup>C communication pins.

### Applications

Wearable Electronics	Keyboards
Remote Control Units	Electronic Shelf Labels
Smart Buildings	Indoor Sensors

### Evaluation Kit Information

Part Number	Dimensions
2AAEM00900C001 REV:2	76 mm x 50 mm

### Device Information

Part Number	Package	Body size
10AEM00900C0000	QFN 28-pin	4x4mm

# 1. Connections Diagram

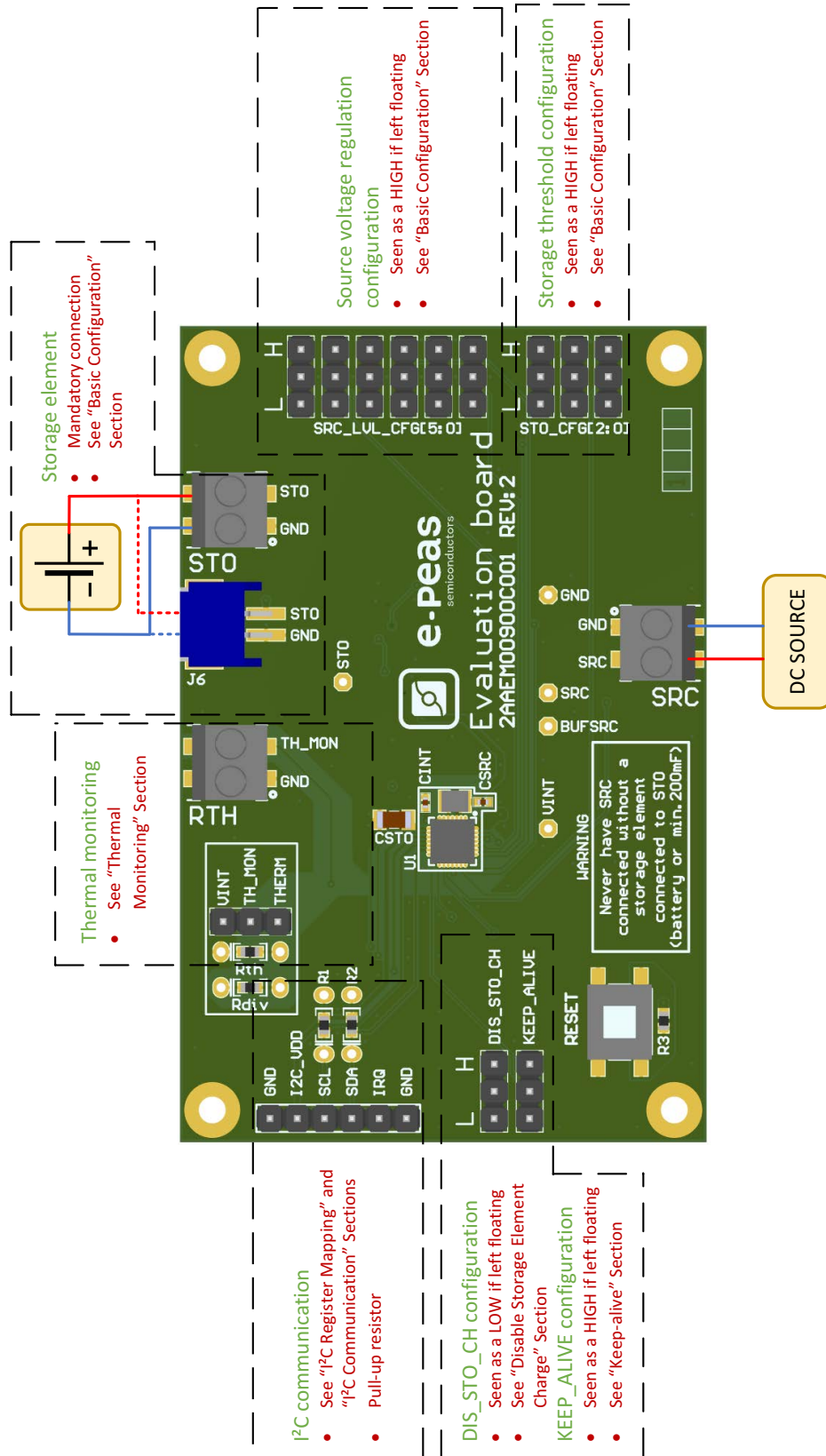


Figure 1: Connection diagram

## 1.1. Signals Description

NAME	FUNCTION	CONNECTION	
		If used	If not used
<b>Power signals</b>			
<b>SRC</b>	Connection to the harvested energy source.	Connect the source element.	Can be left floating.
<b>STO</b>	Connection to the energy storage element.	Cannot be left floating, voltage must always be above 2.8 V.	
<b>I<sup>2</sup>C_VDD</b>	Connection to I <sup>2</sup> C voltage supply.	Connect to I <sup>2</sup> C supply.	Connect to GND.
<b>VINT</b>	AEM Internal voltage supply.		
<b>BUFSRC</b>	AEM connection to a capacitor buffering the boost converter input (no connector on EVK).		
<b>Configuration signals</b>			
<b>SRC_LVL_CFG[5:0]</b>	Used for the configuration of the source voltage level.	Connect jumpers.	Read as high if left floating.
<b>STO_CFG[2:0]</b>	Configuration of the threshold voltages for the energy storage element.	Connect jumpers.	Read as high if left floating.
<b>TH_MON</b>	Configuration of the thermal monitoring.	Connect a thermistor.	Connect to <b>VINT</b> .
<b>Control signals</b>			
<b>DIS_STO_CH</b>	Disabling pin for the storage charging.	Connect jumper (see Section 2.5.1).	Read as low if left floating.
<b>KEEP_ALIVE</b>	Enabling pin to supply internal circuitry from the storage element if no power on <b>SRC</b> .	Connect jumper (see Section 2.5.1).	Read as low if left floating.
<b>I<sup>2</sup>C signals</b>			
<b>SDA</b>	Bidirectional data line.	Connect to host I <sup>2</sup> C bus.	Connect <b>I<sup>2</sup>C_VDD</b> to GND ( <b>SDA</b> and <b>SCL</b> will be pulled down by <b>R<sub>1</sub></b> and <b>R<sub>2</sub></b> ).
<b>SCL</b>	Unidirectional serial clock.		
<b>IRQ</b>	Interrupt request.	Connect to host GPIO.	Leave floating.

Table 1: Pin description

## 2. General Considerations

### 2.1. Safety Information

Always connect the elements in the following order:

1. Reset the board: push the “RESET” (SW2) switch during 5 seconds minimum.
2. Completely configure the PCB (jumpers/resistors):
  - Battery configuration.
  - Mode configuration.
  - Thermal monitoring configuration.
3. Connect I2C\_VDD:
  - To GND if I<sup>2</sup>C is not used (SDA and SCL will also be connected to GND through their pull up resistors).
  - To a power supply if I<sup>2</sup>C is used (1.5 V to 2.2 V).
4. Connect the storage elements on STO with a voltage higher than 2.8 V.
5. Connect the source to the SRC connector (open circuit voltage lower than 2.0 V).

## 2.2. Basic Configurations

Configuration pins						Voltage Level
SRC_LVL_CFG[5:0]						$V_{SRC,REG}$
L	L	L	H	H	L	0.12 V
L	L	L	H	H	H	0.13 V
L	L	H	L	L	L	0.15 V
L	L	H	L	L	H	0.16 V
L	L	H	L	H	L	0.18 V
L	L	H	L	H	H	0.19 V
L	L	H	H	L	L	0.21 V
L	L	H	H	L	H	0.22 V
L	L	H	H	H	L	0.24 V
L	L	H	H	H	H	0.25 V
L	H	L	L	L	L	0.27 V
L	H	L	L	L	H	0.28 V
L	H	L	L	H	L	0.30 V
L	H	L	L	H	H	0.33 V
L	H	L	H	L	L	0.36 V
L	H	L	H	L	H	0.39 V
L	H	L	H	H	L	0.42 V
L	H	L	H	H	H	0.45 V
L	H	H	L	L	L	0.48 V
L	H	H	L	L	H	0.51 V
L	H	H	L	H	L	0.54 V
L	H	H	L	H	H	0.57 V
L	H	H	H	L	L	0.60 V
L	H	H	H	L	H	0.63 V
L	H	H	H	H	L	0.66 V
L	H	H	H	H	H	0.69 V

Configuration pins						Voltage Level
SRC_LVL_CFG[5:0]						$V_{SRC,REG}$
H	L	L	L	L	L	0.72 V
H	L	L	L	L	H	0.75 V
H	L	L	L	H	L	0.78 V
H	L	L	L	H	H	0.81 V
H	L	L	H	L	L	0.84 V
H	L	L	H	L	H	0.87 V
H	L	L	H	H	L	0.90 V
H	L	L	H	H	H	0.93 V
H	L	H	L	L	L	0.96 V
H	L	H	L	L	H	0.99 V
H	L	H	L	H	L	1.02 V
H	L	H	L	H	H	1.05 V
H	L	H	H	L	L	1.08 V
H	L	H	H	L	H	1.11 V
H	L	H	H	H	L	1.14 V
H	L	H	H	H	H	1.17 V
H	H	L	L	L	L	1.20 V
H	H	L	L	L	H	1.23 V
H	H	L	L	H	L	1.26 V
H	H	L	L	H	H	1.29 V
H	H	L	H	L	L	1.32 V
H	H	L	H	L	H	1.35 V
H	H	L	H	H	L	1.38 V
H	H	L	H	H	H	1.41 V
H	H	H	L	L	L	1.44 V
H	H	H	L	L	H	1.47 V

Table 2: Configuration of SRC\_LVL\_CFG[5:0]



Configuration	Availability Through Pins		Storage Element Threshold Voltage	
	I <sup>2</sup> C Interface	Configuration pins	V <sub>OVCH</sub>	V <sub>OVDIS</sub>
STO_CFG[2:0]				
LLL	yes	yes	4.50 V	3.30 V
LLH	yes	yes	4.00 V	2.80 V
LHL	yes	yes	3.63 V	2.80 V
LHH	yes	yes	3.90 V	2.80 V
HLL	yes	yes	3.90 V	3.50 V
HLH	yes	yes	3.90 V	3.01 V
HHL	yes	yes	4.35 V	3.01 V
HHH	yes	yes	4.12 V	3.01 V

Table 3: Usage of STO\_CFG[2:0]

## 2.3. I<sup>2</sup>C Register Map

Address	Name	Bit	Field Name	Access	RESET	Description
0x00	VERSION	[3:0]	MINOR	R	-	Chip ID
		[7:4]	MAJOR	R	-	
0x01	SRCREGU	[6:0]	VALUE	R/W	0x77 (1.47V)	Source voltage regulation
0x02	VOVDIS	[5:0]	THRESH	R/W	0x2D (3.05V)	Overdischarge level of the storage element
0x03	VOVCH	[5:0]	THRESH	R/W	0x33 (4.1V)	Overcharge level of the storage element
0x04	TEMPCOLD	[7:0]	THRESH	R/W	0x8F (0°C)	Cold temperature level
0x05	TEMPHOT	[7:0]	THRESH	R/W	0x2F (45°C)	Hot temperature level
0x06	PWR	[0:0]	KEEPALEN	R/W	0x01	Keepalive enable
		[1:1]	HPEN	R/W	0x01	High power mode enable
		[2:2]	TMONEN	R/W	0x01	Temperature monitoring enable
		[3:3]	STOCHDIS	R/W	0x00	Battery charging disable
0x07	SLEEP	[0:0]	EN	R/W	0x01	Sleep mode enable
0x08	STOMON	[2:0]	RATE	R/W	0x00	ADC rate
0x09	APM	[0:0]	EN	R/W	0x00	APM enable
		[1:1]	MODE	R/W	0x00	APM mode
		[3:2]	WINDOW	R/W	0x00	APM computation window
0x0A	IRQEN	[0:0]	I2CRDY	R/W	0x01	IRQ serial interface ready enable
		[1:1]	VOVDIS	R/W	0x00	IRQ STO OVDIS enable
		[2:2]	VOVCH	R/W	0x00	IRQ STO OVCH enable
		[3:3]	SLPTHRESH	R/W	0x00	IRQ SRC LOW enable
		[4:4]	TEMP	R/W	0x00	IRQ temperature enable
		[5:5]	APMDONE	R/W	0x00	IRQ APM done enable
0x0B	CTRL	[0:0]	UPDATE	R/W	0x00	Load I <sup>2</sup> C registers configuration
		[2:2]	SYNCBUSY	R	0x00	Synchronization busy flag
0x0C	IRQFLG	[0:0]	I2CRDY	R	0x00	IRQ serial interface ready flag
		[1:1]	VOVDIS	R	0x00	IRQ STO OVDIS flag
		[2:2]	VOVCH	R	0x00	IRQ STO OVCH flag
		[3:3]	SLPTHRESH	R	0x00	IRQ SRC LOW flag
		[4:4]	TEMP	R	0x00	IRQ temperature flag
		[5:5]	APMDONE	R	0x00	IRQ APM done flag
0x0D	STATUS	[1:1]	VOVDIS	R	0x00	Status STO OVDIS
		[2:2]	VOVCH	R	0x00	Status STO OVCH
		[3:3]	SLPTHRESH	R	0x00	Status SRC LOW
		[4:4]	TEMP	R	0x00	Status temperature
		[6:6]	CHARGE	R	0x00	Status STO Charge
0x0E	APM0	[7:0]	DATA	R	0x00	APM data 0
0x0F	APM1	[7:0]	DATA	R	0x00	APM data 1
0x10	APM2	[7:0]	DATA	R	0x00	APM data 2
0x11	TEMP	[7:0]	DATA	R	0x00	Temperature data
0x12	STO	[7:0]	DATA	R	0x00	Storage element voltage
0x13	SRC	[7:0]	DATA	R	0x00	SRC ADC value

Table 4: Register summary

## 2.4. I<sup>2</sup>C Communication

The device address on the I<sup>2</sup>C bus is 0x41. All information about the I<sup>2</sup>C communication is available in the AEM00900 datasheet, "System configuration" Section.

I<sup>2</sup>C\_VDD must be connected to an external power supply which voltage is within the 1.5 V to 2.2 V range. On the Evaluation Board, 1 kΩ pull-up on SDA and SCL (R1 and R2) to I<sup>2</sup>C\_VDD are provided.

In case one or more configurations are set by I<sup>2</sup>C communication, none of the configuration pins (GPIOs) will be taken into account anymore. Thus, applying the default values to any registers that have not been explicitly configured by I<sup>2</sup>C.

## 2.5. Advanced Configurations

A complete description of the system constraints and configurations is available in Section "System configuration" of the AEM00900 datasheet.

### 2.5.1. Mode Configuration

#### DIS\_STO\_CH

Enabling/disabling battery charging can be done by setting a jumper on the corresponding 3-pin header.

- Use a jumper to connect the DIS\_STO\_CH to H to disable the charge of the storage element.
- Use a jumper to connect the DIS\_STO\_CH to L to enable the charge of the storage element.

#### KEEP\_ALIVE

The KEEP\_ALIVE feature allows to supply the internal circuitry from the storage element when no power is available on the source terminal.

- Use a jumper to connect the KEEP\_ALIVE to H to enable the feature.
- Use a jumper to connect the KEEP\_ALIVE to L to disable the feature.

### 2.5.2. Thermal Monitoring

The thermal monitoring feature protects the battery by disabling the battery charging when ambient temperature is outside a specified range. The higher and lower thresholds are configurable using the I<sup>2</sup>C communication (see datasheet).

- Place a jumper between TH\_MON and VINT to disable the feature.
- Place a jumper between TH\_MON and THERM to enable the feature.



## 3. Functional Tests

This section presents a few simple tests that allow users to understand the functional behavior of the AEM00900. To avoid damaging the board, follow the procedure found in Section 2.1 “Safety Information”. If a test has to be restarted, make sure to properly reset the system to obtain reproducible results.

The measurements use the following equipment:

- Two Source Measurement Units (SMU, four-quadrant power supply).
- One 2-channel oscilloscope.

The following functional tests were made using the following setup:

- EVK jumpers configuration:
  - `SRC_LVL_CFG[5:0]` = LHHHL (0.54 V).
  - `STO_CFG[2:0]` = HHH (3.01 V - 4.12 V).
  - `DIS_STO_CH` = L.
  - `KEEP_ALIVE` = H.
  - Place the jumper to connect `TH_MON` with `VINT`.
- Place a jumper to connect `I2C_VDD` and `GND` if the I<sup>2</sup>C communication is not used.

Users can adapt the setup to match the use case system as long as the input limitations are respected, as well as the minimum storage voltage and cold-start constraints (see “Introduction” Section of AEM00900 datasheet).

### 3.1. Start-up

The following example allows users to observe the start-up behavior of the AEM00900.

#### Setup

- Place oscilloscope probes on `VINT` and `STO`.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”.
- `STO`: SMU set as a 3.0 V voltage source with 1 mA current compliance.
- `SRC`: SMU set as a 1 mA or 100  $\mu$ A current source with 0.8 V voltage compliance.

#### Observations and measurements

- `VINT`: voltage rises to 2.2 V.
- `STO`: observe the current absorbed by the SMU as power is transferred from `SRC` to `STO`.

### 3.2. Shutdown

This test allows users to observe the behavior of the AEM00900 when the system is running out of energy. This test is to be done when the AEM00900 has already started, as at the end of the test described in Section 3.1.

#### Setup

- Disable the `KEEP_ALIVE` feature (`KEEP_ALIVE` = L).
- Place the oscilloscope probe on `VINT`.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1).
- Disconnect the SMU from `SRC`.

#### Observations and measurements

- `VINT`: voltage falls to `GND`.
- `STO`: no leakage from `STO` (probe impedance considered).

### 3.3. Cold Start

The following test allows users to observe the minimum voltage required to coldstart the AEM00900. To prevent current leakage caused by the probe impedance, users should avoid probing any unnecessary node. Make sure to properly reset the board to observe the cold-start behavior.

#### Setup

- Place oscilloscope probe on `SRC`.
- Referring Figure 1, follow steps 1 to 5 explained in Section 2.1.
- `SRC`: SMU set as 20  $\mu$ A current source with 0.3 V voltage compliance.
- `STO`: SMU as 3.0 V voltage source with 100  $\mu$ A current compliance.

#### Observations and measurements

- `SRC` voltage clamped at the cold-start voltage during the cold-start phase and then regulated at the selected source voltage when cold start is over. The duration of the cold-start phase decreases as the input power increases. Select the input power accordingly to be able to observe the cold-start phase.
- `STO`: SMU starts absorbing current sourced by the `STO` pin once the cold-start phase is completed.

### 3.4. Thermal Monitoring

The following test allows users to observe the thermal monitoring functionality.

#### Setup

- Place a 10 kΩ NTC thermistor with  $\beta = 3380$  on  $R_{th}$ .
- Place a 22 kΩ pull-up resistor on  $R_{DIV}$ .
- Place the jumper to connect  $TH\_MON$  with THERM.
- Place the probes on the nodes to be observed.
- Referring to Figure 1, follow steps 1 to 5 as explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1).

#### Observations and measurements

- If the temperature is lower than 0°C, the charge of the storage element is disabled.
- If the temperature is higher than 45°C, the charge of the storage element is disabled.
- If the temperature is between 0°C and 45°C, the charge of the storage element is enabled.

### 3.5. Keep-alive

The **KEEP\_ALIVE** feature sets the behavior of the AEM00900 when no power is available on **SRC**.

#### Setup

- Place the oscilloscope probe on **VINT**.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1).
- Enable the **KEEP\_ALIVE** feature (connect **KEEP\_ALIVE** to H).
- Disconnect the SMU from the **SRC** pin.

#### Observations and measurements

- **VINT**: the internal circuitry is supplied by the storage element ( $V_{VINT}$  does not drop).

### 3.6. Disable Storage Element Charge

The **DIS\_STO\_CH** feature allows to disable the storage element charge.

#### Setup

- Use a jumper to connect **DIS\_STO\_CH** to H to disable the charge of the storage element.
- **STO**: SMU set as a 3.0 V voltage source with 1 mA current compliance.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1).

#### Observations and measurements

- **STO**: observe that no current is absorbed by the SMU on **STO** when power is applied on **SRC**.

### 3.7. I<sup>2</sup>C Communication

This test allows users to change a configuration through the I<sup>2</sup>C communication.

#### Setup

- Place the oscilloscope probe on **SRC**.
- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1).
- Connect **I<sup>2</sup>C\_VDD** to the I<sup>2</sup>C supply (between 1.8 V and 2.2 V).
- Write ‘0010 0011’ (0x23) on the SRCREGU register (0x01), so that constant source voltage is set to 0.285 V).
- Write ‘1’ to the CTRL register (0x0B) to load the I<sup>2</sup>C register configuration (at startup the AEM00900 load its configurations from the pins settings).

#### Observations and measurements

- **SRC**: observe that the voltage regulation switches to 0.285 V, when the register value is loaded.

### 3.8. Efficiency

This test allows users to reproduce the efficiency graphs of the boost converter (see “DCDC Conversion Efficiency” Section in the AEM00900 datasheet).

#### Setup

- Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1 “Safety Information”. Configure the board in the desired state and start the system (see Section 3.1).
- **STO**: connect SMU configured as a 4.7 V voltage source with a 100 mA current compliance.
- **SRC**: connect SMU configured as a source current with a voltage compliance of 1.0 V to ensure the AEM00900 coldstarts.

#### Manipulations

- **STO**: set the SMU to the desired voltage, between  $V_{OVDIS}$  and  $V_{OVCH}$ . Make sure the SMU integration time is as long as possible.

- **SRC**: sweep the source level voltage by either changing the **SRC\_LVL\_CFG[5:0]** pins connections (jumpers) or by writing the SRCREGU register by I<sup>2</sup>C communication.

#### Observations and measurements

- For each data point of the **SRC** voltage sweep, note the **SRC** SMU voltage and current, as well as the **STO** SMU voltage and current. Repeat the measurement for each data point a copious number of times to ensure capturing current peaks.
- The efficiency  $\eta$  in percent is computed by applying the following formula:

$$\eta = 100 \cdot \frac{V_{STO} \cdot I_{STO}}{V_{SRC} \cdot I_{SRC}}$$

*NOTE: to ensure optimal efficiency, make sure a minimal decoupling capacitance of 22  $\mu$ F is present on the STO pin.*

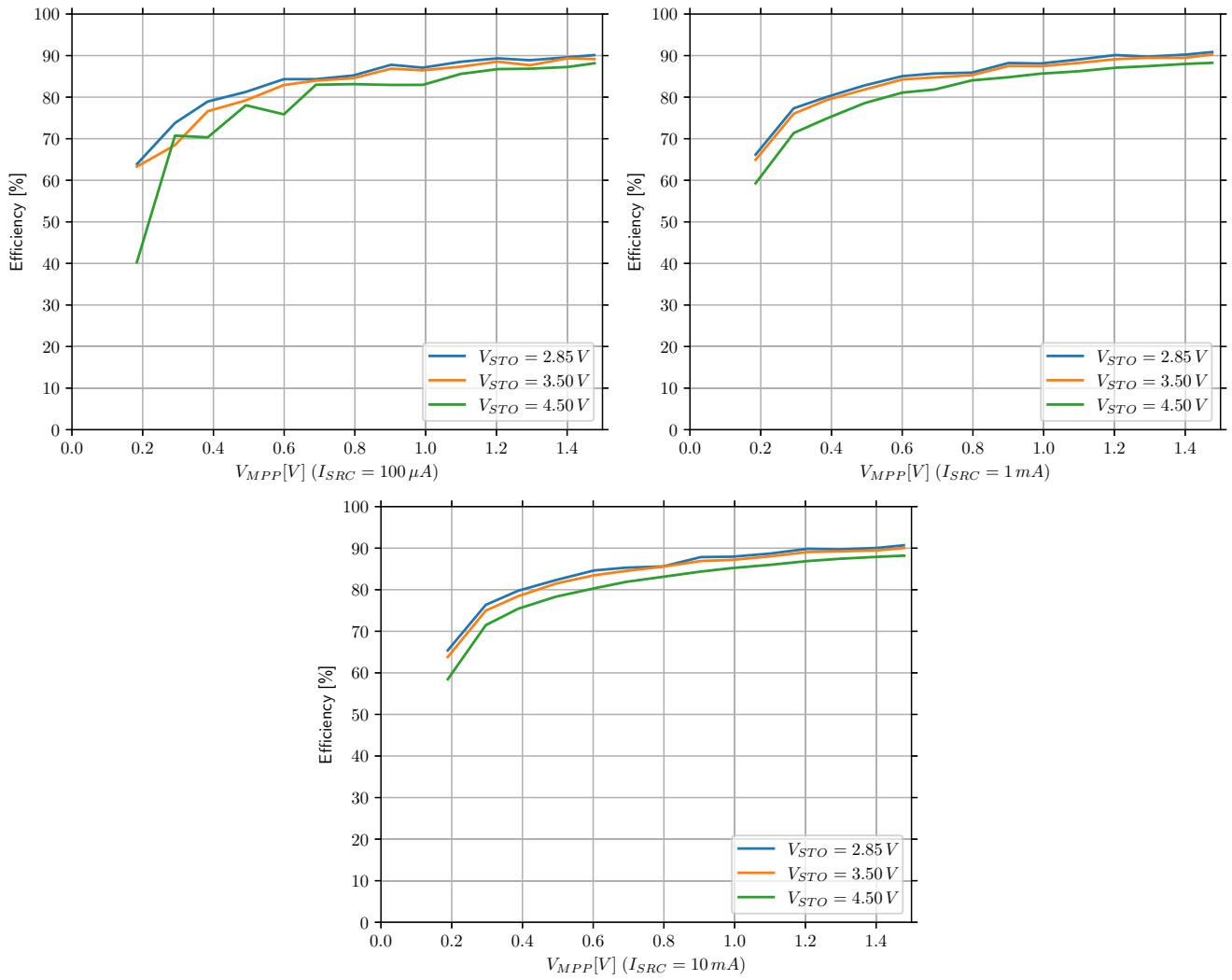


Figure 2: AEM00900 efficiency (LDCDC: TDK VLS252012HBX-6R8M-1)

## 4. Schematics

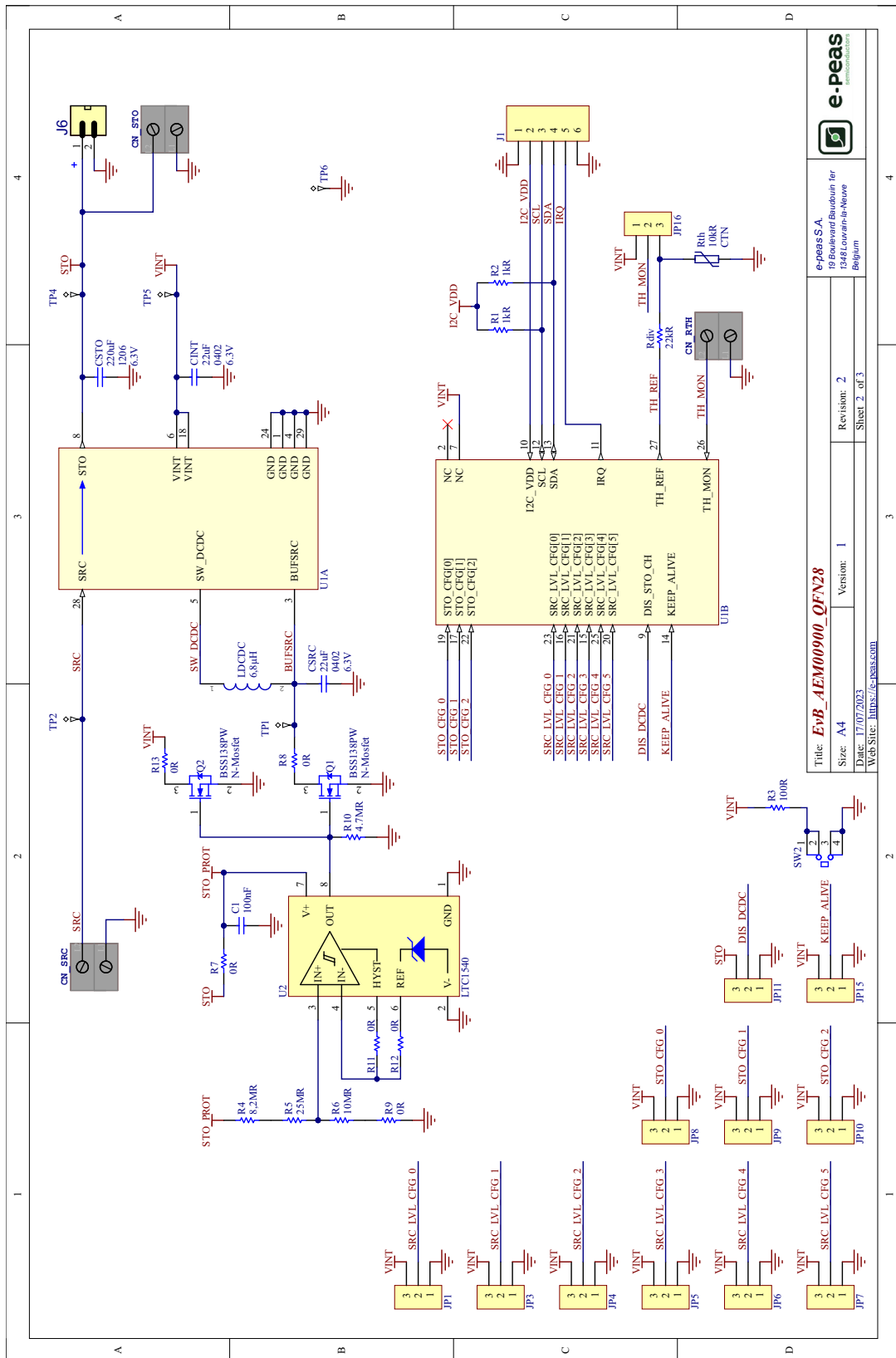


Figure 3: AEM00900 Evaluation Board Schematic

## 5. Revision History

EVK Version	User Guide Revision	Date	Description
Up to 1.1	1.0	February, 2022	Creation of the document.
1.2	1.0	September, 2023	Fixed some inconsistencies and updated images.

Table 5: Revision History

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