DATASHEET

AEM10941

Highly efficient, regulated dual-output, ambient energy manager for up to 7-cell solar panels with optional primary battery

Features

Ultra-low-power start-up:
- Cold start from 380 mV input voltage and 3 µW input power (typical)

Ultra-low-power boost regulator:
- Open-circuit voltage sensing for MPPT every 5 s
- Configurable MPPT with 2-pin programming
- Selectable Voc ratios of 70, 75, 85 or 90%
- Input voltage operation range from 50 mV to 5 V
- MPPT voltage operation range from 50 mV to 5 V

Integrated 1.2/1.8 V LDO regulator:
- Up to 20 mA load current
- Power gated dynamically by external control
- Selectable output voltage

Integrated 1.8 V-4.1 V LDO regulator:
- Up to 80 mA load current with 300 mV drop-out
- Power gated dynamically by external control
- Selectable or adjustable output voltage

Flexible energy storage management:
- Selectable overcharge and overdischarge protection for any type of rechargeable battery or (super)capacitor
- Fast supercapacitor charging
- Warning when the battery is running low
- Warning when output voltage regulators are available

Optional primary battery:
- Automatic switching to the primary battery when the secondary battery is exhausted

Integrated balun for dual-cell supercapacitor

Applications

- PV cell harvesting
- Industrial monitoring
- Geolocation
- Home automation
- E-health monitoring
- Wireless sensor nodes

Description

The AEM10941 is an integrated energy management circuit that extracts DC power from up to 7-cell solar panels to simultaneously store energy in a rechargeable element and supply the system with two independent regulated voltages. The AEM10941 allows to extend battery lifetime and ultimately eliminates the primary energy storage element in a large range of wireless applications, such as industrial monitoring, geolocation, home automation, e-health monitoring and wireless sensor nodes.

The AEM10941 harvests the available input current up to 110 mA. It integrates an ultra-low-power boost converter to charge a storage element, such as a Li-ion battery, a thin film battery, a supercapacitor or a conventional capacitor. The boost converter operates with input voltages in a range from 50 mV to 5 V. With its unique cold start circuit, it can start operating with empty storage elements at an input voltage as low as 380 mVand an input power of just 3 µW.

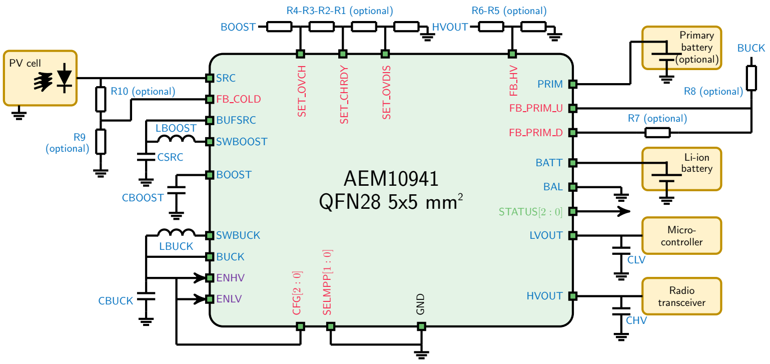
The low-voltage supply typically drives a microcontroller at 1.2 V or 1.8 V. The high-voltage supply typically drives a radio transceiver at a configurable voltage between 1.8 V and 4.1 V. Both are driven by highly-efficient LDO (Low Drop-Out) regulators for low noise and high stability.

Configuration pins determine various operating modes by setting predefined conditions for the energy storage element (overcharge or overdischarge voltages), and by selecting the voltage of the high-voltage supply and the low-voltage supply. Moreover, special modes can be obtained at the expense of a few configuration resistors.

The chip integrates all the active elements for powering a typical wireless sensor. Five capacitors and two inductors are required, available in the small 0402 and 0603 size, respectively. With only seven external components, integration is maximum, footprint and BOM are minimum, optimizing the time-to-market and the costs of WSN designs.

Device information

Part number	Package	Body size
10AEM10941C0000	QFN 28-pin	5 mm x 5 mm



Contents

List of Figures

List of Tables

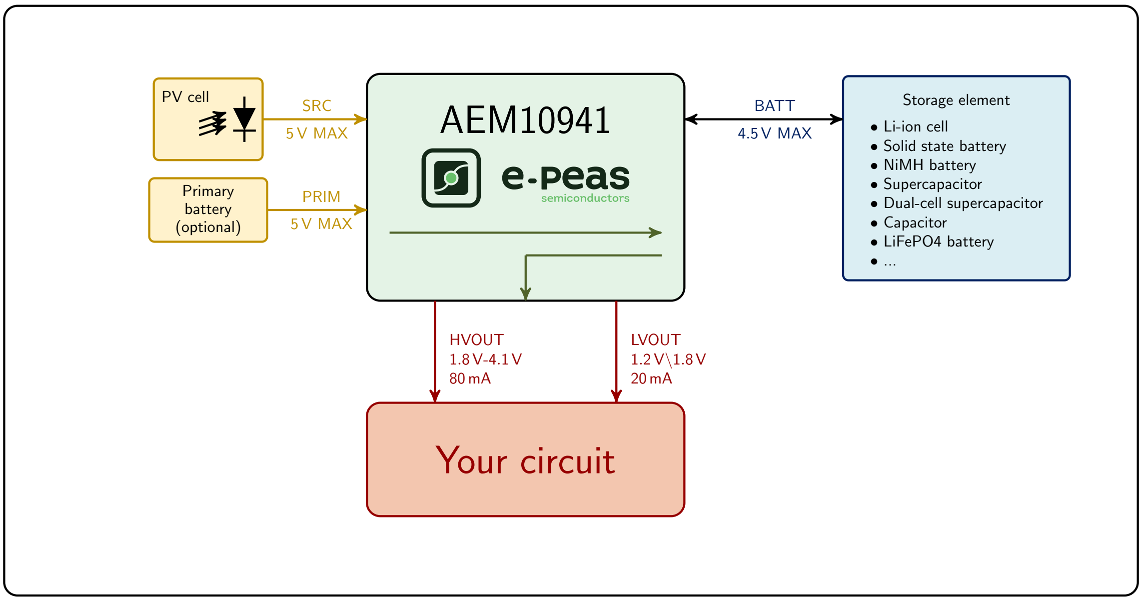


Figure 1: Simplified schematic view

1 Introduction

The AEM10941 is a full-featured energy efficient power management circuit able to charge a storage element (battery or supercapacitor, connected to BATT) from an energy source (connected to SRC) as well as to supply loads at different operating voltages through two powers supplying LDO regulators (LVOUT and HVOUT).

The heart of the AEM10941 is a cascade of two regulated switching converters, namely the boost converter and the buck converter with high-power conversion efficiency (See page 18).

At first start-up, as soon as a required cold start voltage of 380 mV and a scant amount of power of just 3 µW available from the harvested energy source, the AEM cold starts. After the cold start, the AEM can extract the power available from the source as long as the input voltage is comprised between 50 mV and 5 V. Note that the minimum voltage for the cold start may be set by adding resistors (see page 12).

Through three configuration pins (CFG[2:0]), the user can select a specific operating mode from a range of seven modes that cover most application requirements without any dedicated external component. These operating modes define the LDO output voltages and the protection levels of the storage element. Note that a custom mode allows the user to define his own storage element protection levels and the output voltage of the high-voltage LDO (See page 11).

The Maximum Power Point (MPP) ratio can be configured using two configuration pins (SELMPP[1:0]) (See page 12).

Two logic control pins are provided (ENLV and ENHV) to dynamically activate or deactivate the LDO regulators that supply the low and high-voltage load, respectively. The status pin STATUS[0] alerts the user that the LDOs are operational and can be enabled. This signal can also be used to enable an optional external regulator.

If the battery voltage gets depleted, the LDOs are power gated and the controller is no longer supplied by the storage element to protect it from further discharge. Around 600 ms before the shutdown of the AEM, the status pin STATUS[1] alerts the user for a clean shutdown of the system.

However, if the storage element gets depleted and an optional primary battery is connected on PRIM, the chip automatically uses it as a source to recharge the storage element before switching back to the ambient source. This guarantees continuous operation even under the most adverse conditions (See page 10). STATUS[1] is asserted when the primary battery is providing power.

The status of the MPP controller is reported with one dedicated status pin (STATUS[2]). The status pin is asserted when an MPP calculation is being performed.

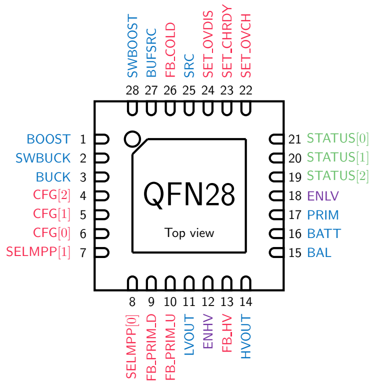


Figure 2: Pinout diagram QFN28

NAME	PIN NUMBER	FUNCTION	
Power pins			
BOOST	1	Output of the boost converter.	
SWBUCK	2	Switching node of the buck converter.	
BUCK	3	Output of the buck converter.	
LVOUT	11	Output of the low voltage LDO regulator.	
HVOUT	14	Output of the high voltage LDO regulator.	
BAL	15	Connection to mid-point of a dual-cell supercapacitor (optional). Must be connected to GND if not used.	
BATT	16	Connection to the energy storage element, battery or capacitor. Cannot be left floating.	
PRIM	17	Connection to the primary battery (optional). Must be connected to GND if not used.	
SRC	25	Connection to the harvested energy source.	
BUFSRC	27	Connection to an external capacitor buffering the boost converter input.	
SWBOOST	28	Switching node of the boost converter.	
Configuration pins			
CFG[2]	4	Used for the configuration of the threshold voltages for the energy storage element and the output voltage of the LDOs.	See page 11
CFG[1]	5		
CFG[0]	6		
SELMPP[1]	7	Used for the configuration of the MPP ratio.	
SELMPP[0]	8		
FB_PRIM_D	9	Used for the configuration of the primary battery (optional). Must be connected to GND if not used.	
FB_PRIM_U	10		
FB_HV	13	Used for the configuration of the high-voltage LDO in the custom mode (optional). Must be left floating if not used.	
SET_OVCH	22	Used for the configuration of the threshold voltages for the energy storage element in the custom mode (optional). Must be left floating if not used.	
SET_CHRDY	23		
SET_OVDIS	24		
FB_COLD	26	Used for the configuration of the cold start (optional). Must be connected to SRC if not used.	
Control pins			
ENHV	12	Enabling pin for the high-voltage LDO.	See page 9
ENLV	18	Enabling pin for the low-voltage LDO.	
Status pins			
STATUS[2]	19	Logic output. Asserted when the AEM performs a MPP evaluation.	See pages 8-10
STATUS[1]	20	Logic output. Asserted if the battery voltage falls below Vovdis or if the AEM is taking energy from the primary battery.	
STATUS[0]	21	Logic output. Asserted when the LDOs can be enabled.	
Other pins			
GND	Exposed Pad	Ground connection, should be solidly tied to the PCB ground plane.	

Table 1: Pins description

2 Absolute Maximum Ratings

Parameter	Rating
Vsrc	5.5 V
Operating junction temperature	-40 °C to +125 °C
Storage temperature	-65 °C to +150 °C

Table 2: Absolute maximum ratings

3 Thermal Resistance

Package	θ_{JA}	θ_{JC}	Unit
QFN28	38.3	2.183	°C/W

Table 3: Thermal data

ESD CAUTION		
	ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.	
V_{ESD}	Human-body model according to Jedec JS001-2017	± 500 V
	Charge device model according to Jedec JS002-2014	± 1.000 V

4 Typical Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input voltage and input power						
$Psrc_{CS}$	Source power required for cold start.	During cold start	3			μW
Vsrc	Input voltage of the energy source.	During cold start	0.38		5	V
		After cold start	0.05		5	
Isrc	Input current of the energy source				110	mA
V_{CS}	Custom cold start voltage.	During the cold start (See page 12)	0.5		4	V
DC-DC converters						
Vboost	Output of the boost converter.	During normal operation	2.2		4.5	V
Vbuck	Output of the buck converter.	During normal operation	2	2.2	2.5	
Storage element						
Vbatt	Voltage on the storage element.	Rechargeable battery	2.2		4.5	V
		Capacitor	0		4.5	V
Tcrit	Time before shutdown once STATUS[1] has been asserted.		400	600	800	ms
Vprim	Voltage on the primary battery.		0.6		5	V
Iprim	Current from the primary battery.			20		mA
Vfb_prim_u	Feedback for the minimal voltage level on the primary battery.		0.15		1.1	V
Vovch	Maximum voltage accepted on the storage element before disabling the boost converter.	see Table 7	2.3		4.5	V
Vchrdy	Minimum voltage required on the storage element before enabling the LDOs after a cold start.	see Table 7	2.25		4.45	V
Vovdis	Minimum voltage accepted on the storage element before switching to primary battery or entering into a shutdown.	see Table 7	2.2		4.4	V
Low-voltage LDO regulator						
Vlv	Output voltage of the low-voltage LDO.	see Table 7	1.2		1.8	V
Ilv	Load current from the low-voltage LDO.		0		20	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High-voltage LDO regulator						
Vhv	Output voltage of the high-voltage LDO.	see Table 7	1.8		Vbatt - 0.3	V
Ihv	Load current from the high-voltage LDO.		0		80	mA
Logic output pins						
STATUS[2:0]	Logic output levels on the status pins.	Logic high (VOH)	1.98	Vbatt		V
		Logic low (VOL)	-0.1		0.1	V

Table 4: Electrical characteristics

5 Recommended Operation Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External components						
CSRC	Capacitor decoupling the BUFSRC pin.		8	10	150	µF
CBOOST	Capacitor of the boost converter.		10	22	25	µF
LBOOST	Inductor of the boost converter.		4	10	25	µH
CBUCK	Capacitor of the buck converter.		8	10	22	µF
LBUCK	Inductor of the buck converter.		4	10	25	µH
CLV	Capacitor decoupling the low-voltage LDO regulator.		8	10	14	µF
CHV	Capacitor decoupling the high-voltage LDO regulator.		8	10	14	µF
CBATT	**Optional** - Capacitor on BATT if no storage element is connected (See page 12).		150			µF
RT	**Optional** - Resistor for setting threshold voltage of the battery in custom mode. Equal to R1 + R2 + R3 + R4 (See page 11).		1	10	100	MΩ
RV	**Optional** - Resistor for setting the output voltage of the high-voltage LDO in custom mode. Equal to R5 + R6 (See page 11)		1	10	40	MΩ
RC	**Optional** - Resistor for the cold start configuration. Equal to R9 + R10 (See page 12).		0.1		10	MΩ
RP	**Optional** - Resistor to be used with a primary battery. Equal to R7 + R8 (See page 12).		100		500	kΩ
Logic input pins						
ENHV	Enabling pin for the high-voltage LDO[1].	Logic high (VOH)	1.75	Vbuck	Vbuck	V
		Logic low (VOL)	-0.01	0	0.01	
ENLV	Enabling pin for the low-voltage LDO[2].	Logic high (VOH)	1.75	Vbuck	Vboost	V
		Logic low (VOL)	-0.01	0	0.01	
SELMPP[1:0]	Configuration pins for the MPP evaluation (see Table 8).	Logic high (VOH)	Connect to BUCK			
		Logic low (VOL)	Connect to GND			
CFG[2:0]	Configuration pins for the storage element (see Table 7).	Logic high (VOH)	Connect to BUCK			
		Logic low (VOL)	Connect to GND			

Table 5: Recommended operating conditions

Note 1: ENHV can be dynamically driven by a logic signal from the LV domain. For a static usage, connect to BUCK (High) or GND (Low).
Note 2: ENLV can be dynamically driven by a logic signal from the HV domain. For a static usage, connect to BUCK or BOOST (High) or GND (Low).

6 Functional Block Diagram

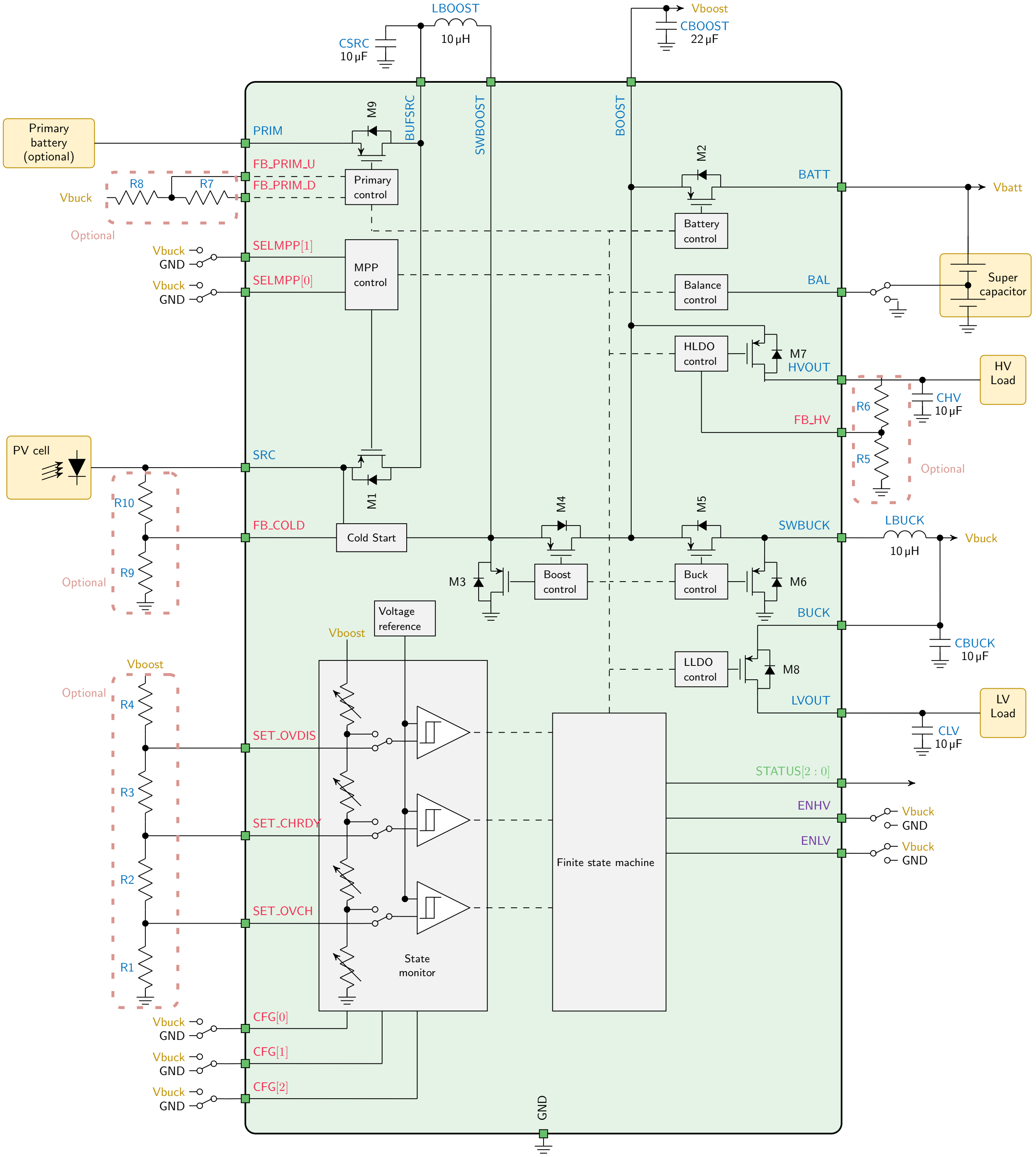


Figure 3: Functional block diagram

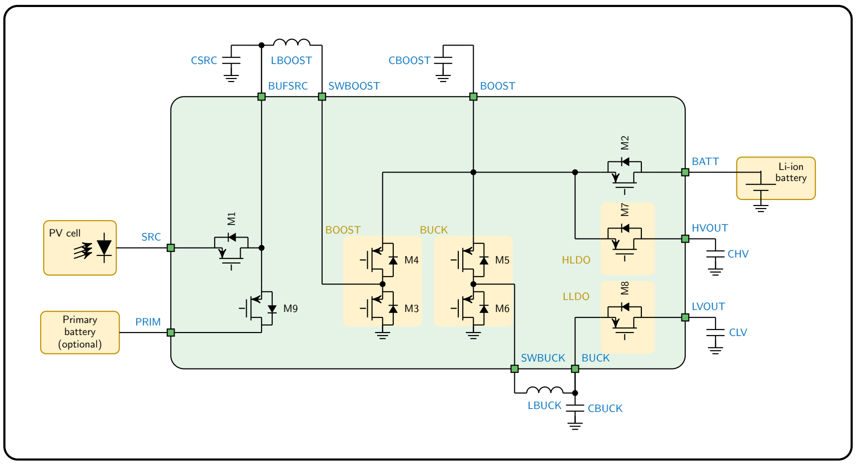


Figure 4: Simplified schematic view of the AEM10941

7 Theory of Operation

7.1 Deep sleep & Wake up modes

The DEEP SLEEP MODE is a state where all nodes are deeply discharged and there is no available energy to be harvested. As soon as the required cold start voltage of 380 mV and a sparse amount of power of just 3 µW becomes available on SRC, the WAKE UP MODE is activated. Vboost and Vbuck rise up to a voltage of 2.2 V. Vboost then rises alone up to Vovch.
Note that the required cold start voltage can be configured as explained in the Cold start configuration section on Page 12.
At that stage, both LDOs are internally deactivated. Therefore, STATUS[0] is equal to 0 as shown in Figure 9 and Figure 10.
When Vboost reaches Vovch, two scenarios are possible: in the first scenario, a supercapacitor or a capacitor having a voltage lower than Vchrdy is connected to the BATT node. In the second scenario, a charged battery is connected to the BATT node.

Supercapacitor as a storage element

If the storage element is a supercapacitor, the storage element may need to be charged from 0 V. The boost converter charges BATT from the input source and by modulating the conductance of M2. During the charge of the BATT node, both LDOs are deactivated and STATUS[0] is de-asserted. When Vbatt reaches Vchrdy, the circuit goes to NORMAL MODE, STATUS[0] is asserted and the LDOs can be activated by the user using the ENLV and ENHV control pins as shown in Figure 9.

Battery as a storage element

If the storage element is a battery, but its voltage is lower than Vchrdy, then the storage element first needs to be charged until it reaches Vchrdy. Once Vbatt exceeds Vchrdy, or if the battery was initially charged above Vchrdy, the circuit goes to NORMAL MODE. STATUS[0] is asserted and the LDOs can be activated by the user thanks to ENLV and ENHV as shown in Figure 10.

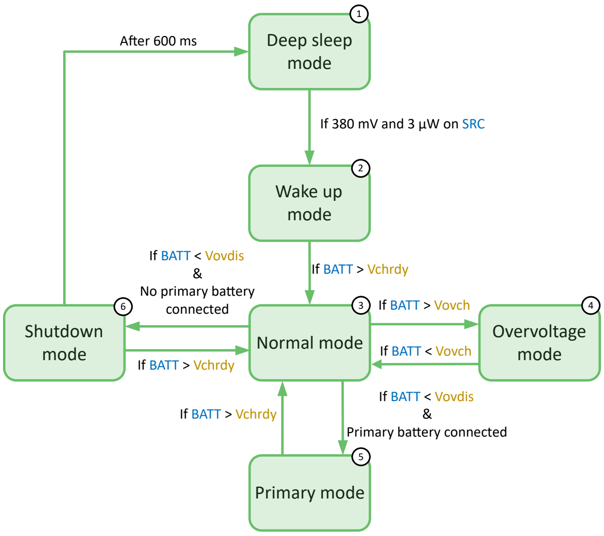


Figure 5: Diagram of the AEM10941 modes

7.2 Normal mode

Once the AEM goes to NORMAL MODE, three scenarios are possible:

- There is enough power provided by the source to maintain Vbatt above Vovdis but Vbatt is below Vovch. In that case, the circuit remains in NORMAL MODE.
- The source provides more power than the load consumes, and Vbatt increases above Vovch, the circuit goes to the OVERVOLTAGE MODE, as explained in the Overvoltage mode section.
- Due to a lack of power from the source, Vbatt falls below Vovdis. In this case, either the circuit goes into the SHUTDOWN MODE as explained in Shutdown mode section or, if a charged primary battery is connected on PRIM, the circuit shifts to PRIMARY MODE as described in the Primary mode section.

Boost

The boost (or step-up) converter raises the voltage available at BUFSRC to a level suitable for charging the storage element, in the range of 2.2 V to 4.5 V, according to the system configuration. This voltage (Vboost) is available at the BOOST pin. The switching transistors of the boost converter are M3 and M4, with the switching node available externally at SWBOOST. The reactive power components of this converter are the external inductor and capacitor LBOOST and CBOOST.

Periodically, the MPP control circuit disconnects the source from the BUFSRC pin with the transistor M1 in order to measure the open-circuit voltage of the harvester on SRC and define the optimal level of voltage. BUFSRC is decoupled by the capacitor CSRC, which smooths the voltage against the current pulses induced by the boost converter.

The storage element is connected to the BATT pin, at a voltage Vbatt. This node is linked to BOOST through the transistor M2. In NORMAL MODE, this transistor effectively shorts the battery to the BOOST node (Vbatt = Vboost). When energy harvesting is occurring, the boost converter delivers a current that is shared between the battery and the loads. M2 is opened to disconnect the storage element when Vbatt reaches Vovdis. However, in such a scenario, the AEM10941 offers the possibility of connecting a primary battery to recharge Vbatt up to the Vchrdy. The transistor M9 connects PRIM to BUFSRC and the transistor M1 is opened to disconnect the SRC input pin as explained in the Primary mode section and shown in Figure 13.

Buck

The buck (or step-down) converter lowers the voltage from Vboost to a constant Vbuck value of 2.2 V. This voltage is available at the BUCK pin. The switching transistors of the buck converter are M5 and M6, with the switching node available externally at SWBUCK. The reactive power components of the buck converter are the external inductor LBUCK and the capacitor CBUCK.

LDO outputs

Two LDOs are available to supply loads at different operating voltages.

Through M7, Vboost supplies the high-voltage LDO that powers its load through HVOUT. This regulator delivers a clean voltage (Vhv) with a maximum current of 80 mA on HVOUT. In the built-in configuration modes, an output voltage of 1.8 V, 2.5 V or 3.3 V can be selected. In the custom configuration mode, it is adjustable between 2.2 V and Vbatt-0.3 V.The high-voltage output can be dynamically enabled or disabled with the logic control pin ENHV. The output is decoupled by the external capacitor CHV.

Through M8, Vbuck supplies the low-voltage LDO that powers its load through LVOUT. This regulator delivers a clean voltage (Vlv) of 1.8 V or 1.2 V with a maximum current of 20 mA on LVOUT. The low-voltage output can be dynamically enabled or disabled with the logic control pin ENLV. The output is decoupled by the external capacitor CLV.

Status pin STATUS[0] alerts the user when the LDOs can be enabled as explained in the Deep sleep & Wake up modes section and in the Shutdown mode section. The table below shows the four possible configurations:

ENLV	ENHV	LV output	HV output
1	1	Enabled	Enabled
1	0	Enabled	Disabled
0	1	Disabled	Enabled
0	0	Disabled	Disabled

Table 6: LDOs configurations

7.3 Overvoltage mode

When Vbatt reaches Vovch, the charge is complete and the internal logic maintains Vbatt around Vovch with a hysteresis of a few mV as shown in Figure 11 to prevent damage to the storage element and to the internal circuitry. In this configuration, the boost converter is periodically activated to maintain Vbatt and the LDOs are still available. Moreover, when the boost converter is not activated, the transistor M1 in Figure 4 is opened to prevent current from the source to the storage element when Vsrc is higher than Vovch.

7.4 Primary mode

When Vbatt drops below Vovdis, the circuit compares the voltage on PRIM with the voltage on FB_PRIM_U to determine whether a charged primary battery is connected on PRIM. The voltage on FB_PRIM_U is set thanks to two optional resistances as explained in the Primary battery configuration section. If the voltage on PRIM divided by 4 is higher than the voltage on FB_PRIM_U, the circuit considers the primary battery as available and the circuit enters PRIMARY MODE as shown in Figure 13.

In that mode, transistor M1 is opened and the primary battery is connected to BUFSRC through transistor M9 in order to become the source of energy for the AEM10941. The chip remains in this mode until Vbatt reaches Vchrdy. When Vbatt reaches Vchrdy, the circuit goes to NORMAL MODE. As long as the chip is in PRIMARY MODE, STATUS[1] is asserted.

If no primary battery is used in the application, PRIM, FB_PRIM_U and FB_PRIM_D must be tied to GND.

In case of the primary mode, it is recommended to use a CSRC capacitor of 150 μF

7.5 Shutdown mode

When Vbatt drops below Vovdis and no power is available from a primary battery, the circuit shifts to SHUTDOWN MODE as shown in Figure 12 to prevent deep discharge potentially leading to damage to the storage element and instability of the LDOs. The circuit asserts STATUS[1] in order to warn the system that a shutdown will occur. Both LDO regulators remain enabled. If no primary battery is used, this allows the load, whether it is powered on LVOUT or HVOUT, to be interrupted by the low-to-high transition of STATUS[1], and to take all appropriate actions before power shutdown.

If energy at the input source is available and Vbatt recovers to Vchrdy within Tcrit ($\sim$ 600 ms), the AEM returns in NORMAL MODE. But if, after Tcrit, Vbatt does not reach Vchrdy, the circuit goes to DEEP SLEEP MODE. The LDOs are deactivated and BATT is disconnected from BOOST to avoid damaging the battery due to the overdischarge. From there, the AEM will have to go through the wake-up procedure described in the Deep sleep & Wake up modes section.

7.6 Maximum power point tracking

During NORMAL MODE, SHUTDOWN MODE and a part of WAKE UP MODE, the boost converter is regulated thanks to an internal MPPT (Maximum Power Point Tracking) module. Vmpp is the voltage level of the MPP and depends on the input power available at the source. The MPPT module evaluates Vmpp as a given fraction of Voc, the open-circuit voltage of the source. By temporarily disconnecting the source from CSRC as shown in Figure 4 for 82 ms, the MPPT module estimates and maintains knowledge of Vmpp. This sampling occurs approximately every 5 s .
With the exception of this sampling process, the voltage across the source, Vsrc, is continuously compared to Vmpp. When Vsrc exceeds Vmpp by a small hysteresis, the boost converter is switched on, extracting electrical charges from the source and lowering its voltage. When Vsrc falls below Vmpp by a small hysteresis, the boost converter is switched off, allowing the harvester to accumulate new electrical charges into CSRC, which restores its voltage. In this manner, the boost converter regulates its input voltage so that the electrical current (or flow of electrical charges) that enters the boost converter yields the best power transfer from the harvester under any ambient conditions. The AEM10941 supports any Vmpp level in the range from 0.05 V to 5 V. It offers a choice of four values for the Vmpp/Voc fraction through configuration pins SELMPP[1:0] as shown in Table 8. The status of the MPPT controller is reported through one dedicated status pin (STATUS[2]). The status pin is asserted when an MPP calculation is being performed.

7.7 Balun for dual-cell supercapacitor

The balun circuit allows users to balance the internal voltage in a dual-cell supercapacitor in order to avoid damaging the super-capacitor because of excessive voltage on one cell. If BAL is connected to GND, the balun circuit is disabled. This configuration must be used if a battery, a capacitor or a single-cell supercapacitor is connected on BATT. If BAL is connected to the node between the cells of a supercapacitor, the balun circuit compensates for any mismatch of the two cells that could lead to overcharge of one of both cells. The balun circuit ensures that BAL remains close to Vbatt/2. This configuration must be used if a dual-cell supercapacitor is connected on BATT.

8 System Configuration

Configuration pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	Vovch	Vchrdy	Vovdis	Vhv	Vlv	
1	1	1	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
1	1	0	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
1	0	1	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
1	0	0	2.70 V	2.30 V	2.20 V	1.8 V	1.2 V	Single-cell supercapacitor
0	1	1	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
0	1	0	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
0	0	1	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
0	0	0	Custom mode - Programmable through R1 to R6				1.8 V	

Table 7: Usage of CFG[2:0]

8.1 Battery and LDOs configuration

Through three configuration pins (CFG[2:0]), the user can set a particular operating mode from a range that covers most application requirements, without any dedicated external component as shown in Table 7. The three threshold levels are defined as:

- Vovch: Maximum voltage accepted on the storage element before disabling the boost converter;
- Vchrdy: Minimum voltage required on the storage element after a cold start before enabling the LDOs;
- Vovdis: Minimum voltage accepted on the storage element before considering the storage element as depleted.

See the Theory of Operation section for more information about the purposes of these thresholds.

The two LDOs output voltages are called Vhv and Vlv for the high and low-output voltages, respectively. In the built-in configuration mode, seven combinations of these voltage levels are hardwired and selectable through the CFG[2:0] configuration pins, covering most application cases. When a predefined configuration is selected, the resistor pins dedicated to a custom configuration should be left floating (SET_OVDIS, SET_CHRDY, SET_OVCH, FB_HV).

A custom mode allows the user to define the Vovch, Vchrdy, Vovdis and Vhv threshold voltages.

Custom mode

When CFG[2:0] are tied to GND, the custom mode is selected and all six configuration resistors shown in Figure 6 must be wired as follows:

Vovch, Vchrdy and Vovdis are defined thanks to R1, R2, R3 and R4. If we define the total resistor (R1 + R2 + R3 + R4) as RT, R1, R2, R3 and R4 are calculated as:

- $1\ \text{M}\Omega \leq \text{RT} \leq 100\ \text{M}\Omega$
- $\text{R1}=\text{RT}(1\ \text{V}/\text{Vovch})$
- $\text{R2}=\text{RT}(1\ \text{V}/\text{Vchrdy} - 1\ \text{V}/\text{Vovch})$
- $\text{R3}=\text{RT}(1\ \text{V}/\text{Vovdis} - 1\ \text{V}/\text{Vchrdy})$
- $\text{R4}=\text{RT}(1 - 1\ \text{V}/\text{Vovdis})$

Vhv is defined thanks to R5 and R6. If we define the total resistor(R5 + R6) as RV, R5 and R6 are calculated as:

- $1\ \text{M}\Omega \leq \text{RV} \leq 40\ \text{M}\Omega$
- $\text{R5}=\text{RV}(1\ \text{V}/\text{Vhv})$
- $\text{R6}=\text{RV}(1 - 1\ \text{V}/\text{Vhv})$

The resistors should have high values to make the additional power consumption negligible. Moreover, the following constraints must be adhered to ensure the functionality of the chip:

- $\text{Vchrdy} + 0.05\ \text{V} \leq \text{Vovch} \leq 4.5\ \text{V}$
- $\text{Vovdis} + 0.05\ \text{V} \leq \text{Vchrdy} \leq \text{Vovch} - 0.05\ \text{V}$
- $2.2\ \text{V} \leq \text{Vovdis}$
- $\text{Vhv} \leq \text{Vovdis} - 0.3\ \text{V}$

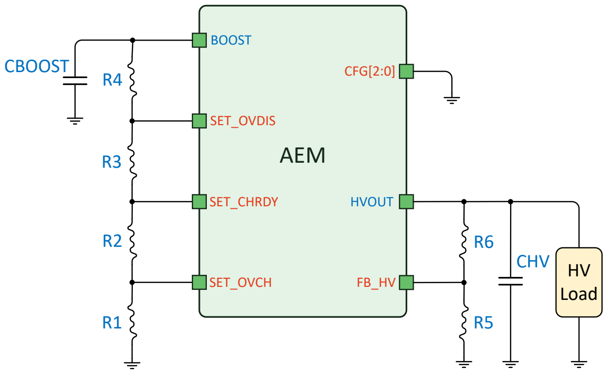


Figure 6: Custom configuration resistors

8.2 MPPT configuration

Two dedicated configuration pins, SELMPP[1:0], allow selecting the MPP tracking ratio based on the characteristic of the input power source.

SELMPP[1]	SELMPP[0]	Vmpp/Voc
0	0	70%
0	1	75%
1	0	85%
1	1	90%

Table 8: Usage of SELMPP[1:0]

8.3 Primary battery configuration

To use the primary battery, it is mandatory to determine Vprim_min, the voltage of the primary battery at which it has to be considered as empty. During the evaluation of Vprim_min, the circuit connects FB_PRIM_D to GND. The circuit uses a resistive divider between BUCK and FB_PRIM_D to define the voltage on FB_PRIM_U as Vprim_min divided by 4. When Vprim_min is not evaluated, FB_PRIM_D is left floating to avoid quiescent current on the resistive divider. If we define the total resistor (R7 + R8) as RP, R7 and R8 are calculated as:

- $100\ \text{k}\Omega \leq \text{RP} \leq 500\ \text{k}\Omega$
- R7= $(\frac{\text{Vprim\_min}}{4} * \text{RP})/2.2\ \text{V}$
- R8=RP-R7

Note that FB_PRIM_U and FB_PRIM_D must be tied to GND if no primary battery is used.

8.4 Cold start configuration

The minimum cold start voltage can be set above the 380 mV thanks to the FB_COLD pin. Use a resistive divider between SRC and GND to set the FB_COLD pin at the required cold start voltage. If we define the total resistor (R9 + R10) as RC and the new cold start voltage as Vcs, R9 and R10 are calculated as:

- $100\ \text{k}\Omega \leq \text{RC} \leq 10\ \text{M}\Omega$
- R9= $\frac{0.38\ V}{\text{Vcs}} * \text{RC}$
- R10=RC-R9

8.5 No battery configuration

If the harvested energy source is permanently available and covers the application purposes or if the application does not need to store energy when the harvested energy source is not available, the storage element may be replaced by an external capacitor CBATT of at least 150 μF.

8.6 Storage element information

The energy storage element of the AEM10941 can be a rechargeable battery, a supercapacitor or a large capacitor (at least 150 μF). It should be chosen so that its voltage does not fall below Vovdis even during occasional peaks of the load current. If the internal resistance of the storage element cannot sustain this voltage limit, it is advisable to buffer the battery with a capacitor.

The BATT pin that connects the storage element must never be left floating. If the application expects a disconnection of the battery (e.g. because of a user removable connector), the PCB should include a capacitor of at least 150 μF. The leakage current of the storage element should be small as leakage currents directly impact the quiescent current of the subsystem.

External inductors information

The AEM10941 operates with two standard miniature inductors of 10 μH. LBOOST and LBUCK must respectively sustain a peak current of at least 250 mA and 50 mA and a switching frequency of at least 10 MHz. Low equivalent series resistance (ESR) favors the power conversion efficiency of the boost and buck converters.

External capacitors information

The AEM10941 operates with four identical standard miniature ceramic capacitors of 10 μF and one miniature ceramic capacitor of 22 μF. The leakage current of the capacitors should be small as leakage currents directly impact the quiescent current of the subsystem.

CSRC

This capacitor acts as an energy buffer at the input of the boost converter. It prevents large voltage fluctuations when the boost converter is switching. The recommended value is 10 μF +/- 20%. If the primary mode is used, the minimum recommended value is 150 μF +/- 20%.

CBUCK

This capacitor acts as an energy buffer for the buck converter. It also reduces the voltage ripple induced by the current pulses inherent to the switched mode of the converter. The recommended value is 10 μF +/- 20%.

CBOOST

This capacitor acts as an energy buffer for the boost converter. It also reduces the voltage ripple induced by the current pulses inherent to the switched mode of the converter. The recommended value is 22 μF +/- 20%.

CHV and CLV

These capacitors ensure a high-efficiency load regulation of the high-voltage and low-voltage LDO regulators. Closed-loop stability requires the value to be in the range of 8 μF to 14 μF.

9 Typical Application Circuits

9.1 Example: Circuit 1

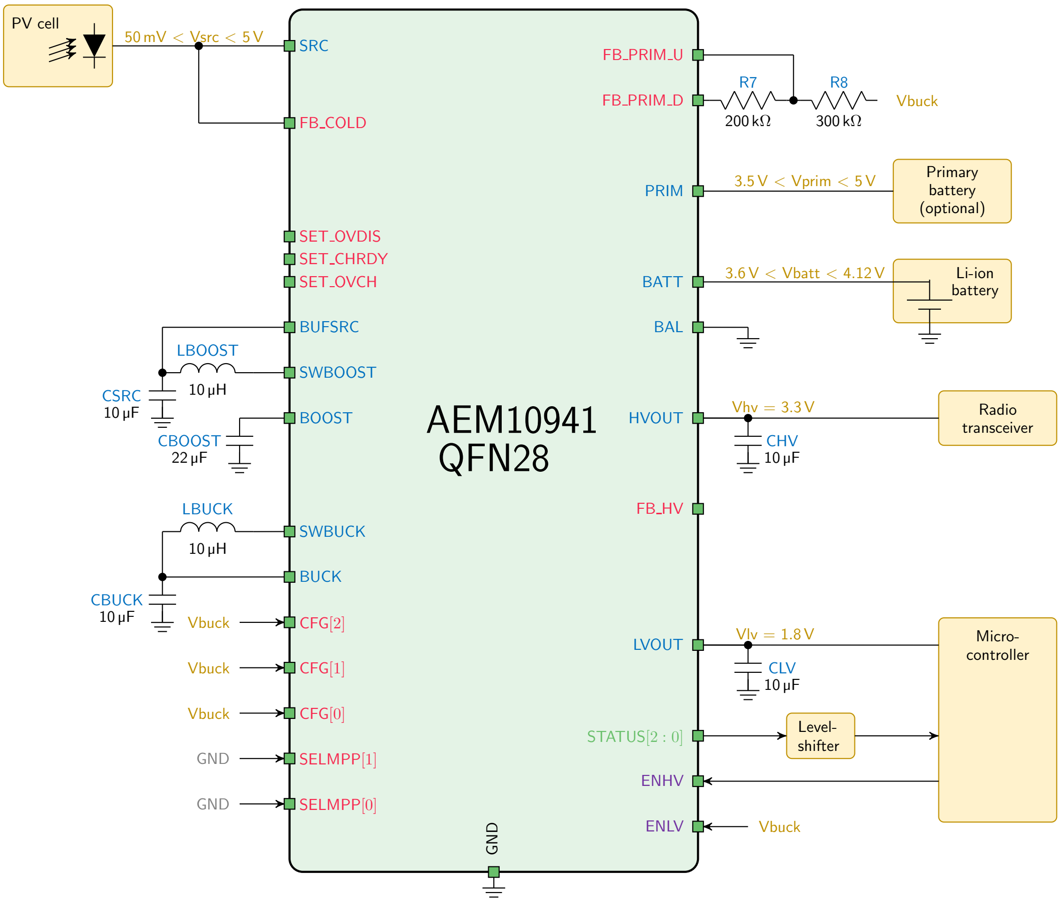


Figure 7: Typical application circuit 1

The energy source is a photovoltaic cell, and the storage element is a standard Li-ion battery cell. The radio communication makes use of a transceiver that operates from a 3.3 V supply. A microcontroller supplied by a 1.8 V supply controls the application.

This circuit uses a pre-defined operating mode, typical of systems that use standard components for radio and energy storage.

The operating mode pins are connected to:

- CFG[2:0] = 111

Referring to Table 7, in this mode, the threshold voltages are:

- Vovch = 4.12 V
- Vchrdy = 3.67 V
- Vovdis = 3.60 V

Moreover, the LDOs output voltages are:

- Vhv = 3.3 V
- Vlv = 1.8 V

A primary battery is also connected as a back-up solution. The minimal level allowed on this battery is set at 3.5 V. Following equations on page 12:

- RP = 0.5 MΩ
- R7 = $(\frac{3.5\ \text{V}}{4}*0.5\ \text{M}\Omega)/2.2\ \text{V} = 200\ \text{k}\Omega$
- R8 = 0.5 MΩ-200 kΩ = 300 kΩ

The MPP configuration pins SELMPP[1:0] are tied to GND (logic low), selecting an MPP ratio of 70%, suitable for the particular PV cell in use.

The ENLV enable pin for the low-voltage LDO is tied to BUCK. The microcontroller will be enabled when Vbatt and Vboost exceed Vchrdy as the low-voltage regulator supplies it.

The application software can enable or disable the radio transceiver with a GPIO connected to ENHV.

9.2 Example: Circuit 2

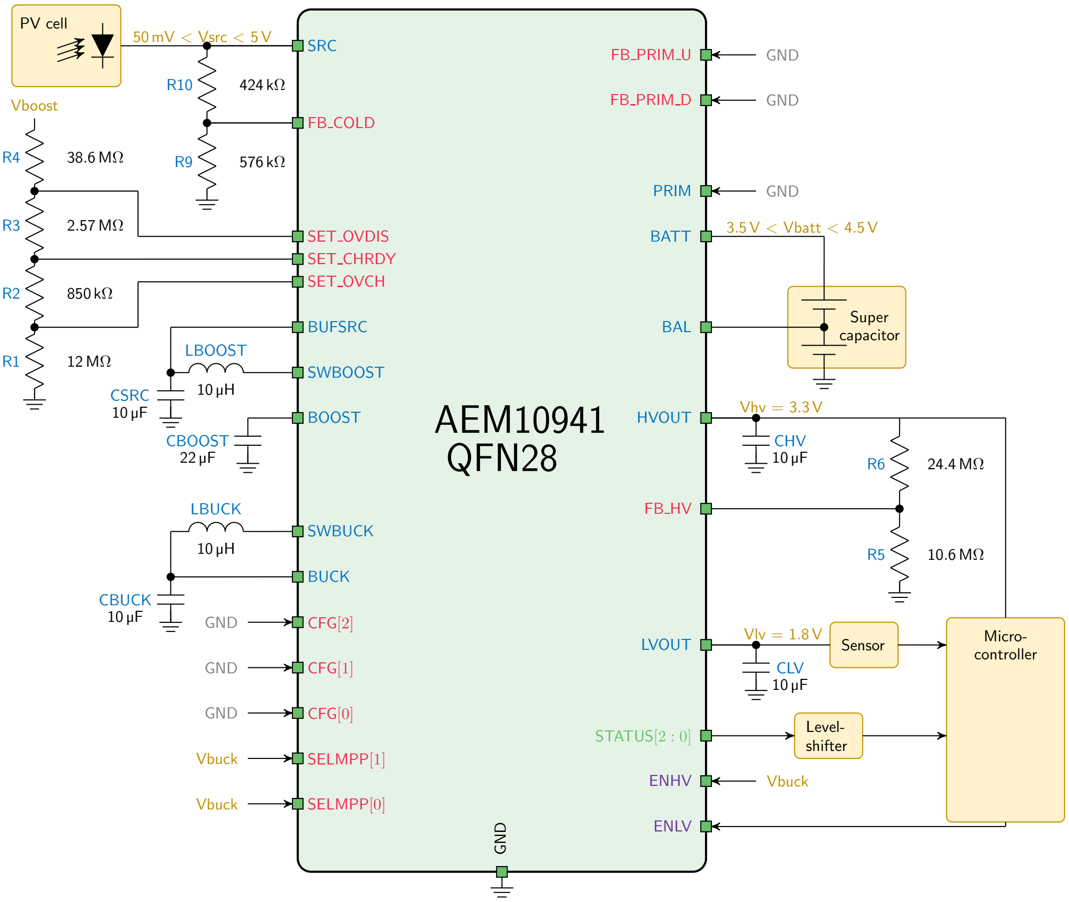


Figure 8: Typical application circuit 2

The energy source is a photovoltaic cell, and the storage element is a dual-cell supercapacitor. The supercapacitor can be completely depleted during the cold start.

Moreover, BAL is connected to the dual-cell supercapacitor to compensate for any mismatch between the two cells and in that way to protect the supercapacitor.

A microcontroller pilots and collects information from a sensor. The operating mode pins are connected to:

- CFG[2:0] = 000

The user wants a custom configuration with Vovch, Vchrdy and Vovdis at 4.5 V, 4.2 V and 3.5 V, respectively. The user choose 54 MΩ for RT. Following the equation in page 11:

- R1 = 54 MΩ$(\frac{1\ V}{4.5\ V})$ =1 2 MΩ
- R2 = 54 MΩ$(\frac{1\ V}{4.2\ V}$-$\frac{1\ V}{4.5\ V})$ = 850 kΩ
- R3 = 54 MΩ$(\frac{1\ V}{3.5\ V}$-$\frac{1\ V}{4.2\ V})$ = 2.57 MΩ
- R4 = 54 MΩ(1-$\frac{1\ V}{3.5\ V}$) = 38.6 MΩ

In the custom mode, the Vlv equals 1.8 V and the application software can enable or disable the sensor with a GPIO connected to ENLV.

On Vhv, the user wants a 3.3 V voltage. As shown in page 11, the user chooses a resistor RV equal to 35 MΩ

- R5 = 35 MΩ$(\frac{1\ V}{3.3\ V})$ = 10.6 MΩ
- R6 = 35 MΩ(1-$\frac{1\ V}{3.3\ V}$) = 24.4 MΩ

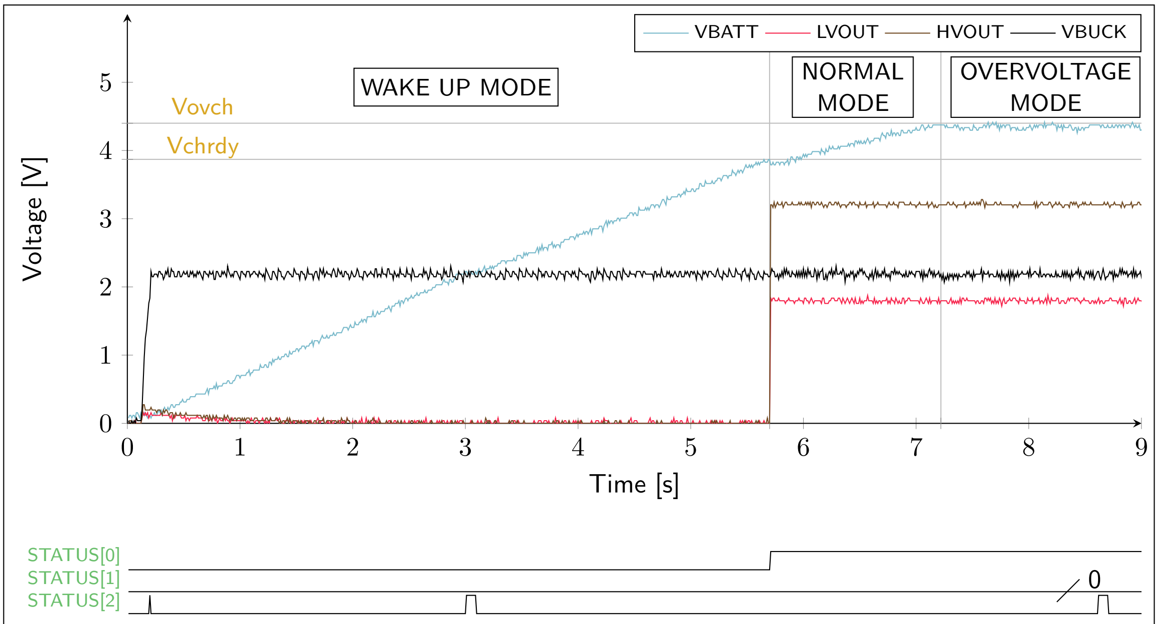
The ENHV enable pin for the high-voltage LDO is tied to BUCK. The microcontroller is enabled when Vbatt and Vboost exceed Vchrdy as the high-voltage regulator supplies it.

The MPP configuration pins SELMPP[1:0] are tied to BUCK (logic high), selecting an MPP ratio of 90%, suitable for the particular PV cell in use.

No primary battery is connected and the PRIM, FB_PRIM_U and FB_PRIM_D pins are tied to GND.

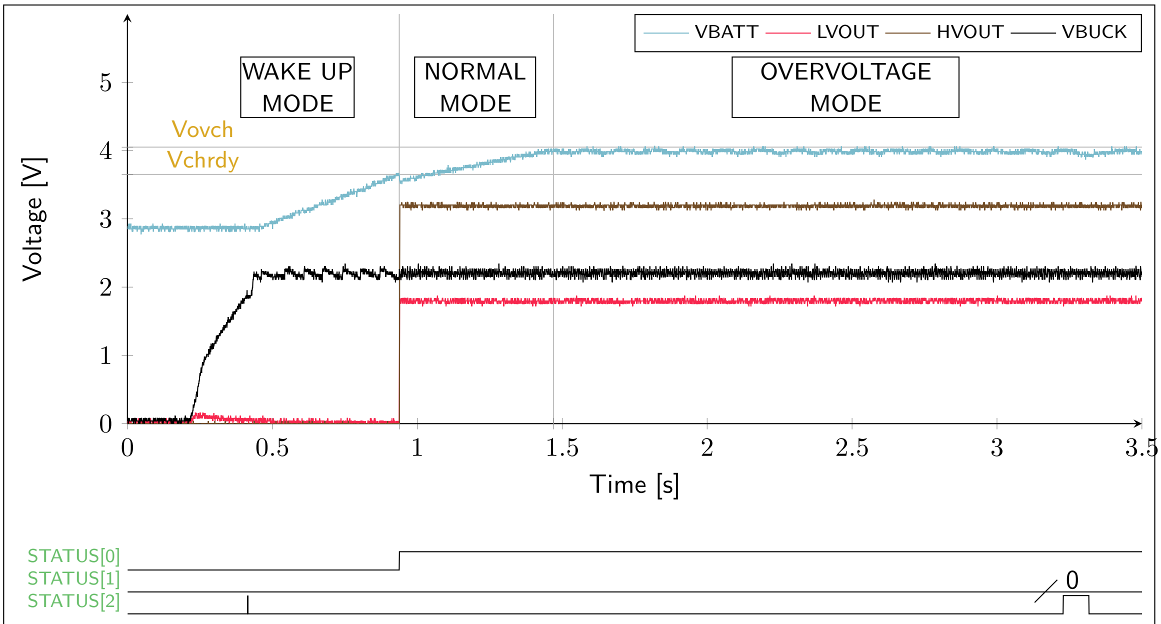
The cold start voltage is set at 700 mV instead of the 380 mV defined by default. The total resistor RC is set at 1 MΩ.

- R9 = 1 MΩ $\frac{0.4\ V}{0.7\ V}$ = 576 kΩ
- R10 = 424 kΩ



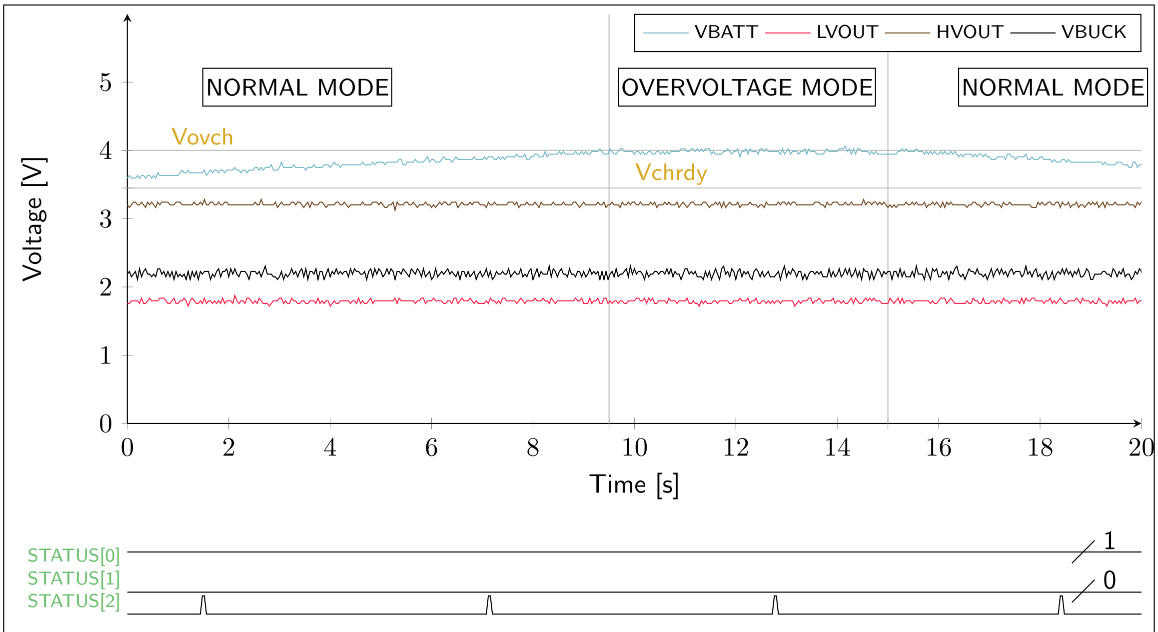
CFG[2:0] = 3'b010, SELMPP[1:0] = 2'b00, Storage element: capacitor (480 µF), SRC: current source (2 mA) with voltage compliance (1 V), ENLV = 1'b1, ENHV = 1'b1, LVOUT load = 100 kΩ, HVOUT load = 100 kΩ.

Figure 9: Cold start with a capacitor connected to BATT



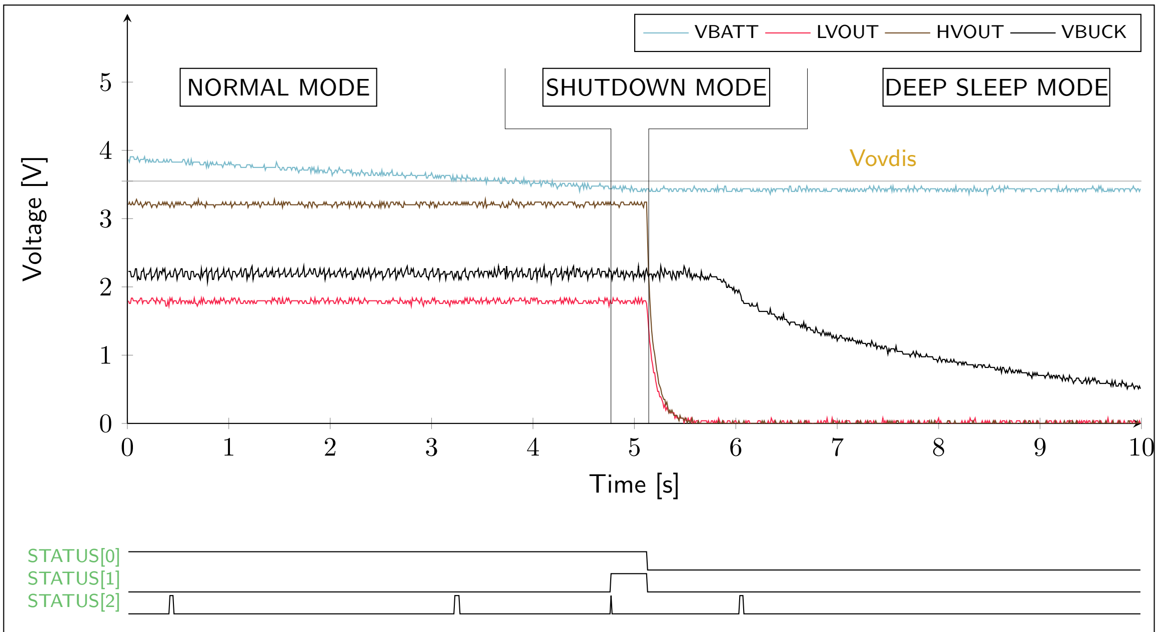
CFG[2:0] = 3'b111, SELMPP[1:0] = 2'b00, Storage element: capacitor (450 µF) pre-charged at 3 V, SRC: current source (1 mA) with voltage compliance (3 V), ENLV = 1'b1, ENHV = 1'b1, LVOUT load = 22 kΩ, HVOUT load = 22 kΩ.

Figure 10: Cold start with a battery connected to BATT



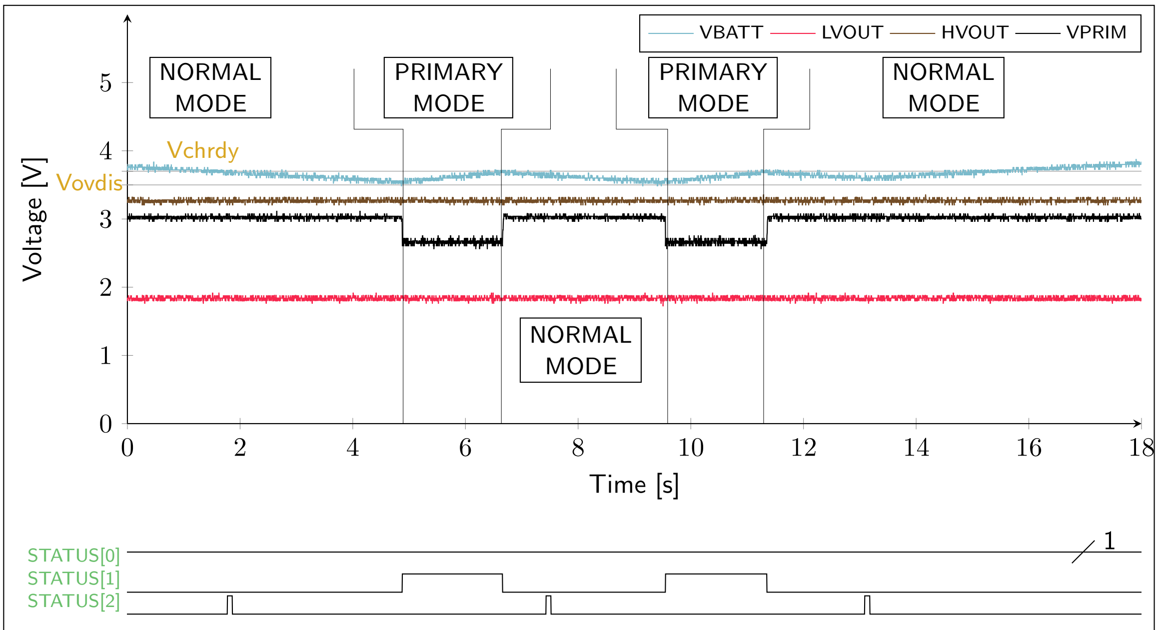
CFG[2:0] = 3'b111, SELMPP[1:0] = 2'b00, Storage element: capacitor (4.85 mF), SRC: current source (1 mA) with voltage compliance (3 V), ENLV = 1'b1, ENHV = 1'b1, LVOUT load = 22 kΩ, HVOUT load = 22 kΩ.

Figure 11: Overvoltage mode



CFG[2:0] = 3'b010, SELMPP[1:0] = 2'b00, Storage element: capacitor (4.85 mF), SRC: current source (2 mA) with voltage compliance (1 V), ENLV = 1'b1, ENHV = 1'b1, LVOUT load = 22 kΩ, HVOUT load = 22 kΩ.

Figure 12: Shutdown mode (without primary battery)



CFG[2:0] = 3'b111, SELMPP[1:0] = 2'b00, Storage element: capacitor (4.85 mF), SRC: current source (1 mA) with voltage compliance (3 V), ENLV = 1'b1, ENHV = 1'b1, LVOUT load = 22 kΩ, HVOUT load = 22 kΩ, PRIM: voltage source (3 V) with current compliance (1 mA). R7 = 68 kΩ, R8 = 330 kΩ.

Figure 13: Switch to primary battery if the battery is overdischarged

10 Performance Data

10.1 BOOST conversion efficiency 10 uH

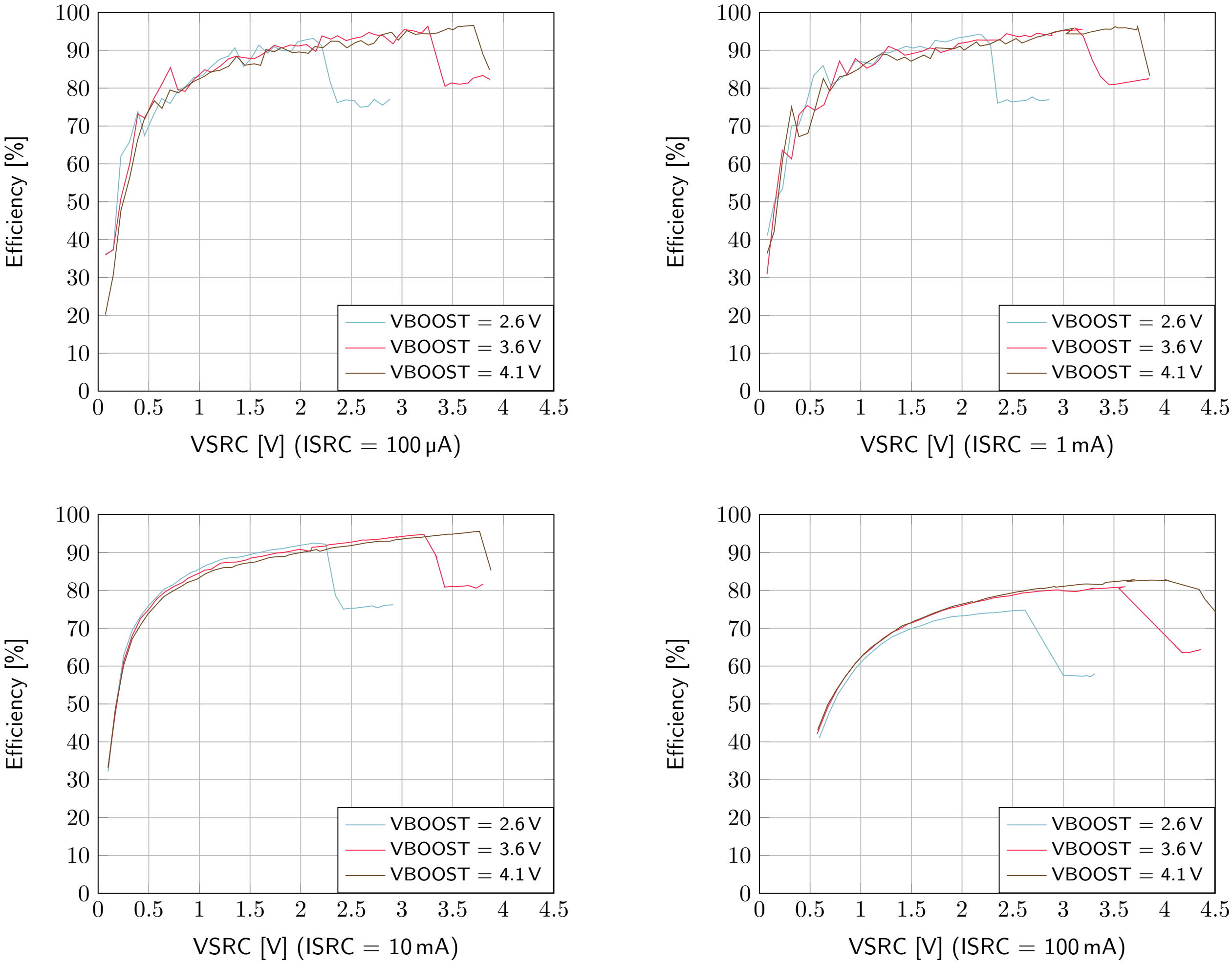


Figure 14: Boost efficiency for Isrc at 100 µA, 1 mA, 10 mA and 100 mA with Lboost = 10 µH

10.2 BOOST conversion efficiency with 22 uH

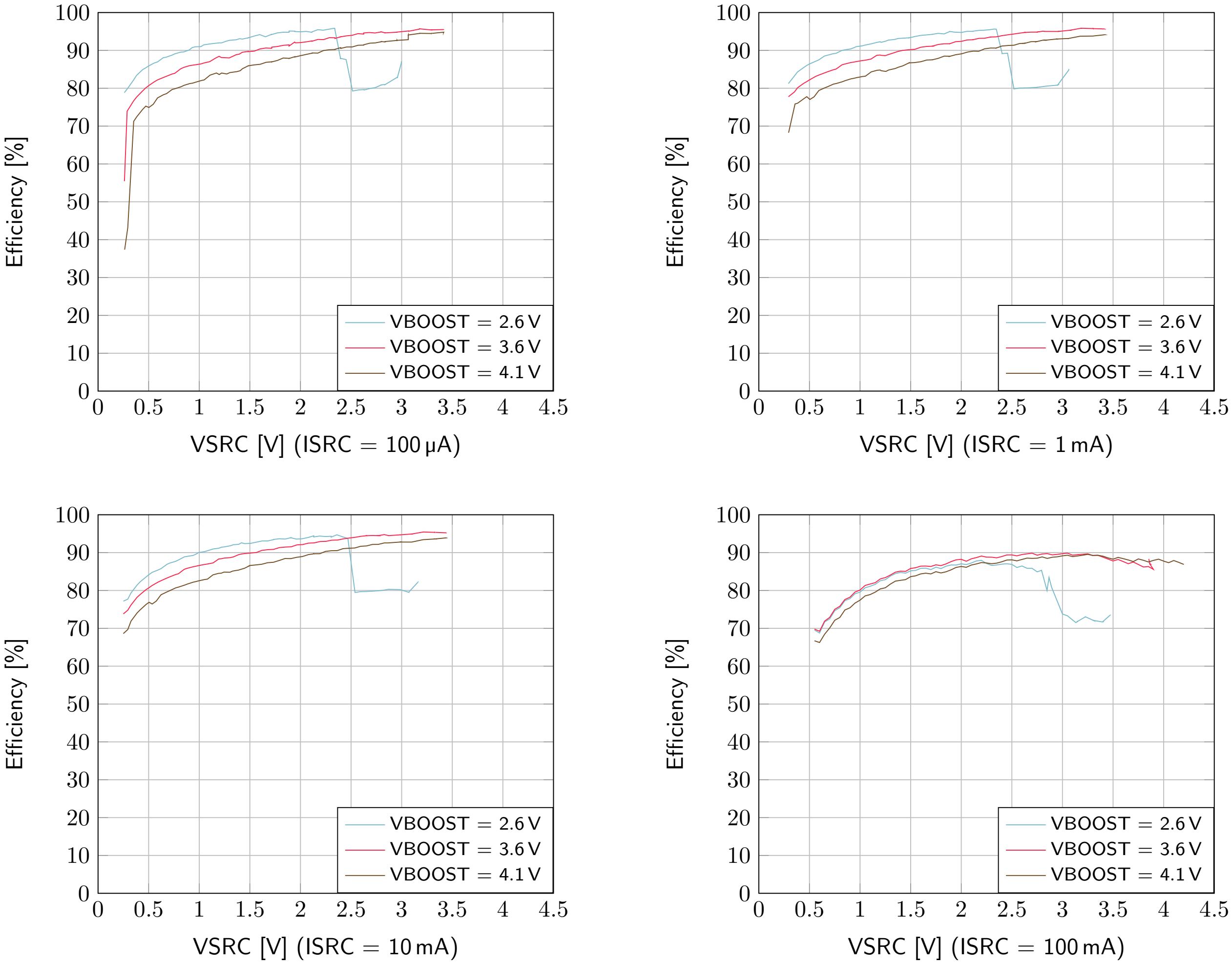


Figure 15: Boost efficiency for Isrc at 100 μA, 1 mA, 10 mA and 100 mA with Lboost = 22 µH

For application with low voltage source, it is more efficient to use a 22 μH for the LBOOST

10.3 Quiescent current

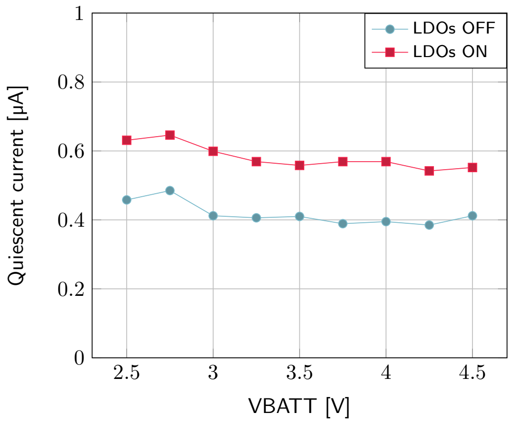


Figure 16: Quiescent current with LDOs on and off

10.4 High-voltage LDO regulation

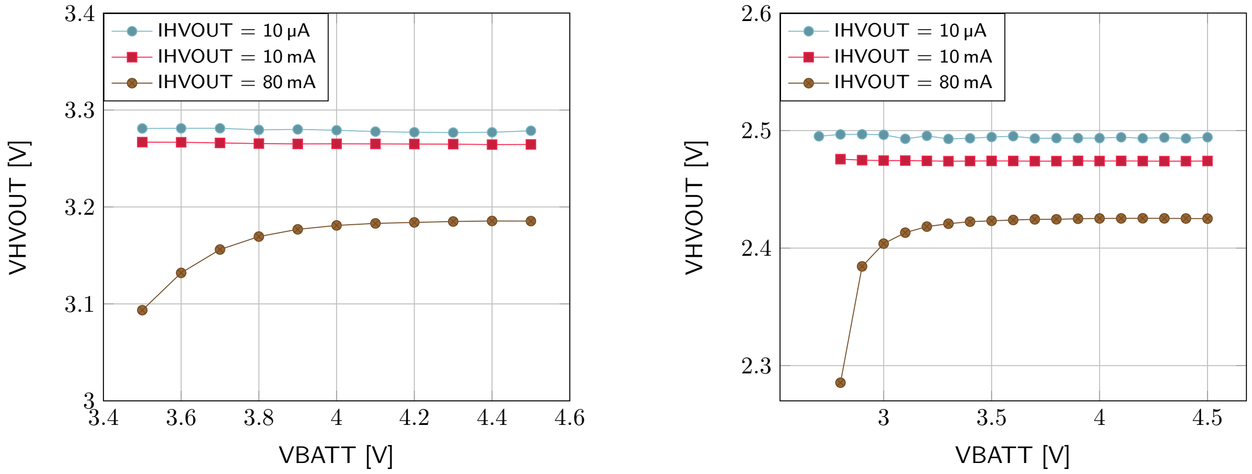


Figure 17: HVOUT at 3.3 V and 2.5 V

10.5 Low-voltage LDO regulation

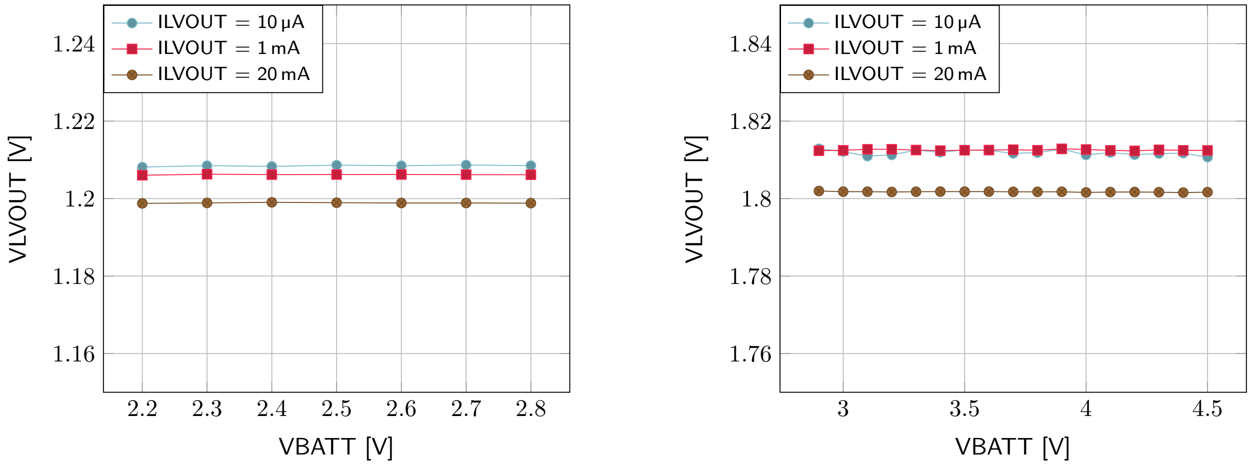


Figure 18: LVOUT at 1.2 V and 1.8 V

10.6 High-voltage LDO efficiency

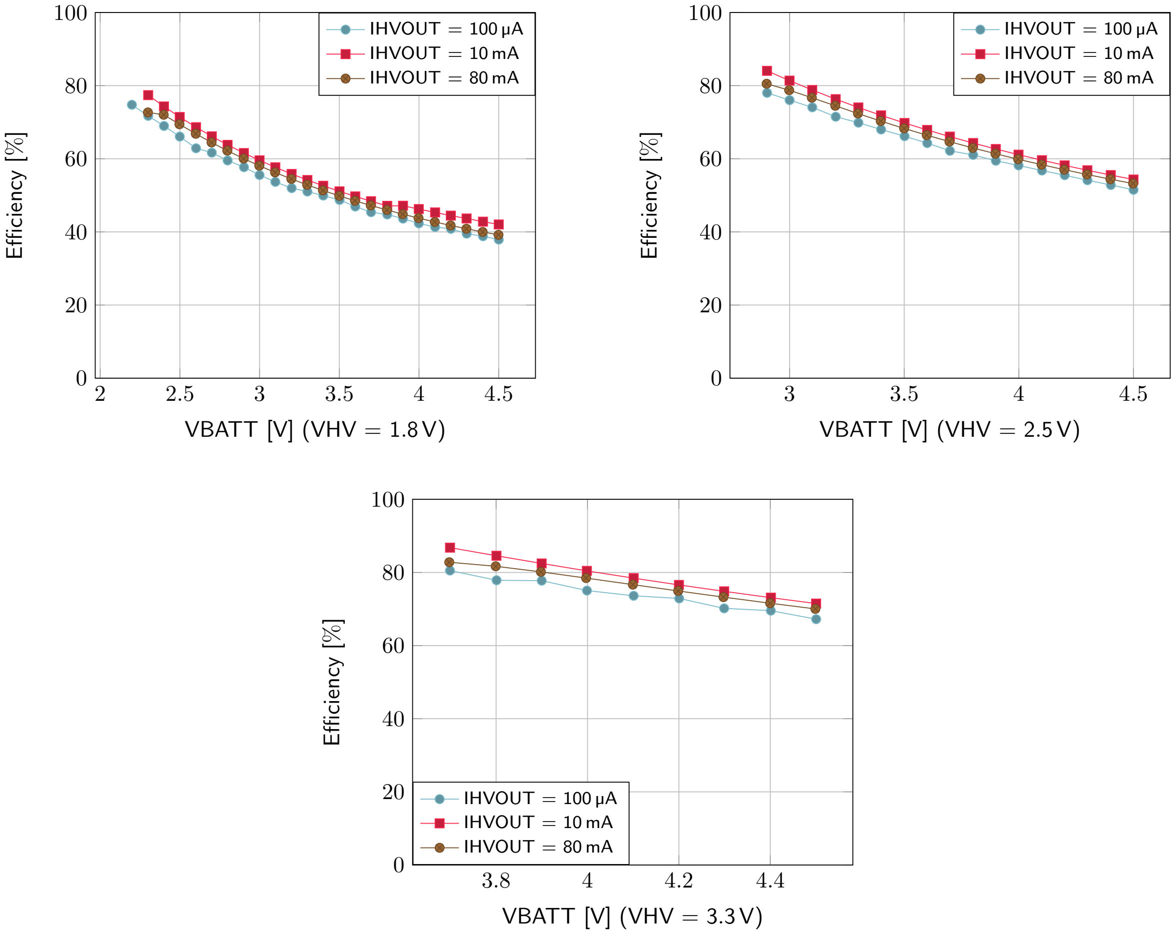


Figure 19: HVOUT efficiency at 1.8 V, 2.5 V and 3.3 V

The theoretical efficiency of a LDO can be simply calculated as $\frac{\text{Vout}}{\text{Vin}}$ if quiescent current can be neglected with regards to the output current. In the case of the high-voltage LDO, the theoretical efficiency is equal to $\frac{\text{Vhv}}{\text{Vbatt}}$.

10.7 Low-voltage LDO efficiency

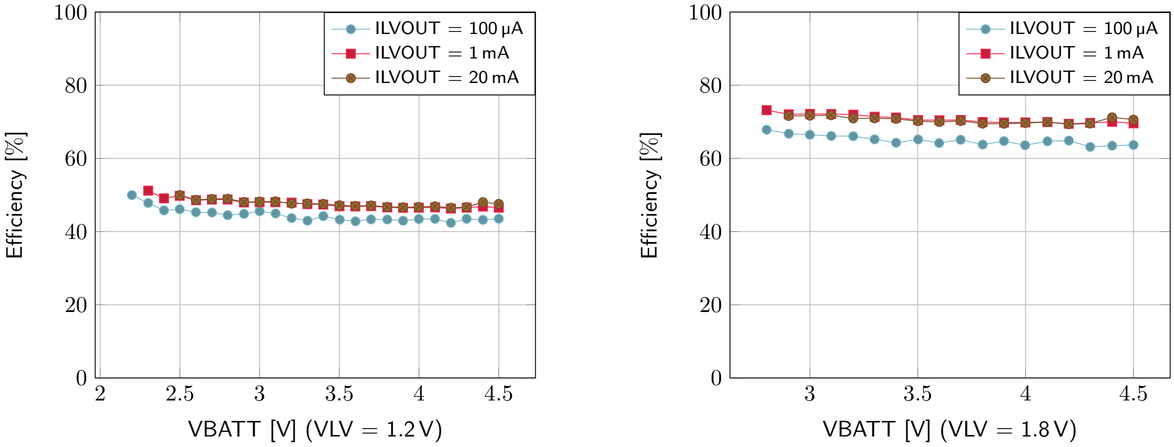


Figure 20: Efficiency of BUCK cascaded with LVOUT at 1.2 V and 1.8 V

The theoretical efficiency of the low-voltage LDO is equal to $\frac{\text{Vlv}}{\text{Vbuck}}$. Starting from the battery, the efficiency of the buck converter has to be taken into account (see Figure 4). The efficiency between Vbatt and Vlv is therefore equal to $\eta_{\text{buck}}\frac{\text{Vlv}}{\text{Vbuck}}$.

11 Schematic

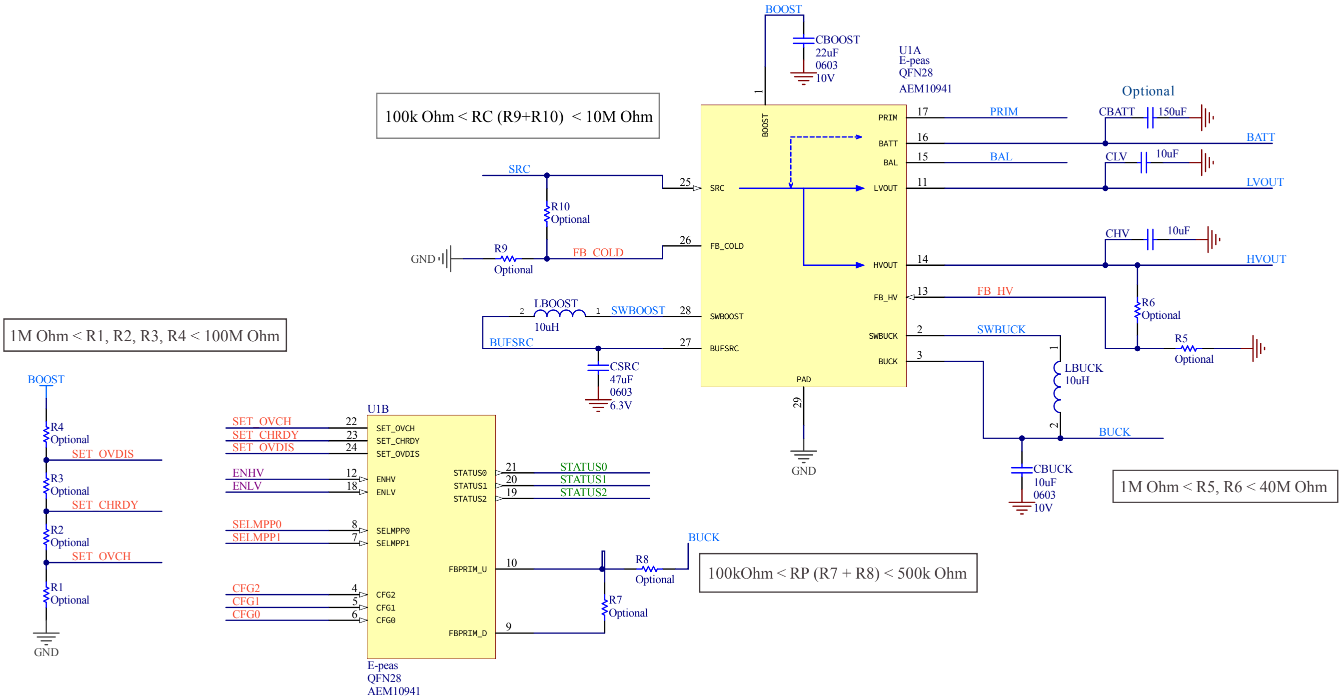


Figure 21: Schematic example

Designator	Description	Quantity	Manufacturer	Part Number
CBOOST	Ceramic Cap 22 μF, 10 V, 20%, X5R 0603	1	Murata	GRM188R61A226ME15D
CBUCK	Ceramic Cap 10 μF, 10 V, 20%, X5R	1	TDK	C1608X5R1A106M080AC
CHV	Ceramic Cap 10 μF, 10 V, 20%, X5R	1	TDK	C1608X5R1A106M080AC
CLV	Ceramic Cap 10 μF, 10 V, 20%, X5R	1	TDK	C1608X5R1A106M080AC
CSRC	Ceramic Cap 10 μF, 10 V, 20%, X5R	1	TDK	C1608X5R1A106M080AC
LBOOST	Power Inductor 10 μH - 0,54 A - LPS4012	1	Coilcraft	LPS4012-103MR
	Power Inductor 10 μH - 0,8 A - 3015	1	Würth	744 040 321 00
LBUCK	Power Inductor 10 μH - 0,25 A	1	TDK	MLZ1608M100WT
U1	AEM10941 - Symbol QFN28	1		order at sales@e-peas.com or Where to buy

Table 9: BOM example for AEM10941 and its required passive components

12 Layout

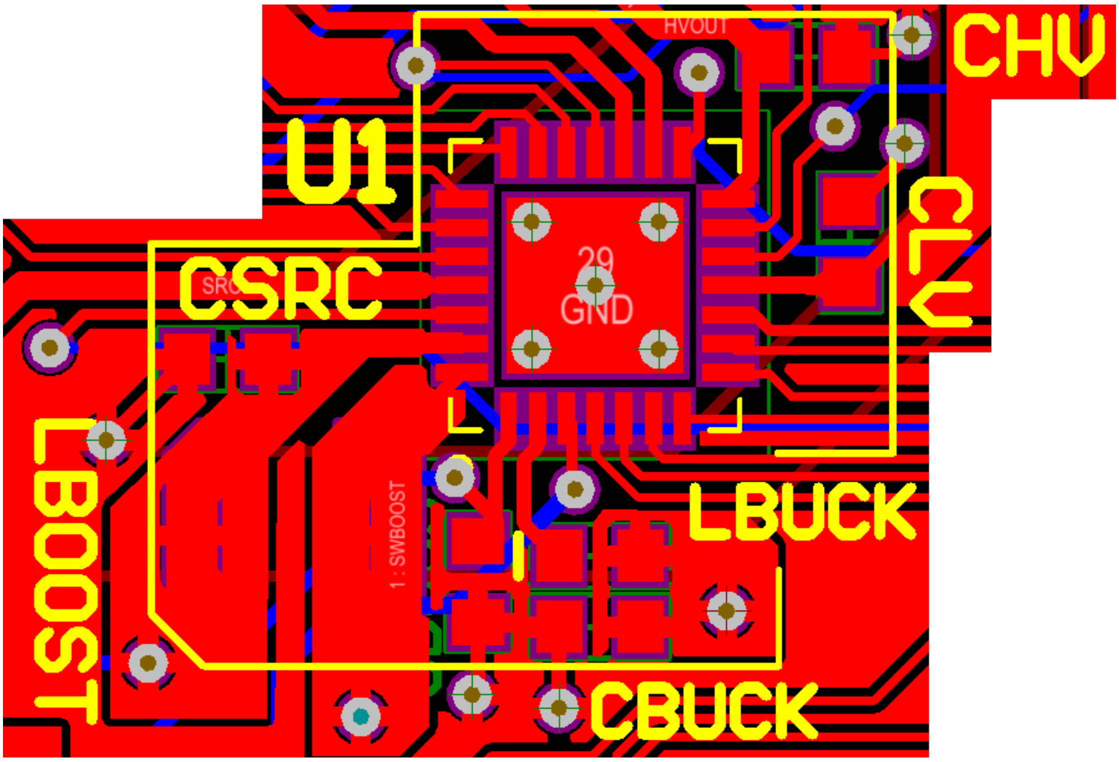


Figure 22: Layout example for the AEM10941 and its passive components

Note: Schematic, symbol and footprint for the e-peas component can be ordered by contacting the e-peas support team: support@e-peas.com

13 Package Information

13.1 Plastic quad flatpack no-lead (QFN28 5mm x 5mm)

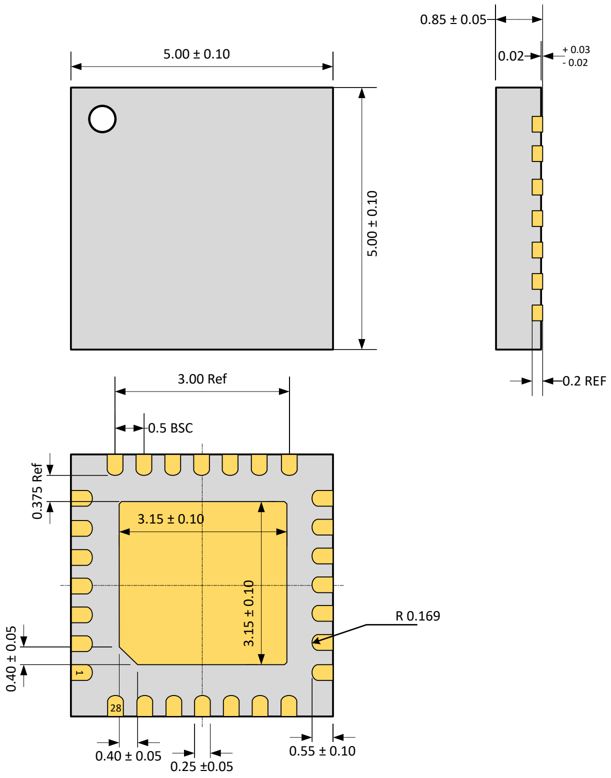


Figure 23: QFN28 5mm x 5mm

13.2 Board layout

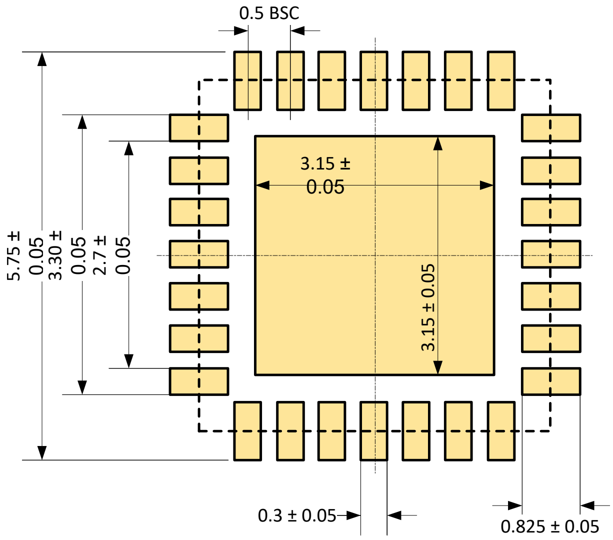


Figure 24: Board layout

Revision History

Revision	Date	Description
1.0	July, 2018	Creation of the document.
1.3	June, 2019	- p21, 22 → Updated efficiencies measurements; - p5 → ESD specifications; - p3 → HVOUT voltage on Figure 1 ~~4.2V~~ → 4.1V.
1.4	November, 2020	- p5 → Ading current from the Prim battery and the maximum current on SRC - p14 → Minor modification on figure 8 (SET_OVDIS switch with SET_OVCH) - p15 → Modification on figure 10 (Position of Vchrdy and Vovch) - p14 → Figure 8: BATT Pin (~~3.6V~~3.5V and ~~4.12V~~ 4.5V) - p14 → Figure 8: Inversion between ENHV and ENLV - p6 → Suppression of STONBATT - p5 → Adding ESD qualification - All → ~~Cold-start~~ ~~Coldstart~~ → Cold start