

LOW-JITTER SAW OSCILLATOR (SPSO)

OUTPUT: LV-PECL, LVDS, HCSL



•Frequency range
•Supply voltage

•Supply voltage

•Output
•Function
•External dimensions

: 53.125 MHz to 700 MHz
2.5 V ... EG-2121CA
3.3 V ... EG-2102CA

• UV-PECL or LVDS or HCSL
• Output enable (OE)
7.0 × 5.0 × 1.2 mm

Very low jitter and low phase noise by SAW unit.





Product Number

EG-2121CA: Q3805CAx0xxxx00 : X1M000101xxxx00

EG-2102CA: Q3806CA00xxxx00 : X1M000091xxxx00





Specifications (characteristics)

▶ Differential LV-PECL Output

Item	Symbol	EG-2121CA	EG-2102CA	Conditions	/ Demarks
item	Symbol	LV-PECL		Conditions / Remarks	
Output frequency range	fo	53.125 MHz to 500 MHz	100 MHz to 700 MHz	Please contact us about available frequencies.	
Supply voltage	Vcc	2.5 V ± 0.125 V	3.3 V ± 0.3 V		
Storage temperature	T_stg	-40 C to +100 C		Storage as single product.	
Operating temperature	T_use	P: 0 C to +70 C, R: -5 C to	+85 C, S: -20 C to +70 C		
Frequency tolerance	f_tol	G: ± 50 × 10 ⁻⁶ ,	H: ±100 × 10 ⁻⁶		
Current consumption	lcc	80 mA Max.	100 mA Max.	OE=V _{CC} , L ECL=50 Ω	
Disable current	I_dis	20 mA Max.	32 mA Max	OE=GND	
Symmetry	SYM	P:40 % to 60 % (fo > 350 MHz) P:45 % to 55 % (fo ≤ 350 MHz)	P:45 % to 55 %	at outputs crossing point	
		D:48 % to 52 % (fo ≤ 175 MHz)	D:48 % to 52 % (fo ≤ 350 MHz)		
	Voн	1.55 V Typ.	2.35 V Typ.		
Output voltage	VOH	V _{CC} -1.025 V to V _{CC} -0.88 V		DC characteristics	
ouput rollago	Vol	0.8 V Typ. Vcc-1 81 V t	1.6 V Typ. o Vcc-1.62 V		
Output load condition (ECL)	L ECL	50 Ω		Terminated to V _{CC} -2.0 V	
Input voltage	V _{IH} V _{IL}	70 % V _{CC} Min. 30 % V _{CC} Max.		OE terminal	
Rise time / Fall time	tr / tf	400 ps Max.		Between 20 % and 80 % of	(Voh-Vol)
Start-up time	t str			Time at minimum supply vol	tage to be 0 s
Phase Jitter		0.8 ps Max.		fo < 100 MHz	0
	tы	0.5 ps Max.		100 MHz ≤ fo < 200 MHz Offset frequency: 12 f	Offset frequency: 12 kHz to
		0.3 ps Max.		200 MHz ≤ fo	ZU MITZ
Frequency aging	f_aging	± 10 × 10 ⁻⁶ / year Max.		+25 C, First year, Vcc=2.5	V, 3.3 V

►LVDS Output

H	Or male at	EG-2121CA	EG-2102CA	04:4:	/ Damada
Item Symt		LVDS		Conditions / Remarks	
Output frequency range	fo	53.125 MHz to 700 MHz		Please contact us about available frequencies.	
Supply voltage	Vcc	2.5 V ± 0.125 V	3.3 V ± 0.3 V	•	
Storage temperature	T stg	-40 C to +100 C Storage as single product.			
Operating temperature	T use	P: 0 C to +70 C, R: -5 C to	+85 C, S: -20 C to +70 C		
Frequency tolerance	f_tol	G: ± 50 × 10 ⁻⁶ ,	H: ±100 × 10 ⁻⁶		
Current consumption	lcc	30 mA Max	45 mA Max.	OE=V _{CC} , L LVDS= 100 Ω	
Disable current	I_dis	20 mA Max	30 mA Max.	OE=GND	
Symmetry	SYM	L:40 % to 60 % (fo > 350 MHz) L:45 % to 55 % (fo ≤ 350 MHz) V:48 % to 52 % (fo ≤ 175 MHz)	L:40 % to 60 % (fo > 350 MHz) L:45 % to 55 % (fo ≤ 350 MHz) V:48 % to 52 % (fo ≤ 175 MHz)	at outputs crossing point	
	Vop		7 mV to 454 mV	V _{OD1} , V _{OD2}	
	dVon	-		dV _{OD} = V _{OD1} -V _{OD2}	1
Output voltage	Vos			Vost, Vos2	DC characteristics
	dVos	150 mV Max.		dVos = Vos1-Vos2	1
Output load condition (LVDS)	L_LVDS			Connected between OUT to	о оот
Input voltage	V _{IH} V _{IL}	70 % V _{CC} Min. 30 % V _{CC} Max.		OE terminal	
Rise time / Fall time	tr/tr			Between 20 % and 80 % of Peak voltage	f Differential Output Peak to
Start-up time	t_str	10 ms Max.		Time at minimum supply vo	Itage to be 0 s
Phase Jitter	tpJ	0.8 ps Max.		fo < 100 MHz	Offset frequency: 12 kHz to
		0.5 ps Max.		100 MHZ ≤ 10 < 200 MHZ 20 MHz	
		0.3 ps Max.		200 MHz ≤ fo	
Frequency aging	f aging	± 10 × 10 ⁻⁶ / year Max.		+25 C, First year, V _{CC} =2.5 V, 3.3 V	



► HCSL Output

Itom	Symbol	EG-2121CA	EG-2102CA	Conditions	/ Demarks
Item		HCSL		Conditions / Remarks	
Output frequency range	fo	100 MHz to 350 MHz		Please contact us about available frequencies.	
Supply voltage	Vcc	2.5 V ± 0.125 V 3.3 V ± 0.3 V			
Storage temperature	T_stg	-40 C to	+125 C	Storage as single product.	
Operating temperature	T_use	P: 0 C to +70 C, R: -5 C to	+85 C, S: -20 C to +70 C		
Frequency tolerance	f_tol	G: ± 50 × 10 ⁻⁶ , H: ±100 × 10 ⁻⁶			
Current consumption	Icc	80 mA Max. 85 mA Max. O		OE=V _{CC} , L HCSL=50 Ω	
Disable current	I_dis	20 mA Max.	35 mA Max	OE=GND	
Symmetry	SYM	45 % to 55 %		at outputs crossing point	
Output Voltage	Voн	0.75 V Typ.		DC characteristics	
	VoL	-0.3 V Typ.			
Output load condition (HCSL)	L HCSL	50 Ω		Terminated to GND	
Input voltage	VIH	70 % V _{CC} Min.		OE terminal	
. •	V _{IL}	30 % V _{CC} Max.			
Rise time / Fall time	tr/tf	500 ps Max.		Between 0.175 V and 0.525	
Start-up time	t str	10 ms Max.		Time at minimum supply vol	tage to be 0 s
		0.8 ps Max.		fo < 100 MHz	Offset frequency: 12 kHz to
Phase Jitter	tej	0.5 ps Max.		100 MHz ≤ fo < 200 MHz	20 MHz
		0.3 ps Max.		200 MHz ≤ fo	ZU IVII IZ
Frequency aging *2	f_aging	± 10 × 10 ⁻⁶ / year Max.		+25 C, First year, Vcc=2.5	/, 3.3 V

Product Name (Standard form) EG-2121 CA 250.000000MHz P G P A 3

②Package type ③Frequency ①Model

- 4)Output/Symmetry ⑤Frequency tolerance ⑥Operating temperature
 - Trequency aging (A*1: Frequency tolerance include aging, N*2: Frequency tolerance exclude aging)
 - *1 This includes initial frequency tolerance, temperature variation, supply voltage change, reflow drift, and aging(+25 C,10 years).
 - *2 This includes initial frequency tolerance, temperature variation, supply voltage change, and reflow drift(except aging).
 - (567: GRA, GSA are not available)

(⑤⑥: As for LV-PECL and LVDS output, for 53.125 MHz ≤ fo < 100 MHz only HP is available)

4	Output	Symmetry		
Symbol	Output	EG-2121CA	EG-2102CA	
Р	LV-PECL	40 % to 60 %(fo > 350 MHz) 45 % to 55 %(fo ≤ 350 MHz) 45 % to 55 %		
D	LV-PECL	48 % to 52 %(fo≤ 175 MHz)	48 % to 52 %(fo ≤ 350 MHz)	
L	LVDS	40 % to 60 %(fo > 350 MHz) 45 % to 55 %(fo ≤ 350 MHz)		
V	LVDS	48 % to 52 %(fo ≤ 175 MHz)		
Н	HCSL	45 % to 55 %		

⑤Frequency tolerance			
G	±50 × 10 ⁻⁶		
H ±100 × 10 ⁻⁸			

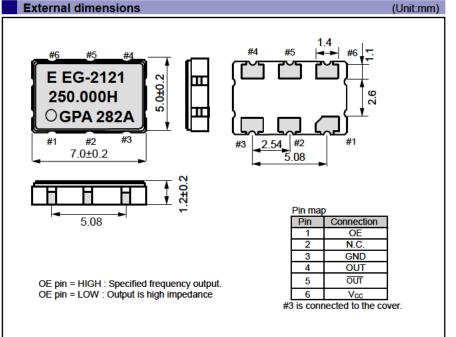
⑥Operating temperature				
Р	0 °C to +70 °C			
R	-5 °C to +85 °C			
S	-20 °C to +70 °C			

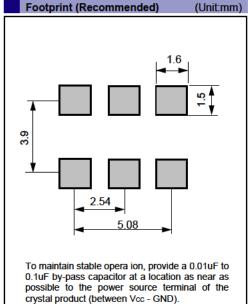
Table 2 Jitter

Item	Symbol	Specifications	Remarks
	tฌ	0.2 ps Typ.	Deterministic Jitter
	t _{RJ}	3 ps Typ.	Random Jitter
Jitter *	t _{RMS}	3 ps Typ.	σ (RMS of total distribution)
	t _{p-p}	25 ps Typ.	Peak to Peak
	t _{acc}	4 ps Typ.	Accumulated Jitter(σ) n=2 to 50 000 cycles

- * Tested using a DTS-2075 Digital iming system made by WAVECREST with jitter analysis software VISI6.
- * Based on SIA-3100C signal integrity analyzer made from WAVECREST.

- Differential LV-PECL, LVDS output
- HCSL output





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► Complies with EU RoHS directive.

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Contains Pb in products exempted by EU RoHS directive.





▶ Designed for automotive applications such as Car Multimedia, Body Electronics, Remote Keyless Entry etc.



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