EPSON
EXCEED YOUR VISION

S1D13743 Mobile Graphics Engine

Hardware Functional Specification

Document Number: X70A-A-001-02

Status: Revision 2.7

Issue Date: 2010/05/18

Table of Contents

1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13743 Embedded Memory LCD Controller. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This document is updated as appropriate. Please check the Epson Research and Development Website at **www.erd.epson.com** for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

1.2 Overview Description

The S1D13743 is a color mobile graphics engine with an embedded 464K byte display buffer. The S1D13743 supports a 8/16-bit Intel 80 CPU architecture while providing high performance bandwidth into 24 bpp display memory allowing for fast screen updates.

Products requiring a rotated display image can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory transparent to the software application. Resolutions supported include 352x440 @ 24 bpp single buffered or 320x240 @ 24 bpp double-buffered. The S1D13743 uses a double-buffer architecture to prevent any visual tearing during streaming video screen updates.

2 Features

2.1 Integrated Frame Buffer

- Embedded 464K byte SRAM display buffer

2.2 CPU Interface

- 8/16-bit Intel 80 interface (used for display or register data)
- Chip select is used to select device. When inactive, any input data/command is ignored.

2.3 Input Data Formats

- RGB: 8:8:8, 6:6:6, 5:6:5

Note
All input data is converted and stored as RGB 8:8:8 (see Section 12, “RGB Input Data Conversion” on page 74 for further information)

- YUV: 4:2:2, 4:2:0 (Internal YUV to RGB Converter converts and stores data as 24 bpp)

2.4 Display Support

- Active Matrix TFT interface
  - 18/24-bit interface
  - Frame Rate Modulation using 24 bpp data when configured for an 18-bit LCD panel.

2.5 Display Modes

- 24 bit-per-pixel (bpp) color depth

Note
All data is stored as 24 bpp. 18-bit panels are supported using the 18 msb’s when FRM is disabled or all 24 bits when FRM is enabled.

2.6 Display Features

- All display writes are handled by window apertures/position for complete or partial display updates. All window coordinates are referenced from the top left corner of the displayed image. Even for a rotated display, the top-left corner is maintained and no translation needs to take place.
- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of the display image. All displayed windows can have independent rotation. No additional programming necessary when enabling these modes.
- Double-Buffering is available to prevent image tearing during streaming input. To be supported, resolutions must fit within 228K bytes (½ of the available display buffer). A typical resolution is 320x240 @ 24 bpp.
- Pixel Doubling uses horizontal and vertical averaging to achieve smooth doubling of a single window. Pixel doubling may be applied to only a single window at any one time.
- Pixel Halving: no limitation on number of windows.

2.7 Clock Source

- Internal programmable PLL
- Single MHz clock input: CLKI
- CLKI is available as CLKOUT (separate CLKOUTEN pin associated with output)
  - output state = 0 when disabled

2.8 Miscellaneous

- Hardware / Software Power Save mode
- Input pin to enable/disable Power Save Mode
- General Purpose Input/Output pins are available (GPIO[7:0])
  - INT pin is associated with selectable GPIO inputs
- Package:

S1D13743B00C	FCBGA8 121-pin package
S1D13743F00A	QFP20 144-pin package

3 Block Diagram

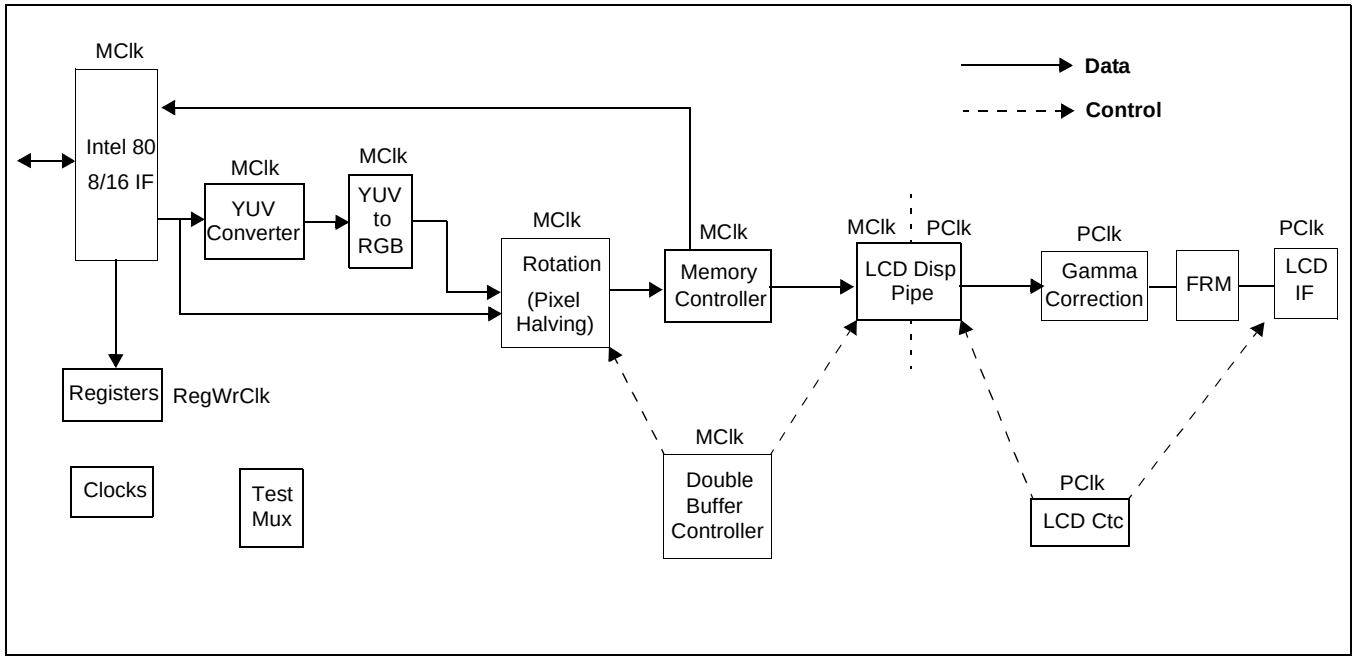


Figure 3-1: Block Diagram

4 Pins

4.1 Pinout Diagrams

	1	2	3	4	5	6	7	8	9	10	11
A	NC	NC	CLKOUT	CLKI	MD3	MD4	MD5	MD6	MD7	NC	NC
B	NC	MD2	MD12	CLKOUTEN	MD13	MD14	MD15	MD8	MD9	MD10	NC
C	MD0	MD11	MD1	IOVDD	VSS	VSS	CS#	WE#	RD#	D/C#	DE
D	RESET#	TE	GPIO_INT	PLLVDD	VCP	PLLVSS	COREVDD	IOVDD	HS	VS	PCLK
E	TEST1	TEST2	TESTEN	COREVDD	VSS	VSS	VSS	PIOVDD	NC	NC	NC
F	TEST0	SCANEN	CNF0	VSS	VSS	VSS	VSS	NC	NC	NC	NC
G	GPIO0	GPIO1	CNF1	PIOVDD	VSS	VSS	COREVDD	NC	NC	NC	NC
H	GPIO2	GPIO3	CNF2	IOVDD	PIOVDD	COREVDD	PIOVDD	NC	NC	VD23	VD22
J	GPIO4	GPIO5	PWRSVE	VD21	VD20	VD19	VD18	VD17	VD16	VD15	VD14
K	NC	GPIO6	GPIO7	VD13	VD12	VD11	VD10	VD9	VD8	VD7	NC
L	NC	NC	VD6	VD5	VD4	VD3	VD2	VD1	VD0	NC	NC

Figure 4-1: S1D13743 FCBGA Pinout (Top View)

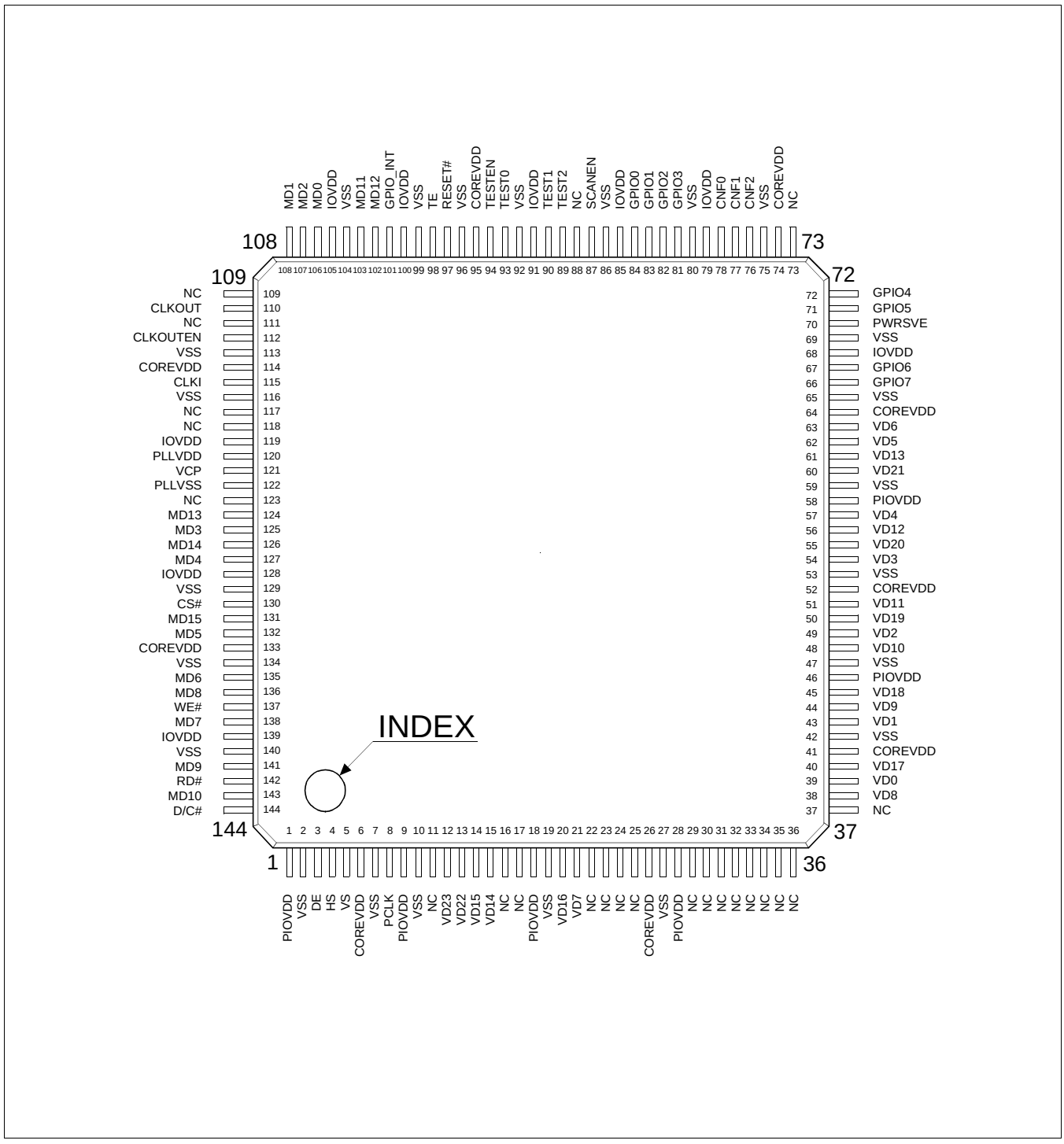


Figure 4-2: S1D13743 QFP20 Pinout (Top View)

4.2 Pin Descriptions

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin

RESET# / Power Save Status

H	=	High level output
L	=	Low level output
Hi-Z	=	High Impedance

Table 4-3 Cell Description

Item	Description
HI	H System[1] LVCMOS[3] Input Buffer
HIS	H System LVCMOS Schmitt Input Buffer
HID	H System LVCMOS Input Buffer with pull-down resistor
HO	H System LVCOMOS Output buffer
HB	H System LVCMOS Bidirectional Buffer
HBD	H System LVCMOS Bidirectional Buffer with pull-down resistor
HB_DSEL	H System LVCMOS Bidirectional Buffer with Drive Selector
LIDS	L System[2] LVCMOS Schmitt Input Buffer with pull-down resistor
LITR	L System Transparent Input Buffer

[1] H System is IOVDD and PIOVDD (see Section 6, “D.C. Characteristics” on page 21).
[2] L System is COREVDD (see Section 6, “D.C. Characteristics” on page 21).
[3] LVCMOS is Low Voltage CMOS (see Section 6, “D.C. Characteristics” on page 21).

4.2.1 Intel 80 Host Interface

Table 4-1: Host Interface Pin Descriptions

Pin Name	Type	FCBGA Pin #	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
MD[15:0]	IO	B7, B6, B5, B3, C2, B10, B9, B8, A9, A8, A7, A6, A5, B2, C3, C1	131,126, 124,102, 103,143, 141,136, 138,135, 132,127, 125,107, 108,106	HB	IOVDD	Hi-Z	Hi-Z	Intel 80 Host Data lines 15-0. **Note:** The Host Data Lines can be swapped (i.e. D15 = D0) using the CNF0 pin. For details, see Section 4.3, “Summary of Configuration Options” on page 18.
WE#	I	C8	137	HI	IOVDD	Input	Input	This input pin is the Write Enable signal.
RD#	I	C9	142	HI	IOVDD	Input	Input	This input pin is the Read Enable signal.
CS#	I	C7	130	HI	IOVDD	Input	Input	This input pin is the Chip Select signal.
D/C#	I	C10	144	HI	IOVDD	Input	Input	This input pin selects between Intel 80 address and data.
TE	O	D2	98	HO	IOVDD	L	L	Tearing Effect: this pin will reflect the VSYNC, HSYNC or the OR’d combination status of the display.
GPIO_INT	O	D3	101	HO	IOVDD	L	L	This interrupt pin is associated with selected GPIO pins when configured as inputs or outputs. See Section 10.3.10, “General Purpose IO Pins Registers” on page 71 for operational description.
RESET#	I	D1	97	HIS	IOVDD	Input	Input	This active low input sets all internal registers to the default state and forces all signals to their inactive states.

4.2.2 LCD Interface

Table 4-2: LCD Interface Pin Descriptions

Pin Name	Type	FCBGA Pin #	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
VD[23:0]	IO	H10, H11, J4, J5, J6, J7, J8, J9, J10, J11, K4, K5, K6, K7, K8, K9, K10, L3, L4, L5, L6, L7, L8, L9	12,13,60, 55,50,45, 40,20,14, 15,61,56, 51,48,44, 38,21,63, 62,57,54, 49,43,39	HB_ DSEL	PIOVDD	L	L	Panel Data lines pins 23-0. **Note:** The Panel Data Lines can be swapped (i.e. VD23 = VD0) using the VD Data Swap bit, REG[14h] bit 7. **Note:** The VD output drive is selectable between 2.5mA and 6.5mA using the CNF2 pin. For details, see Section 4.3, "Summary of Configuration Options" on page 18.
VS	O	D10	5	HO	PIOVDD	H	L	This output pin is the Vertical Sync pulse.
HS	O	D9	4	HO	PIOVDD	H	L	This output pin is the Horizontal Sync pulse.
PCLK	O	D11	8	HO	PIOVDD	CLKI	L	This output pin is the Data Clock.
DE	O	C11	3	HO	PIOVDD	L	L	This output pin is the Data Enable.

Note
The LCD interface requires a separate power rail (PIOVDD) to support the configurable IO drive. For details, see the CNF2 description in Section 4.3, "Summary of Configuration Options" on page 18.

Note
The input function of VD[23:0] is used for production test only.

4.2.3 Clocks

Table 4-3: Clock Input Pin Descriptions

Pin Name	Type	FCBGA Pin #	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
CLKI	I	A4	115	HIS	IOVDD	Input	Input	MHz input for PLL operation or MHz input if PLL is bypassed.
CLKOUT	O	A3	110	HO	IOVDD	L	CLKI	This output pin represents the CLKI pin if enabled by CLKOUTEN. When disabled, the output is low. **Note:** This output is not affected by the various power save modes.
CLKOUTEN	I	B4	112	HI	IOVDD	Input	Input	This pin enables/disables the CLKOUT pin.

4.2.4 Miscellaneous

Table 4-4: Miscellaneous Pin Descriptions

Pin Name	Type	FCBGA Pin #	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
CNF[2:0]	I	H3, G3, F3	76,77,78	HI	IOVDD	Input	Input	These inputs are used for power-up configuration. For further details, see Section 4.3, “Summary of Configuration Options” on page 18. **Note: These pins must be connected directly to IOVDD or VSS.**
TESTEN	I	E3	94	LIDS	IOVDD	—	—	This is the Test Enable input and is used for production test only. This pin should be left unconnected for normal operation.
GPIO[7:0]	IO	K3, K2, J2, J1, H2, H1, G2, G1	66,67,71,72, 81,82,83,84	HBD	IOVDD	L	Pull-down Active	These pins are general purpose input/output pins. These pins have internal pull-down resistors which can be controlled using REG[64h].
PWRSVE	I	J3	70	HID	IOVDD	Input	Pull-down Active	This pin enables/disables the Standby Power Save Mode. This pin has an internal pull-down resistor which is always active.
TEST[2:0]	I	E2, E1, F1	89,90,93	HID	IOVDD	—	—	These are Test Function pins and are used for production test only. These pins should be left unconnected for normal operation.
SCANEN	I	F2	87	HID	IOVDD	—	—	This is the Test Scan Enable input and is used for production test only. This pin should be left unconnected for normal operation.
VCP	I	D5	121	LITR	PLLVDD	—	—	This is the PLL VCP Test pin and is used for production test only. This pin should be left unconnected for normal operation.
NC	—	A1, A2, A10, A11, B1, B11, E9, E10, E11, F8, F9, F10, F11, G8, G9, G10, G11, H8, H9, K1, K11, L1, L2, L10, L11	11,16,17,22, 23,24,25,29, 30,31,32,33, 34,35,36,37, 73,88,109, 111,117, 118,123	—	—	—	—	These pins are not connected.

4.2.5 Power And Ground

Table 4-5: Power And Ground Pin Descriptions

Pin Name	Type	FCBGA Pin #	QFP Pin #	Cell	Description
COREVDD	P	D7, E4, G7, H6	6,26,41,52,64,74, 95,114,133	P	Core power supply
IOVDD	P	C4, D8, H4	68,79,85,91,100, 105,119,128,139	P	IO power supply for the host interface
PIOVDD	P	E8, G4, H5, H7	1,9,18,28,46,58	P	IO power supply for the panel interface
PLLVDD	P	D4	120	P	PLL power supply
PLLVSS	P	D6	122	P	GND for PLL
VSS	P	C5, C6, E5, E6, E7, F4, F5, F6, F7, G5, G6	2,7,10,19,27,42, 47,53,59,65,69, 75,80,86,92,96, 99,104,113,116, 129,134,140	P	GND

4.3 Summary of Configuration Options

These pins are used for power-up configuration and must be connected directly to IOV_{DD} or V_{SS}. Changing the state of these pins is only permitted when RESET# is low (active). The status of these pins can be read in REG[02h] using the CNF[2:0] Status bits.

Table 4-6: Summary of Power-On/Reset Options

Configuration Input	Power-On/Reset State	
	1 (connected to IOV_{DD})	**0 (Connected to V_{SS})**
CNF0	Host Data Lines are normal: If CNF1 = 1b, then D15 = D15, etc. If CNF1 = 0b, then D7 = D7, etc.	Host Data Lines are swapped: If CNF1 = 1b, then D15 = D0, etc. If CNF1 = 0b, then D7 = D0, etc.
CNF1	Host Data is 16-bit (see Note)	Host Data is 8-bit (see Note)
CNF2	PIOVDD output current = 6.5mA	PIOVDD output current = 2.5mA

Note

When CNF1 = 0b, all register access is 8-bit only.
When CNF1 = 1b (16-bit), all register access is 8-bit ONLY (most significant byte on the data bus is ignored) except for the Memory Data Port (REG[48h] ~ REG[49h]) which is 16-bit.

5 Pin Mapping

5.1 Intel 80 Data Pins

Intel 80 data pin mapping is controlled by CNF[1:0]. For details on CNF[1:0], see Section 4.3, “Summary of Configuration Options” on page 18.

Table 5-1: Intel 80 Data Pin Mapping

Pin Name	16-Bit Data No Swap (CNF1=1b, CNF0=1b)	16-Bit Data Swapped (CNF1=1b, CNF0=0b)	8-Bit Data No Swap (CNF1=0b, CNF0=1b)	8-Bit Data Swapped (CNF1=0b, CNF0=0b)
MD15	MD15	MD0	Hi-Z	Hi-Z
• • •	• • •	• • •	• • •	• • •
MD8	MD8	MD7	Hi-Z	Hi-Z
MD7	MD7	MD8	MD7	MD0
• • •	• • •	• • •	• • •	• • •
MD0	MD0	MD15	MD0	MD7

5.2 LCD Interface Data Pins

LCD interface data pin mapping is controlled by REG[14h] bit 7.

Table 5-2: LCD Interface Data Pin Mapping for 24-bit Panels

Pin Name	24-Bit Data No Swap REG[14h] bit 7 = 0b	24-Bit Data Swapped REG[14h] bit 7 = 1b
VD23	VD23	VD0
• • •	• • •	• • •
VD18	VD18	VD5
VD17	VD17	VD6
• • •	• • •	• • •
VD0	VD0	VD23

Table 5-3: LCD Interface Data Pin Mapping for 18-bit Panels

Pin Name	18-Bit Data No Swap REG[14h] bit 7 = 0b	18-Bit Data Swapped REG[14h] bit 7 = 1b
VD23	Driven Low	
• • •		
VD18		
VD17	VD17	VD0
• • •	• • •	• • •
VD0	VD0	VD17

6 D.C. Characteristics

6.1 Absolute Maximum Ratings

Table 6-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
Core V_{DD}	Core Supply Voltage	V_{SS} - 0.3 ~ 2.0	V
PLL V_{DD}	PLL Supply Voltage	V_{SS} - 0.3 ~ 2.0	V
IO V_{DD}	Host IO Supply Voltage	Core V_{DD} ~ 4.0	V
PIO V_{DD}	Panel IO Supply Voltage	Core V_{DD} ~ 4.0	V
V_{IN}	Input Signal Voltage	V_{SS} - 0.3 ~ IO V_{DD} + 0.3	V
V_{OUT}	Output Signal Voltage	V_{SS} - 0.3 ~ IO V_{DD} + 0.3	V
I_{OUT}	Output Signal Current	±10	mA

6.2 Recommended Operating Conditions

Table 6-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Core Supply Voltage	V_{SS} = 0 V	1.40	1.50	1.60	V
PLL V_{DD}	PLL Supply Voltage	V_{SS} = 0 V	1.40	1.50	1.60	V
IO V_{DD}	Host IO Supply Voltage	V_{SS} = 0 V	1.65	—	3.6	V
PIO V_{DD}	Panel IO Supply Voltage	V_{SS} = 0 V	1.65	—	3.6	V
V_{IN}	Input Voltage	—	V_{SS}	—	IO V_{DD}	V
T_{OPR}	Operating Temperature	—	-40	+25	+85	▪ C

Note

There are no special Power On/Off requirements with respect to sequencing the various VDD pins. There are also no special requirements for the IO signals, however, Inputs should not be floating. If the input signals were to power up in a valid cycle, the S1D13743 would decode the cycle.

6.3 Electrical Characteristics

The following characteristics are for: IO V_{DD}, V_{SS} = 0V, T_{OPR} = -40 to +85°C.

Table 6-3: Electrical Characteristics for IOVDD or PIOVDD = 1.8V ± 0.15V

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{QALL}	Quiescent Current	CLKI stopped (grounded), Sleep Mode enabled, all power supplies active	—	100	—	µA
I_{PLL}	PLL Current	f_{PLL} = 54MHz	—	500	1000	µA
I_{CORE}	Operation Peak Current	COREVDD Power Pin	—	—	74	mA
P_{CORE}	Core Typical Operating Power	see Note 1	—	9.2	—	mW
P_{PLL}	PLL Typical Operating Power		—	667	—	µW
P_{PIO}	PIO Typical Operating Power		—	2.7	—	mW
P_{HIO}	HIO Typical Operating Power		—	20	—	µW
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA
IOV_{OH2}	High Level Output Voltage	IOV_{DD} = min I_{OH2} = -2.5mA	IOVDD - 0.40	—	IOVDD	V
$PIOV_{OH2}$	High Level Output Voltage	PIOVDD = min I_{OH2} = -2.5mA	PIOVDD - 0.40	—	PIOVDD	V
$PIOV_{OH4}$	High Level Output Voltage	PIOVDD = min I_{OH2} = -6.5mA	PIOVDD - 0.40	—	PIOVDD	V
IOV_{OL2}	Low Level Output Voltage	IOVDD = min I_{OL2} = 2.5mA	VSS	—	0.40	V
$PIOV_{OL2}$	Low Level Output Voltage	PIOVDD = min I_{OL2} = 2.5mA	VSS	—	0.40	V
$PIOV_{OL4}$	Low Level Output Voltage	PIOVDD = min I_{OL2} = 6.5mA	VSS	—	0.40	V
IOV_{IH}	High Level Input Voltage	CMOS Input	1.27	—	—	V
$PIOV_{IH}$	High Level Input Voltage	CMOS Input	1.27	—	—	V
IOV_{IL}	Low Level Input Voltage	CMOS Input	—	—	0.57	V
$PIOV_{IL}$	Low Level Input Voltage	CMOS Input	—	—	0.57	V
IOV_{T+}	Positive Trigger Voltage	CMOS Schmitt	0.57	—	1.56	V
IOV_{T-}	Negative Trigger Voltage	CMOS Schmitt	0.33	—	1.27	V
IO V_H	Hysteresis Voltage	CMOS Schmitt	0.24	—	—	V
R_{PU1}	Pull-Up Resistance Type1	V_I = VSS	40	100	240	kΩ
R_{PD1}	Pull-Down Resistance Type1	V_I = VDD	40	100	240	kΩ
R_{PU2}	Pull-Up Resistance Type2	V_I = VSS	80	200	480	kΩ
R_{PD2}	Pull-Down Resistance Type2	V_I = VDD	80	200	480	kΩ
C_{IO}	Pin Capacitance	f = 1MHz, VDD = 0V	—	—	8	pF

Note

1. Typical Operating Current Environment:
   352x416 18-bit TFT panel
   24bpp memory storage
   CLKI = 19.2MHz
   SYSCLK = 48.5MHz (PLL)
   PCLK = divide by 4
   V_{CORE} = 1.5V
   V_{HIO} = 1.8V
   V_{PIO} = 1.8V

The following characteristics are for: IOVDD, VSS = 0V, T_{OPR} = -40 to +85°C.

Table 6-4: Electrical Characteristics for IOVDD or PIOVDD = 3.3V ± 0.3V

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{QALL}	Quiescent Current	Quiescent Conditions	—	160	—	µA
I_{PLL}	PLL Current	f_{PLL} = 54MHz	—	500	1000	µA
I_{CORE}	Operation Peak Current	COREVDD Power Pin	—	—	74	mA
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA
IOV_{OH2}	High Level Output Voltage	IOV_{DD} = min I_{OH2} = -4.0mA	IOVDD - 0.40	—	IOVDD	V
$PIOV_{OH2}$	High Level Output Voltage	PIOVDD = min I_{OH2} = -4.0mA	PIOVDD - 0.40	—	PIOVDD	V
$PIOV_{OH4}$	High Level Output Voltage	PIOVDD = min I_{OH2} = -12.0mA	PIOVDD - 0.40	—	PIOVDD	V
IOV_{OL2}	Low Level Output Voltage	IOVDD = min I_{OL2} = 4.0mA	VSS	—	0.40	V
$PIOV_{OL2}$	Low Level Output Voltage	PIOVDD = min I_{OL2} = 4.0mA	VSS	—	0.40	V
$PIOV_{OL4}$	Low Level Output Voltage	PIOVDD = min I_{OL2} = 12.0mA	VSS	—	0.40	V
IOV_{IH}	High Level Input Voltage	CMOS Input	2.20	—	—	V
$PIOV_{IH}$	High Level Input Voltage	CMOS Input	2.20	—	—	V
IOV_{IL}	Low Level Input Voltage	CMOS Input	—	—	0.80	V
$PIOV_{IL}$	Low Level Input Voltage	CMOS Input	—	—	0.80	V
IOV_{T+}	Positive Trigger Voltage	CMOS Schmitt	1.40	—	2.70	V
IOV_{T-}	Negative Trigger Voltage	CMOS Schmitt	0.60	—	1.80	V
IO V_H	Hysteresis Voltage	CMOS Schmitt	0.45	—	—	V
R_{PU1}	Pull-Up Resistance Type1	V_I = VSS	20	50	120	kΩ
R_{PD1}	Pull-Down Resistance Type1	V_I = VDD	20	50	120	kΩ
R_{PU2}	Pull-Up Resistance Type2	V_I = VSS	40	100	240	kΩ
R_{PD2}	Pull-Down Resistance Type2	V_I = VDD	40	100	240	kΩ
C_{IO}	Pin Capacitance	f = 1MHz, VDD = 0V	—	—	8	pF

7 A.C. Characteristics

7.1 Clock Timing

7.1.1 Input Clocks

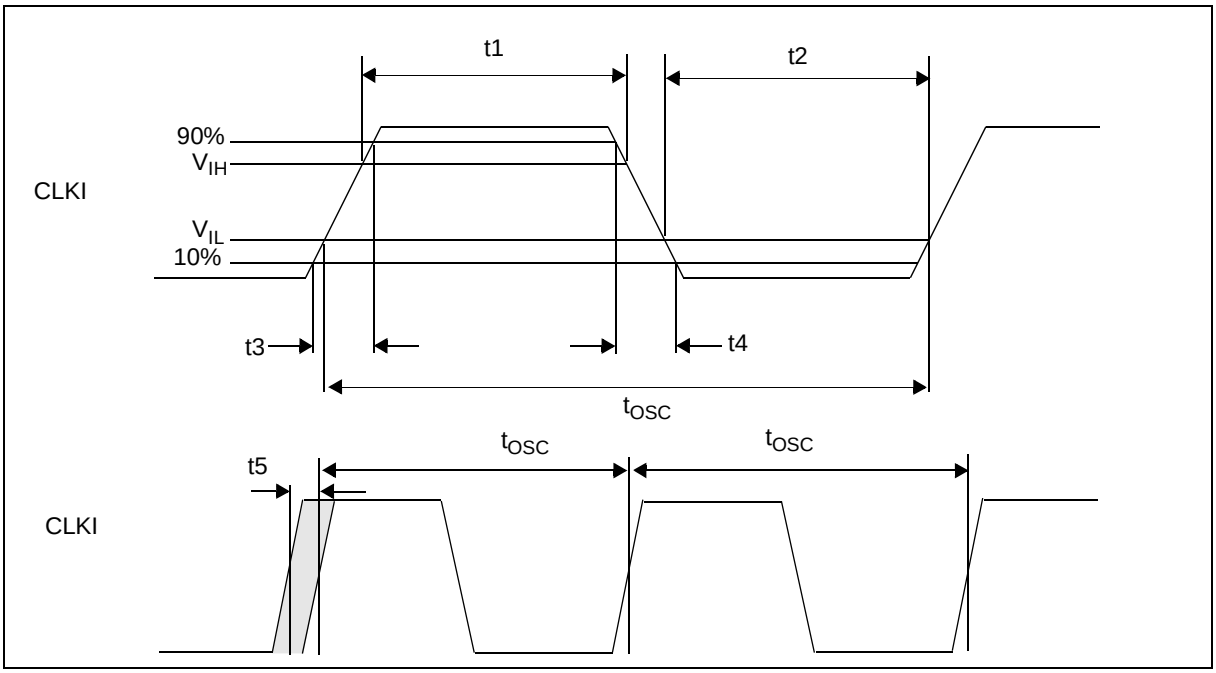


Figure 7-1 Clock Input Required (CLKI)

Table 7-1 Clock Input Requirements (CLKI)

Symbol	Parameter	Min	Typ	Max	Units
f_{OSC} (see note 1)	Input clock frequency - PLL used for System Clock	1	—	33	MHz
	Input clock frequency - CLKI used for System Clock	0	—	68.59	MHz
t_{OSC}	Input clock period	—	$1/f_{OSC}$	—	µs
t1	Input clock pulse width high	$0.4t_{OSC}$	—	$0.6t_{OSC}$	µs
t2	Input clock pulse width low	$0.4t_{OSC}$	—	$0.6t_{OSC}$	µs
t3	Input clock rise time (10% ~ 90%)	—	—	5.0	ns
t4	Input clock fall time (90% ~ 10%)	—	—	5.0	ns
t5	Input clock period jitter (see Notes 2 and 4)	-300		300	ps
t6 (see Note 6)	Input clock cycle jitter (see Notes 3 and 4)	-300		300	ps

1. The minimum System Clock frequency required for correct operation depends on the cycle length of the Intel 80 interface. See Section 9.4, “Setting SYSCLK and PCLK” on page 43 for more details.
2. The input clock period jitter is the displacement relative to the center period (reciprocal of the center frequency).
3. The input clock cycle jitter is the difference in period between adjacent cycles.
4. The jitter characteristics must satisfy both the t5 and t6 characteristics.
5. Input Duty cycle is not critical and can be 40/60.
6. $t6 = 2 \times t_{OSC}$

7.1.2 PLL Clock

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible. The jitter of the input clock waveform should be as small as possible.

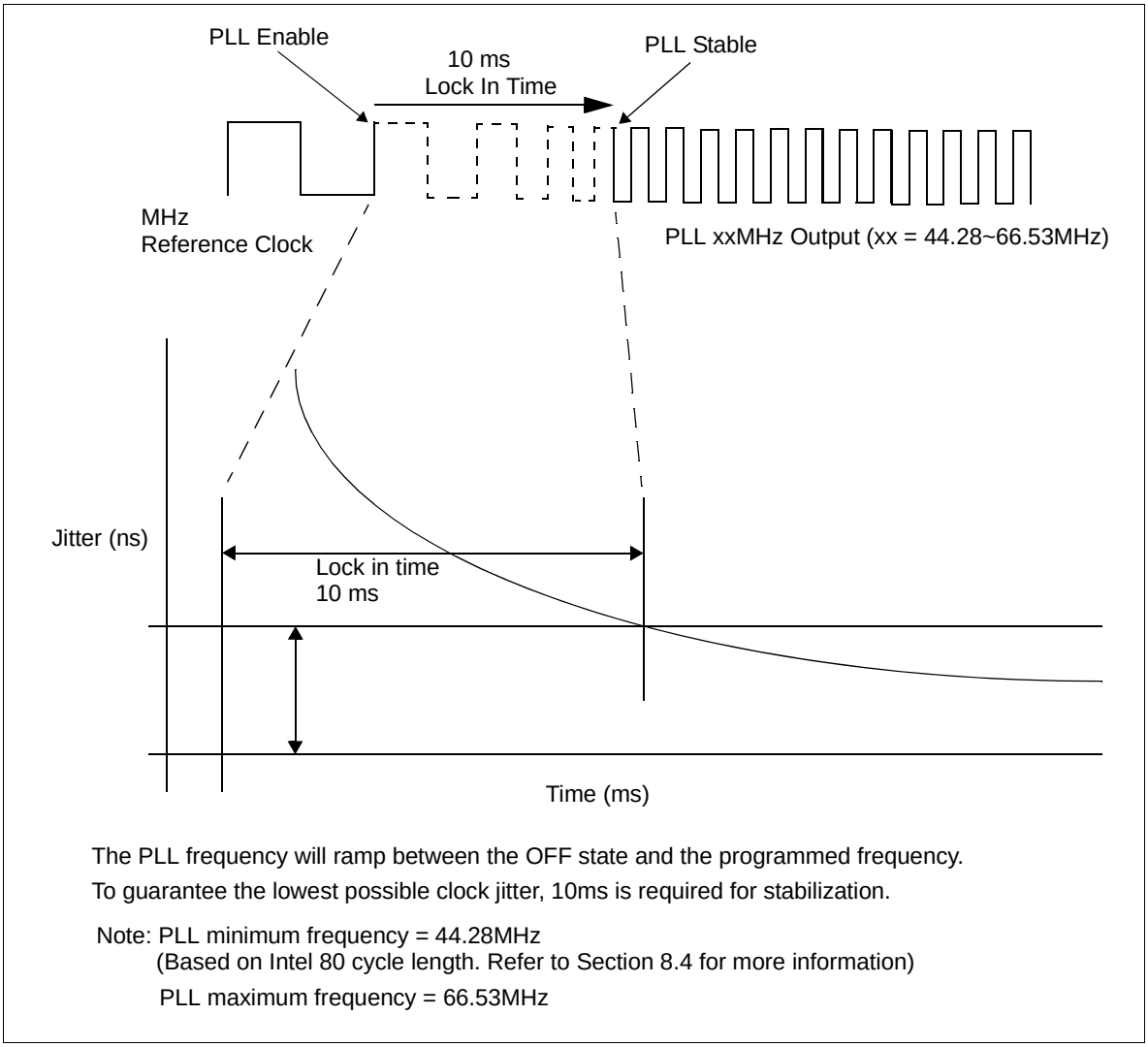


Figure 7-2: PLL Start-Up Time

Table 7-2: PLL Clock Requirements

Symbol	Parameter	Min	Max	Units
f_{PLL}	PLL output clock frequency	44.28 (Note 1)	66.53	MHz
t_{PJref}	PLL output clock period jitter	-3	3	%
t_{PDuty}	PLL output clock duty cycle	40	60	%
t_{PStal}	PLL output stable time	—	10	ms

1. Refer to Section 9.4, “Setting SYSCLK and PCLK” on page 43.

7.2 RESET# Timing

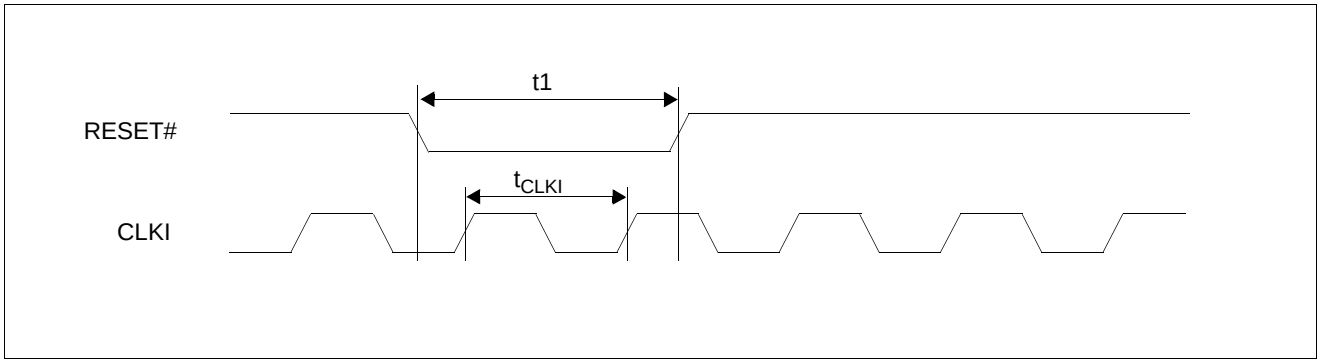


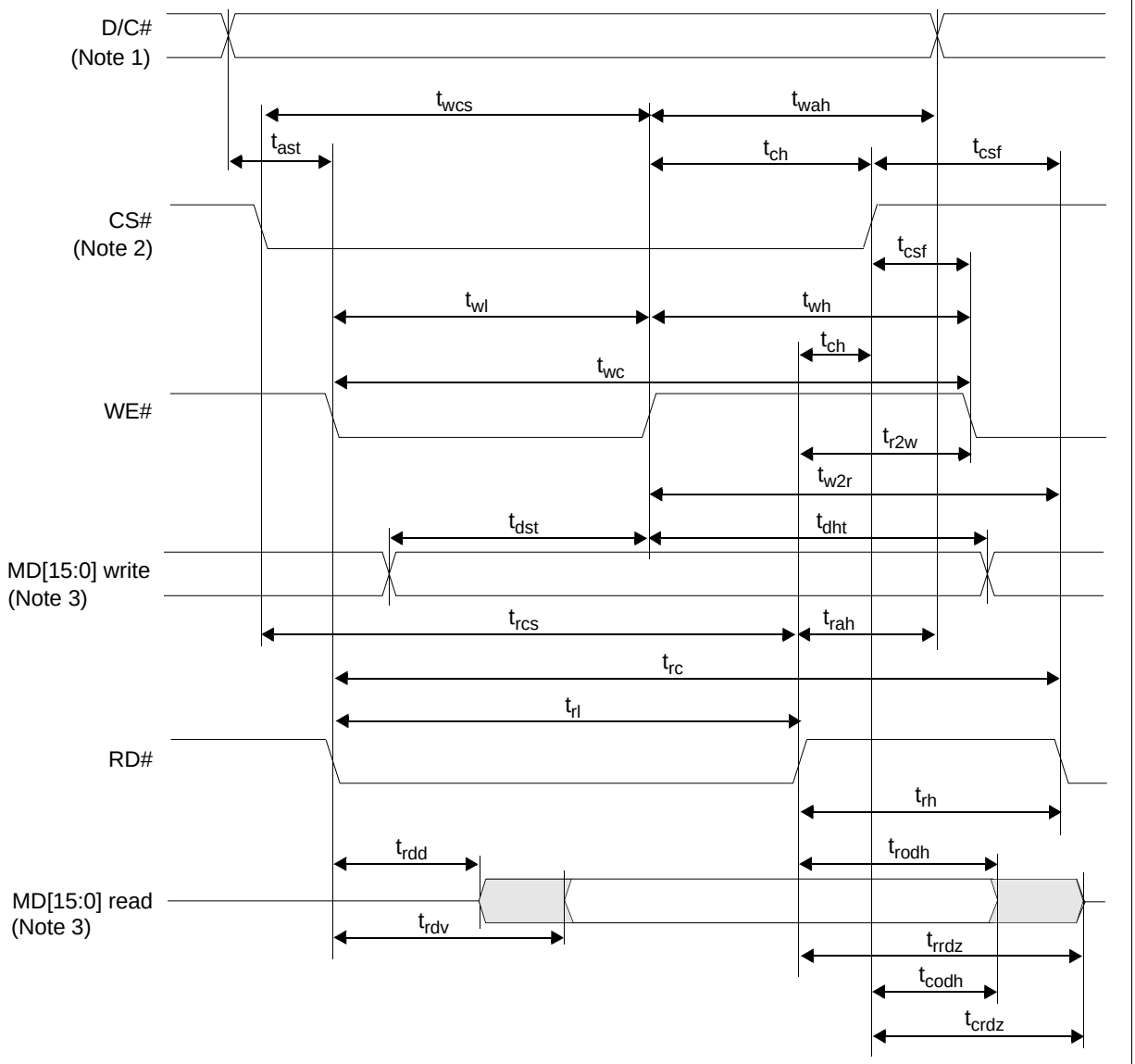
Figure 7-3 S1D13743 RESET# Timing

Table 7-3 S1D13743 RESET# Timing

Symbol	Parameter	Min	Max	Units
t1	Active Reset Pulse Width	1	—	CLKI

7.3 Host interface Timing

7.3.1 Intel 80 Interface Timing - 1.8 Volt



Note 1: The D/C# input pin is used to distinguish between Address and Data.

Note 2: The CS# pin can be kept low between write and read pulses as the register addresses will auto-increment. The register address will auto-increment in word increments for all register access except the Memory Data Port. Writes to the Memory Data Port will not increment the register address to support burst data writes to memory.

Note 3: When CNF1=0, only MD[7:0] are used.
When CNF1=1, MD[15:0] are used for accesses to the Memory Data Port. MD[7:0] are used for all other accesses.

Figure 7-4: Intel 80 Input A.C. Characteristics - 1.8 Volt

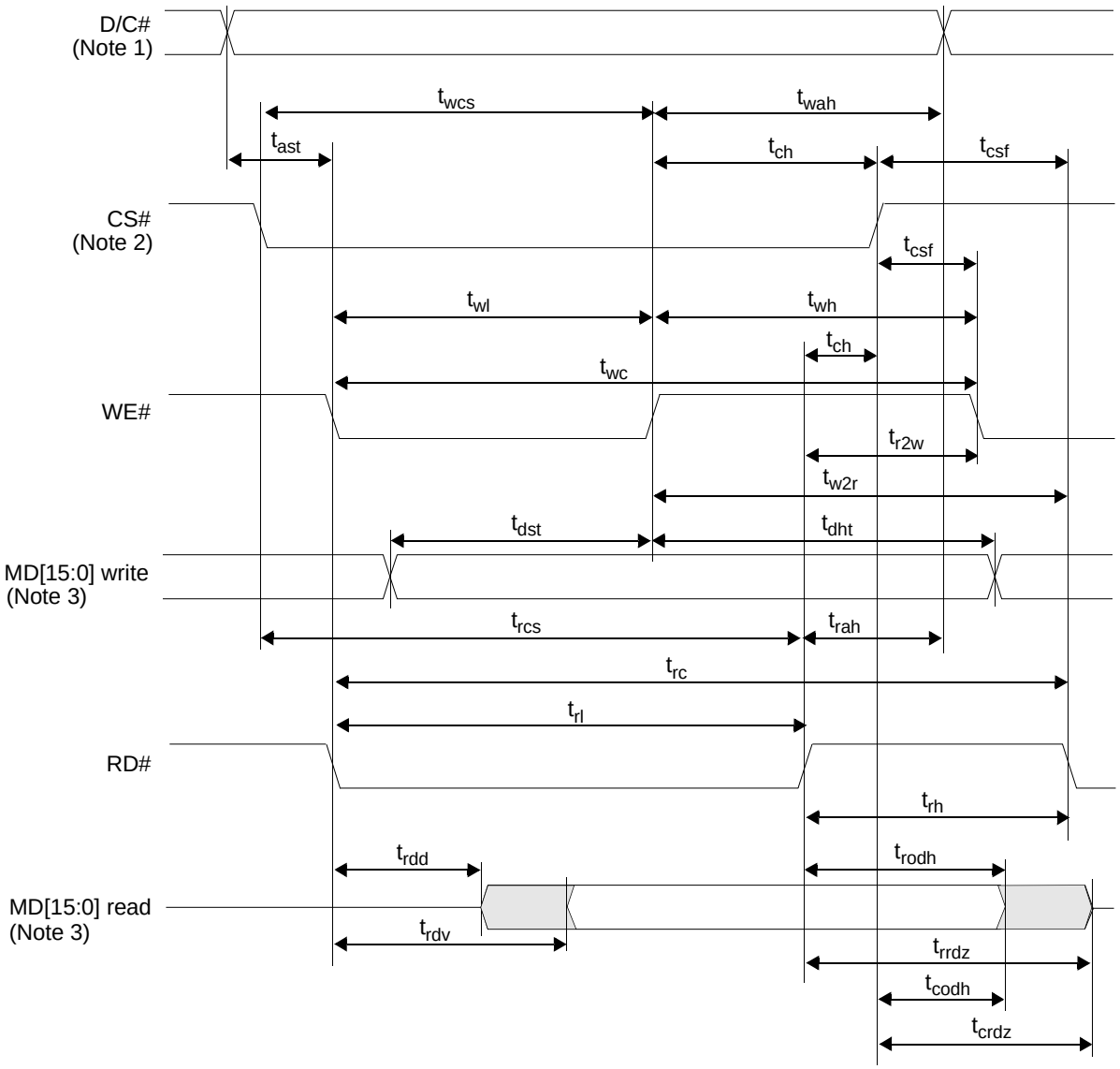
Table 7-4: Intel 80 Input A.C. Characteristics - 1.8 Volt

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/C#	t_{ast}	Address setup time (read/write)	1	-	ns	
	t_{wah}	Address hold time (write)	6	-	ns	
	t_{rah}	Address hold time (read)	30	-	ns	
CS#	t_{wcs}	Chip Select setup time (write)	t_{wl}	-	ns	
	t_{rcs}	Chip Select setup time (read)	t_{rl}	-	ns	
	t_{ch}	Chip Select hold time (read/write)	1	-	ns	
	t_{csf}	Chip Select Wait time (read/write)	0	-	ns	
WE#	t_{wc}	Register Write cycle	12	-	ns	
		LUT write cycle	2SYSCLK + 2	-	ns	
		Memory write cycle	2SYSCLK + 2	-	ns	
	t_{wl}	Pulse low duration	5	-	ns	
	t_{wh}	Pulse high duration	t_{wc} - t_{wl}	-	ns	
	t_{w2r}	WR# rising edge to RD# falling edge	12	-	ns	Note 1
RD#	t_{r2w}	RD# rising edge to WR# falling edge	27	-	ns	Note 2
	t_{rc}	Read cycle	t_{rl} + t_{rh}	-	ns	
	t_{rl}	Pulse low duration	t_{rdv}	-	ns	
	t_{rh}	Pulse high duration for Registers	36	-	ns	
		Pulse high duration for Memory and LUT	1SYSCLK + 25	-	ns	
MD[15:0] (Note 4)	t_{dst}	Write data setup time	2	-	ns	
	t_{dht}	Write data hold time	7	-	ns	
	t_{rodh}	Read data hold time from RD# rising edge	11	-	ns	
	t_{rrdz}	RD# rising edge to MD High-Z	-	32	ns	Note 3
	t_{codh}	Read data hold time from CS# rising edge	1	-	ns	
	t_{crdz}	CS# rising edge to MD High-Z	-	8	ns	
	t_{rdv}	RD# falling edge to MD valid for Registers	-	17	ns	CL=30pF
		RD# falling edge to MD valid for LUT	-	4SYSCLK + 27	ns	
		RD# falling edge to MD valid for Memory	-	5SYSCLK + 20	ns	
		RD# falling edge to MD valid for Registers	-	12	ns	CL = 8pF
		RD# falling edge to MD valid for LUT	-	4SYSCLK + 22	ns	
		RD# falling edge to MD valid for Memory	-	5SYSCLK + 15	ns	
	t_{rdd}	RD# falling edge to MD driven	4	-	ns	CL=30pF
		RD# falling edge to MD driven	3	-	ns	CL = 8pF

Note

1. For a read cycle after a write cycle, MD[15:0] must be driven Hi-Z a maximum of t_{rdd} after the falling edge of RD#.
2. For a write cycle after a read cycle, MD[15:0] should not be driven by the host until t_{rrdz} after the rising edge of RD#.
3. Assumes CS# remains low. After the rising edge of RD#, if CS# goes high before t_{rrdz} then MD[15:0] will go to High-Z according to t_{crdz}.
4. When CNF1=0, only MD[7:0] are used. When CNF1=1, MD[7:0] are used for all accesses except for the Memory Data Port when MD[15:0] are used.

7.3.2 Intel 80 Interface Timing - 3.3 Volt



Note 1: The D/C# input pin is used to distinguish between Address and Data.

Note 2: The CS# pin can be kept low between write and read pulses as the register addresses will auto-increment. The register address will auto-increment in word increments for all register access except the Memory Data Port. Writes to the Memory Data Port will not increment the register address to support burst data writes to memory.

Note 3: When CNF1=0, only MD[7:0] are used.
When CNF1=1, MD[15:0] are used for accesses to the Memory Data Port. MD[7:0] are used for all other accesses.

Figure 7-5: Intel 80 Input A.C. Characteristics - 3.3 Volt

Table 7-5: Intel 80 Input A.C. Characteristics - 3.3 Volt

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/C#	t_{ast}	Address setup time (read/write)	2	—	ns	
	t_{wah}	Address hold time (write)	6	—	ns	
	t_{rah}	Address hold time (read)	31	—	ns	
CS#	t_{wcs}	Chip Select setup time (write)	t_{wl}	—	ns	
	t_{rcs}	Chip Select setup time (read)	t_{rl}	—	ns	
	t_{ch}	Chip Select hold time (read/write)	0	—	ns	
	t_{csf}	Chip Select Wait time (read/write)	1	—	ns	
WE#	t_{wc}	Register Write cycle	10	—	ns	
		LUT write cycle	2SYSCLK + 2	—	ns	
		Memory write cycle	2SYSCLK + 2	—	ns	
	t_{wl}	Pulse low duration	5	—	ns	
	t_{wh}	Pulse high duration	t_{wc} - t_{wl}	—	ns	
	t_{w2r}	WR# rising edge to RD# falling edge	12	—	ns	Note 1
RD#	t_{r2w}	RD# rising edge to WR# falling edge	27	—	ns	Note 2
	t_{rc}	Read cycle	t_{rl} + t_{rh}	—	ns	
	t_{rl}	Pulse low duration	t_{rdv}	—	ns	
	t_{rh}	Pulse high duration for Registers	36	—	ns	
		Pulse high duration for Memory and LUT	1SYSCLK + 26	—	ns	
MD[15:0] (Note 4)	t_{dst}	Write data setup time	2	—	ns	
	t_{dht}	Write data hold time	7	—	ns	
	t_{rodh}	Read data hold time from RD# rising edge	11	—	ns	
	t_{rrdz}	RD# rising edge to MD High-Z	—	31	ns	Note 3
	t_{codh}	Read data hold time from CS# rising edge	0.5	—	ns	
	t_{crdz}	CS# rising edge to MD High-Z	—	8	ns	
	t_{rdv}	RD# falling edge to MD valid for Registers	—	12	ns	CL=30pF
		RD# falling edge to MD valid for LUT	—	4SYSCLK + 22	ns	
		RD# falling edge to MD valid for Memory	—	5SYSCLK + 15	ns	
		RD# falling edge to MD valid for Registers	—	10	ns	CL = 8pF
		RD# falling edge to MD valid for LUT	—	4SYSCLK + 19	ns	
		RD# falling edge to MD valid for Memory	—	5SYSCLK + 12	ns	
	t_{rdd}	RD# falling edge to MD driven	3	—	ns	CL=30pF
		RD# falling edge to MD driven	2	—	ns	CL = 8pF

Note

1. For a read cycle after a write cycle, MD[15:0] must be driven Hi-Z a maximum of t_{rdd} after the falling edge of RD#.
2. For a write cycle after a read cycle, MD[15:0] should not be driven by the host until t_{rrdz} after the rising edge of RD#.
3. Assumes CS# remains low. After the rising edge of RD#, if CS# goes high before t_{rrdz} then MD[15:0] will go to High-Z according to t_{crdz}.
4. When CNF1=0, only MD[7:0] are used. When CNF1=1, MD[7:0] are used for all accesses except for the Memory Data Port when MD[15:0] are used.

7.3.3 Definition of Transition Time to Hi-Z State

Due to the difficulty of Hi-Z impedance measurement for high speed signals, transition time from High/Low to Hi-Z specified as follows.

- High to Hi-Z delay time: t_{pHZ}, delay time when a gate voltage of final stage of the Pch-MOSFET turns to 0.8 x IOVDD (Pch-MOSFET is off). Total delay time to Hi-Z is calculated as follows:
  Internal logic delay + t_{pHZ} (from High to Hi-Z)
- Low to Hi-Z delay time: t_{pLZ}, delay time when a gate voltage of final stage of the Nch-MOSFET turns to 0.2 x IOVDD (Nch-MOSFET is off). Total delay time to Hi-Z is calculated as follows:
  Internal logic delay + t_{pHZ} (from High to Hi-Z)

The functional model of a final stage of the Tri state Output Cell is shown in Figure 7-6: “Definition of transition time to Hi-Z state”.

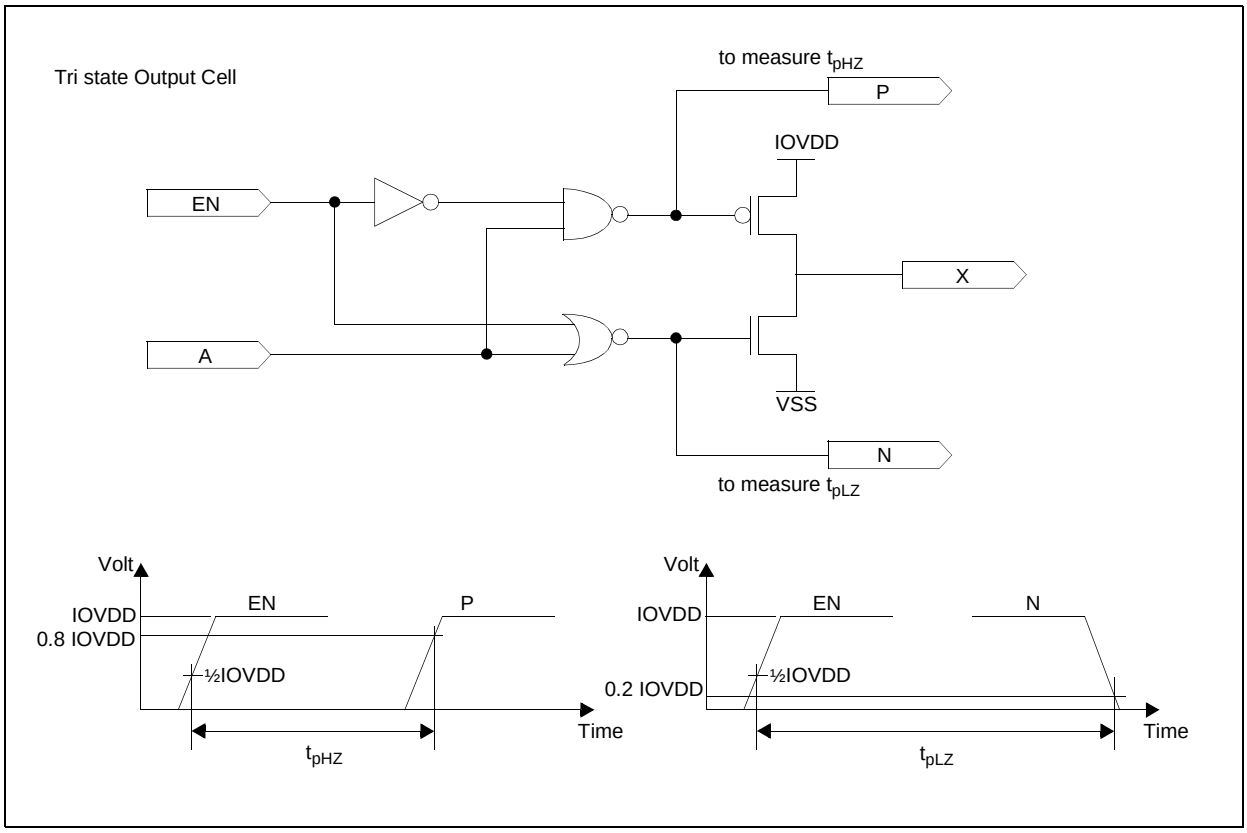


Figure 7-6: Definition of Transition Time to Hi-Z State

7.4 Display Interface

The timing parameters required to drive a flat panel display are shown below. Timing details for each supported panel type are provided in the remainder of this section.

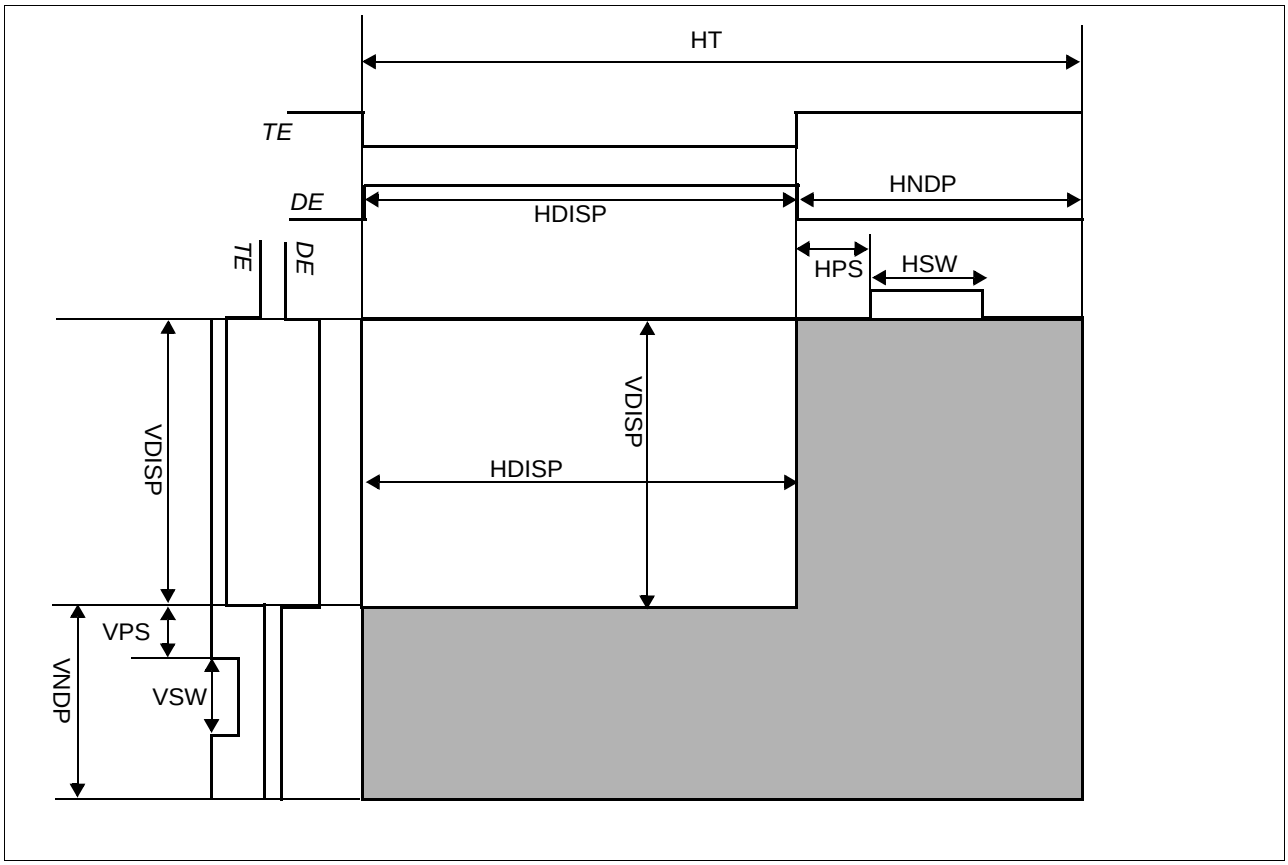


Figure 7-7: Panel Timing Parameters

Table 7-6: Panel Timing Parameter Definition and Register Summary

Symbol	Description	Derived From	Units
HDISP	Horizontal Display Width	REG[16h] bits 6-0 x 8	Ts (Note 1)
HNDP	Horizontal Non-Display Period	REG[18h] bits 6-0	
HPS	HS Pulse Start Position	REG[22h] bits 6-0	
HSW	HS Pulse Width	REG[20h] bits 6-0	
VDISP	Vertical Display Height	REG[1Ch] bits 1-0, REG[1Ah] bits 7-0	Lines (HT)
VNDP	Vertical Non-Display Period	REG[1Eh] bits 7-0	
VPS	VS Pulse Start Position	REG[26h] bits 7-0	
VSW	VS Pulse Width	REG[24h] bits 5-0	

1. TS = $1/f_{PCLK}$

7.4.1 TFT Power-On Sequence

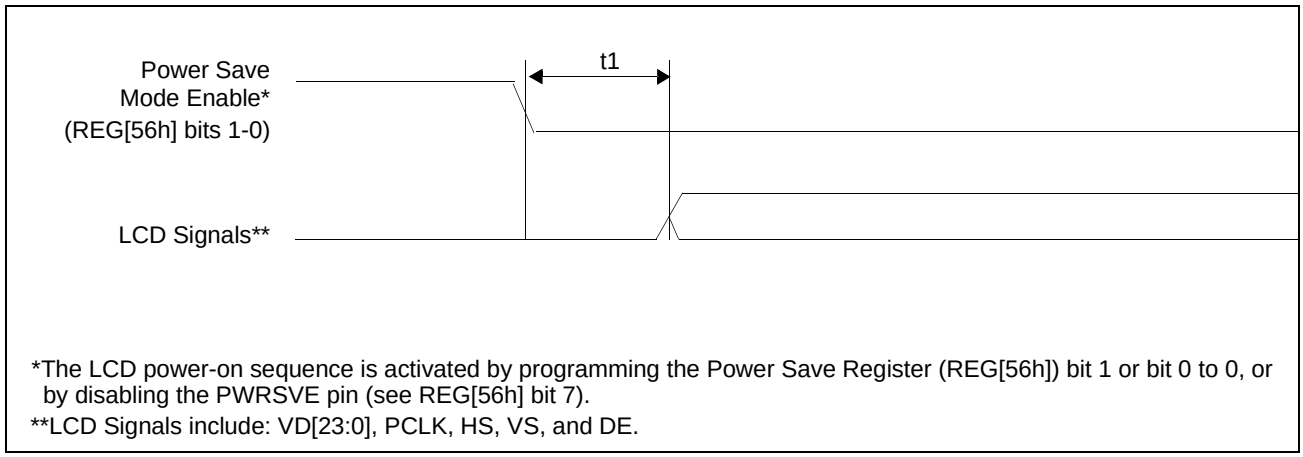
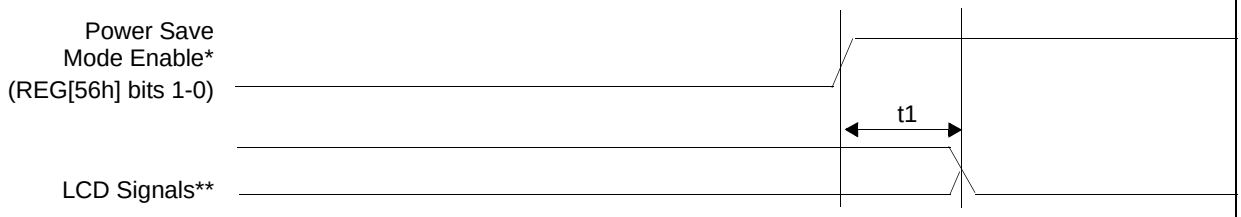


Figure 7-8: TFT Power-On Sequence Timing

Table 7-7: TFT Power-On Sequence Timing

Symbol	Parameter	Min	Max	Units
t1	Power Save Mode disabled to LCD signals active	0	20	ns

7.4.2 TFT Power-Off Sequence



*The LCD power-off sequence is activated by programming the Power Save Register (REG[56h]) bit 1 or bit 0 to 1, or by enabling the PWRSVE pin (see REG[56h] bit 7).
**LCD Signals include: VD[23:0], PCLK, HS, VS, and DE.

Figure 7-9: TFT Power-Off Sequence Timing

Table 7-8: TFT Power-Off Sequence Timing

Symbol	Parameter	Min	Max	Units
t1	Power Save Mode enabled to LCD signals low	0	20	ns

7.4.3 Generic 18/24-Bit TFT Panel Timing

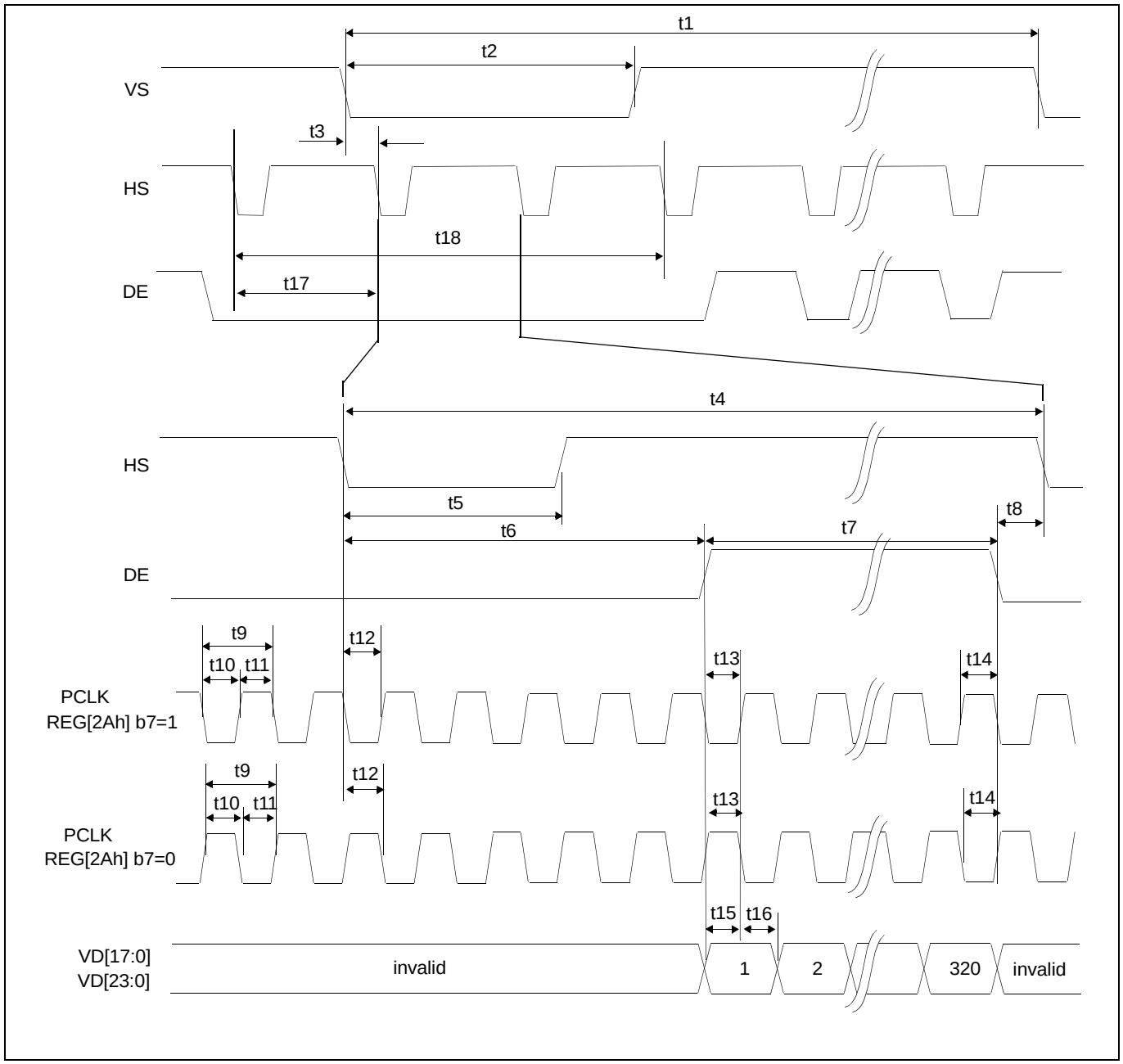


Figure 7-10: 18/24-Bit TFT A.C. Timing

Note

HS, VS, PCLK all have Polarity Select bits via registers

Table 7-9: 18/24-Bit TFT A.C. Timing

Symbol	Parameter	Min	Typ	Max	Units
t1	VS cycle time	—	VDISP + VNDP	—	Lines
t2	VS pulse width low	—	VSW	—	Lines
t3	VS falling edge to HS falling edge phase difference	—	HPS	—	Ts
t4	HS cycle time	—	HDISP + HNDP	—	Ts
t5	HS pulse width low	—	HSW	—	Ts
t6	HS Falling edge to DE active	—	HNDP-HPS	—	Ts
t7	DE pulse width	—	HDISP	—	Ts
t8	DE falling edge to HS falling edge	—	HPS	—	Ts
t9	PCLK period	1	—	—	Ts
t10	PCLK pulse width low	0.5	—	—	Ts
t11	PCLK pulse width high	0.5	—	—	Ts
t12	HS setup to PCLK falling edge	0.5	—	—	Ts
t13	DE to PCLK rising edge setup time	0.5	—	—	Ts
t14	DE hold from PCLK rising edge	0.5	—	—	Ts
t15	Data setup to PCLK rising edge	0.5	—	—	Ts
t16	Data hold from PCLK rising edge	0.5	—	—	Ts
t17	DE Stop setup to VS start	—	VPS	—	Ts
t18	Vertical Non-Display Period	—	VNDP	—	Ts

1. Ts = pixel clock period

Note

In 24-bit mode, the data is always guaranteed to be launched on the correct edge of PCLK. In this mode, the frequency of PCLK is ½ the programmed internal value. If it is desired that HS and VS are always launched on the same edge of PCLK as the data, then HNDP, HSW, and HSS should be programmed with even values.

8 Memory

The S1D13743 contains 464K bytes of embedded SRAM. The SRAM consists of two banks, the first is 304K bytes and the second is 160K bytes in size, each bank being mapped at contiguous addresses.

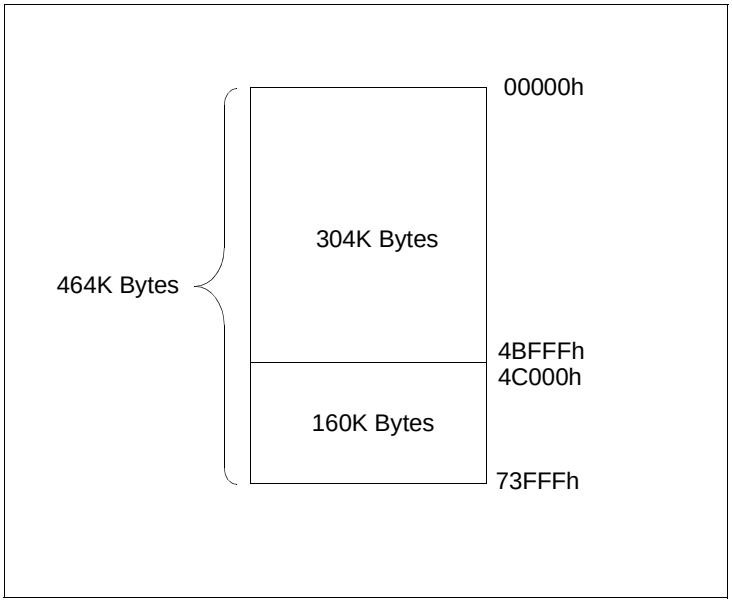


Figure 8-1: S1D13743 Physical Memory

All data written into memory, regardless of input data format, is in RGB 8:8:8 format. The following tables show how the pixel data is stored in the S1D13743 memory.

Table 8-1: Memory Map for Single Buffer (REG[36h] bit 6 = 0b)

Memory Address	Description
00000h	green [7:0] for pixel 1
00001h	red [7:0] for pixel 1
00002h	green [7:0] for pixel 2
00003h	red [7:0] for pixel 2
• • •	• • •
4C000h	blue [7:0] for pixel 1
4C001h	blue [7:0] for pixel 2
• • • 73FFFh	• • • •

Table 8-2: Memory Map for Double Buffer (REG[36h] bit 6 = 1b)

Memory Address	Description
00000h	green [7:0] for pixel 1, buffer 1
00001h	red [7:0] for pixel 1, buffer 1
00002h	green [7:0] for pixel 2, buffer 1
00003h	red [7:0] for pixel 2, buffer 1
• • •	• • •
26000h	green [7:0] for pixel 1, buffer 2
26001h	red [7:0] for pixel 1, buffer 2
26002h	green [7:0] for pixel 2, buffer 2
26003h	red [7:0] for pixel 2, buffer 2
• • •	• • •
4C000h	blue [7:0] for pixel 1, buffer 1
4C001h	blue [7:0] for pixel 2, buffer 1
• • •	• • •
60000h	blue [7:0] for pixel 1, buffer 2
60001h	blue [7:0] for pixel 2, buffer 2
• • • 73FFFh	• • • •

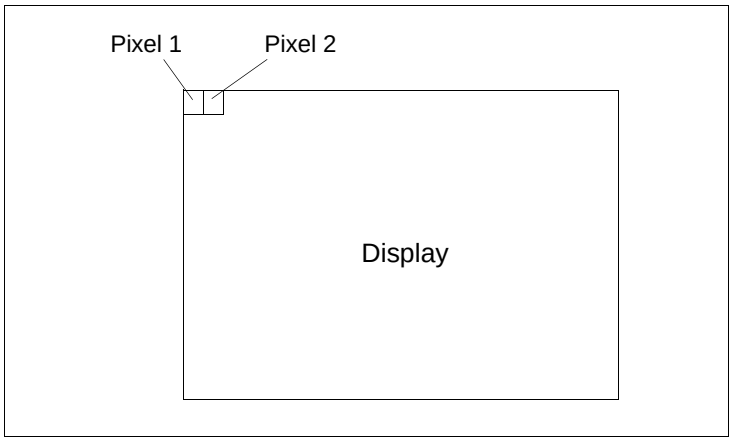


Figure 8-2: Display Pixel Position

9 Clocks

9.1 Clock Descriptions

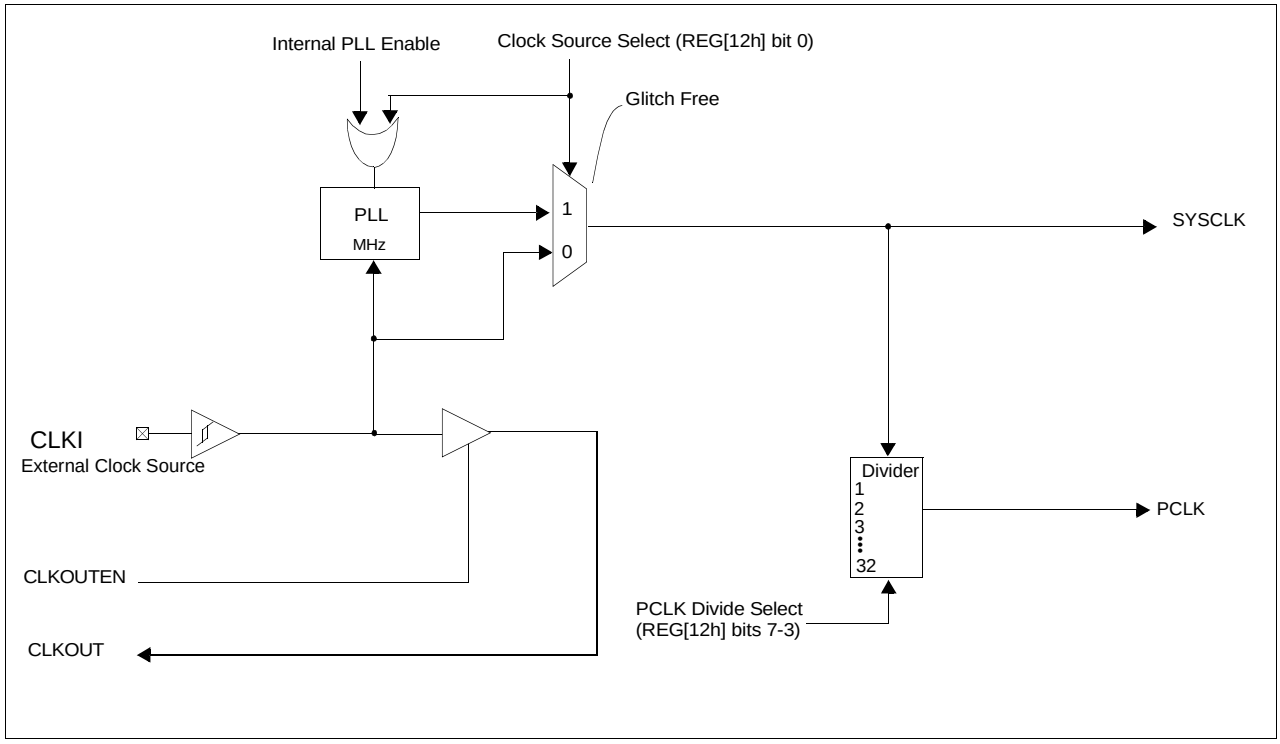


Figure 9-1: S1D13743 Clock Block Diagram

9.2 PLL Block Diagram

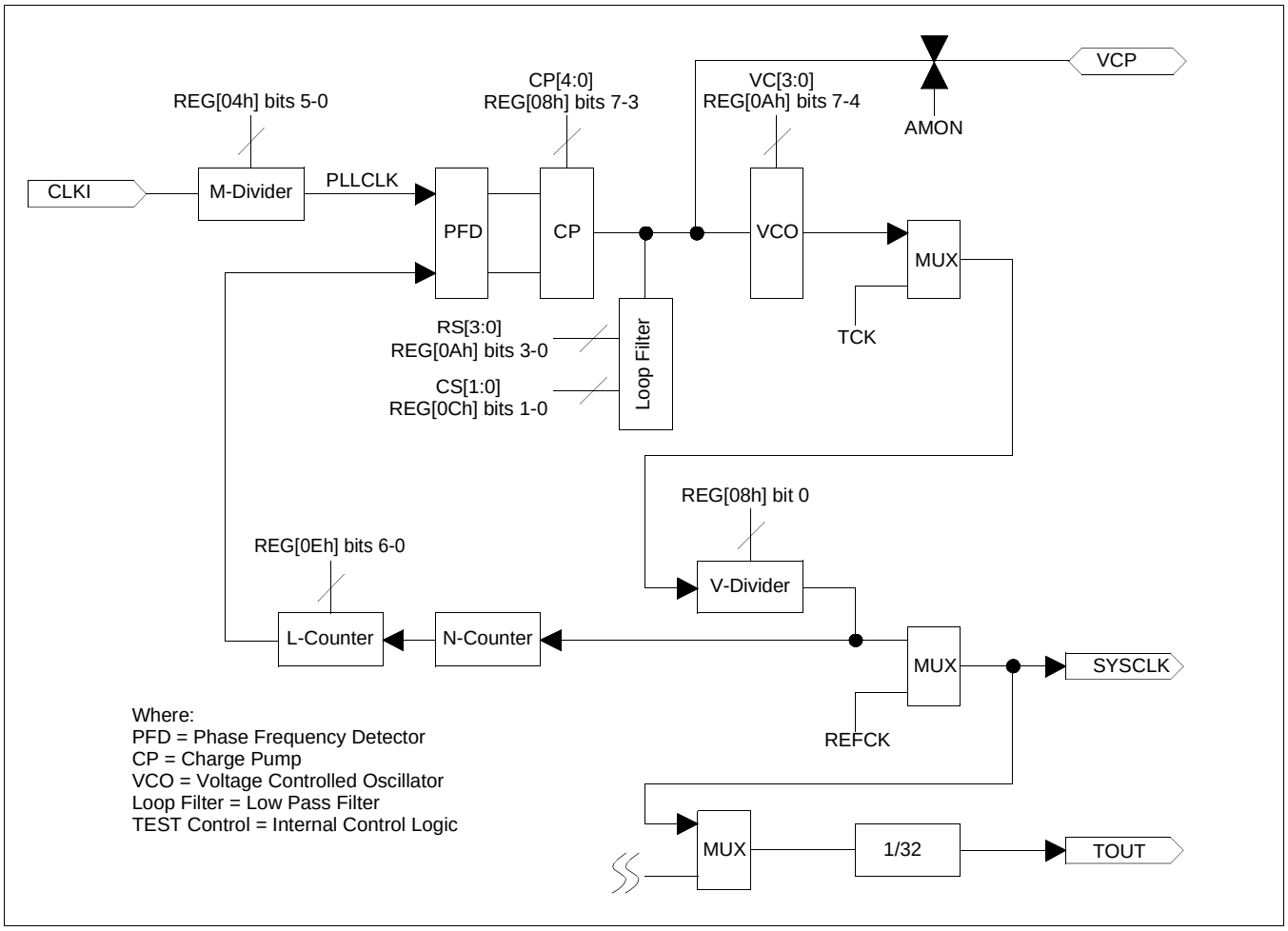


Figure 9-2: PLL Block Diagram

9.3 Clocks versus Functions

The following table summarizes the internal clocks that are required for various S1D13743 functions.

Table 9-1: Internal Clock Requirements

Function	Internal SYSCLK	Internal PCLK
Register Read/Write	No	No
Memory Read/Write	Yes	No
Look-Up Table Register Read/Write	Yes	No
Power Save	No	No
LCD Output	Yes	Yes

Note

Register accesses do not require an internal clock as the S1D13743 creates a clock from the bus cycle alone.

9.4 Setting SYSCLK and PCLK

The period of the system clock, TSYSCLK, must be set such that it falls within the following range:

For PLL: $15.03ns < T_{SYSCLK} < (T_{BBC} - 0.976) \times 0.485ns$
For CLKI: $14.58ns < T_{SYSCLK} < (T_{BBC} - 0.976) \times 0.5ns$

where T_{BBC} is the minimum back-to-back cycle time of the Intel 80 Interface.

For example, if the minimum back-to-back cycle time of the Intel 80 Interface is 47.5ns, then:

For PLL: $15.03ns < T_{SYSCLK} < 22.584ns$
For CLKI: $14.58ns < T_{SYSCLK} < 23.262ns$

Therefore,

For PLL: $44.28MHz < f_{SYSCLK} < 66.53MHz$
For CLKI: $42.99MHz < f_{SYSCLK} < 68.59MHz$

Care should be taken when setting T_{SYSCLK} so that the desired PCLK frequency, f_{PCLK}, can be achieved. PCLK is an integer divided version of SYSCLK. The following graph shows the suggested setting for SYSCLK for a given value of PCLK for T_{BBC} = 47.5ns.

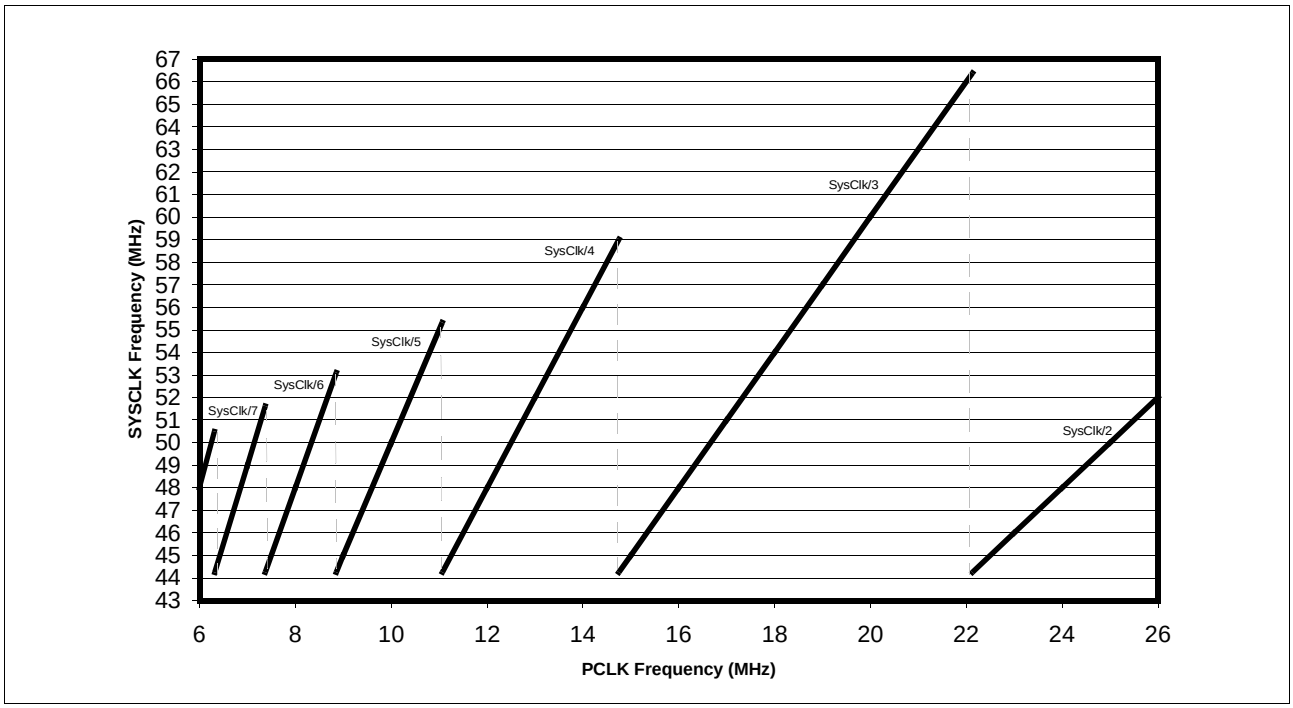


Figure 9-3: Setting of SYSCLK for a Desired PCLK

10 Registers

This section discusses how and where to access the S1D13743 registers. It also provides detailed information about the layout and usage of each register.

Burst data writes to the register space are supported for all register write accesses, except write accesses to the Memory Data Port (REG[48h] ~ REG[49h]) and the Gamma Correction Table Data Register [REG[54h]). All writes to these registers will auto-increment the internal memory address only.

10.1 Register Mapping

All registers and memory are accessed via the Intel 80 interface. All accesses are 8-bit only except for the Memory Data Port (REG[48h ~ 49h]) which is accessed according to the configuration of the CNF1 pin (16-bit for CNF1 = 1b, 8-bit for CFN1 = 0b). For further information on this setting, see Section 4.3, “Summary of Configuration Options” on page 18.

10.2 Register Set

The S1D13743 registers are listed in the following table.

Table 10-1: S1D13743 Register Set

10.3 Register Descriptions

All reserved bits must be set to the default value. Writing a non-default value to a reserved bit may produce undefined results. Bits marked as n/a have no hardware effect. Unless specified otherwise, all register bits are set to 0b during power-on reset.

10.3.1 Read-Only Configuration Registers

REG[00h] Revision Code Register
Default = 98h — Read Only

7	6	5	4	3	2	1	0
Product Code bits 5-0						Revision Code bits 1-0	

bits 7-2 Product Code bits [5:0] (Read Only)
These read-only bits indicate the product code. The product code for the S1D13743 is 100110b.

bits 1-0 Revision Code bits [1:0] (Read Only)
These read-only bits indicates the revision code. The revision code is 00b.

REG[02h] Configuration Readback Register
Default = xxh — Read Only

7	6	5	4	3	2	1	0
n/a					CNF2 Status	CNF1 Status	CNF0 Status

bits 2-0 CNF[2:0] Status (Read Only)
These read-only status bits return the status of the configuration pins CNF[2:0]. For details on CNF[2:0] functionality, see Section 4.3, “Summary of Configuration Options” on page 18.

10.3.2 Clock Configuration Registers

REG[04h] PLL M-Divider Register
Default = 00h — Read/Write

PLL Lock (RO)	n/a	M-Divider bits 5-0					
7	6	5	4	3	2	1	0

bit 7 PLL Lock (Read Only)
This bit indicates the status of the PLL output.
When this bit = 0, the PLL output is not stable. In this state read/write access to the display buffer is prohibited.
When this bit = 1, the PLL output is stable.

bits 5-0 M-Divider bits [5:0]
These bits determine the divide ratio between CLKI and the actual input clock to the PLL

Note
The internal input clock to the PLL (PLLCLK) must be between 1 MHz and 2 MHz. Depending on CLKI, these bits will have to be set accordingly.

Note
Values higher than 20h are not allowed.

Table 10-2: PLL M-Divide Selection

REG[04h] Bits 5-0	M-Divide Ratio
0h	1:1
01h	2:1
02h	3:1
03h	4:1
• • •	• • •
20h	33:1
21h to 3Fh	Reserved

REG[06h] PLL Setting Register 0
Default = 00h Read/Write

PLL Setting Register 0 bits 7-0							
7	6	5	4	3	2	1	0

This register must be programmed with the value F8h.

REG[08h] PLL Setting Register 1
Default = 00h Read/Write

PLL Setting Register 1 bits 7-0							
7	6	5	4	3	2	1	0

This register must be programmed with the value 80h.

REG[0Ah] PLL Setting Register 2
Default = 00h Read/Write

PLL Setting Register 2 bits 7-0							
7	6	5	4	3	2	1	0

This register must be programmed with the value 28h.

REG[0Ch] PLL Setting Register 3
Default = 00h Read/Write

PLL Setting Register 3 bits 7-0							
7	6	5	4	3	2	1	0

This register must be programmed with the value 00h.

REG[0Eh] PLL Setting Register 4
Default = 00h Read/Write

n/a	L-Counter bits 6-0						
7	6	5	4	3	2	1	0

bits 6-0 L-Counter bits [6:0]
These bits are used to configure the PLL Output (in MHz) and must be set according to the following formula.

PLL Output = (L-Counter + 1) x PLLCLK
= LL x PLLCLK

Where:
PLL Output is the desired PLL output frequency (in MHz).
L-Counter is the value of this register (in decimal).
PLLCLK is the internal input clock to the PLL (in MHz).

Table 10-3 PLL Setting Example

Target Frequency (MHz)	LL	CLKI Input Clock (MHz)	M-Divider REG[04h] bits 5-0	M-Divide Ratio	PLLCLK (MHz)	POUT (MHz)
53	53	12	0Bh	12:1	1.0	53
60	60	12	0Bh	12:1	1.0	60
•	•	•	•	•	•	•
53	53	19.2	12h	19:1	1.0105	53.53
60	60	19.2	12h	19:1	1.0105	60.63

REG[10h]
Default = 00h Read/Write

n/a							
7	6	5	4	3	2	1	0

Writes to this register have no effect on hardware. During Auto Increment, a dummy write must be performed to this register.

REG[12h] Clock Source Select Register
Default = 00h — Read/Write

PCLK Divide Select bits 4-0					n/a		SYSCLK Source Select
7	6	5	4	3	2	1	0

bits 7-3 PCLK Divide Select bits [4:0]

These bits specify the divide ratio for the panel clock (PCLK) frequency. The clock source for PCLK is SYSCLK.

All resulting clock frequencies will maintain a 50/50 duty cycle regardless of divide ratio.

Table 10-4 PCLK Divide Ratio Selection

REG[12h] bits 7-3	PCLK Divide Ratio	REG[12h] bits 7-3	PCLK Divide Ratio
00000b	Reserved	10000b	17:1
00001b	2:1	10001b	18:1
00010b	3:1	10010b	19:1
00011b	4:1	10011b	20:1
00100b	5:1	10100b	21:1
00101b	6:1	10101b	22:1
00110b	7:1	10110b	23:1
00111b	8:1	10111b	24:1
01000b	9:1	11000b	25:1
01001b	10:1	11001b	26:1
01010b	11:1	11010b	27:1
01011b	12:1	11011b	28:1
01100b	13:1	11100b	29:1
01101b	14:1	11101b	30:1
01110b	15:1	11110b	31:1
01111b	16:1	11111b	32:1

bit 0 SYSCLK Source Select

This bit selects the source of the system clock (SYSCLK) for the S1D13743.
When this bit = 0, the SYSCLK source is the external CLKI input.
When this bit = 1, the SYSCLK source is the internal PLL.

If the PLL is selected as the SYSCLK source (REG[12h] bit 0 = 1b), the PLL must be configured using REG[06h], REG[08h], REG[0Ah], REG[0Ch], REG[0Eh] and REG[10h] before setting these bits.

Note

The PLL output will become stable after 10ms. The display memory and the Gamma Correction Table must not be accessed before PLL output is stable. The PLL Lock bit, REG[04h] bit 7, can be used to determine if the PLL output is stable.

10.3.3 Panel Configuration Registers

REG[14h] Panel Type Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
VD Data Swap	n/a						Panel Data Width

bit 7 VD Data Swap
This bit determines whether the panel data lines (VD[23:0]) are swapped. If enabled, the data swap is from the msb to the lsb on the active output pins as shown in Table 5-2: “LCD Interface Data Pin Mapping for 24-bit Panels,” on page 20 and Table 5-3: “LCD Interface Data Pin Mapping for 18-bit Panels,” on page 20.
When this bit = 0, the data lines are normal (i.e. output pin VD23 = VD23, etc.).
When this bit = 1, the data lines are swapped (i.e. output pin VD23 = VD0, etc.).

bit 0 Panel Data Width
This bit specifies the data width for the LCD interface.
When this bit = 0, the LCD interface is configured as 18-bit (1 pixel / clock).
When this bit = 1, the LCD interface is configured as 24-bit (1 pixel / clock).

REG[16h] Horizontal Display Width Register (HDISP)
Default = 01h — Read/Write

7	6	5	4	3	2	1	0
n/a	Horizontal Display Width bits 6-0						

bits 6-0 Horizontal Display Width bits [6:0]
These bits specify the Horizontal Display Width (HDISP) for the LCD panel, in 8 pixel resolution.

HDISP in number of pixels = (REG[16h] bits 6-0) × 8

Note
The minimum Horizontal Display Width is 8 pixels (REG[16h] bits 6-0 = 01h).

REG[18h] Horizontal Non-Display Period Register (HNDP)
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a	Horizontal Non-Display Period bits 6-0						

bits 6-0 Horizontal Non-Display Period bits [6:0]
These bits specify the Horizontal Non-Display Period (HNDP), in pixels.

HNDP in pixels = REG[18h] bits 6-0

Note
The minimum Horizontal Non-Display Period is 3 Pixels (REG[18h] bits 6-0 = 03h).
HS Start + HS Width <= HNDP

REG[1Ah] Vertical Display Height Register 0 (VDISP)
Default = 01h — Read/Write

7	6	5	4	3	2	1	0
Vertical Display Height bits 7-0							

REG[1Ch] Vertical Display Height Register 1 (VDISP)
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a						Vertical Display Height bits 9-8	

REG[1Ch] bits 1-0
REG[1Ah] bits 7-0 Vertical Display Height bits [9:0]

These bits specify the Vertical Display Height (VDISP) for the LCD panel, in lines.

VDISP in lines = (REG[1Ch] bits 1-0, REG[1Ah] bits 7-0)

Note

The minimum Vertical Display Height is 1 line (REG[1Ch] bits 1-0, REG[1Ah] bits 7-0 = 001h).

REG[1Eh] Vertical Non-Display Period Register (VNDP)
Default = 01h — Read/Write

7	6	5	4	3	2	1	0
Vertical Non-Display Period bits 7-0							

bits 7-0 Vertical Non-Display Period bits [7:0]

These bits specify the Vertical Non-Display Period (VNDP) for the LCD panel, in lines.

VNDP in lines = REG[1Eh] bits 7-0

Note

The minimum Vertical Non-Display Period is 2 lines (REG[1Eh] bits 7-0 = 02h).

REG[20h] HS Pulse Width Register (HSW)
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
HS Pulse Polarity	HS Pulse Width bits 6-0						

bit 7 HS Pulse Polarity

This bit selects the polarity of the horizontal sync signal. This bit is set according to the horizontal sync signal of the panel.

When this bit = 0, the horizontal sync signal is active low.

When this bit = 1, the horizontal sync signal is active high.

bits 6-0 HS Pulse Width bits [6:0]

These bits specify the width of the horizontal sync signal for the LCD panel (HSW), in pixels. The horizontal sync signal is typically HS, depending on the panel type.

HSW in pixels = REG[20h] bits 6-0

REG[22h] HS Pulse Start Position Register (HPS)
Default = 00h Read/Write

7	6	5	4	3	2	1	0
n/a	HS Pulse Start Position bits 6-0						

bits 6-0 HS Pulse Start Position bits [6:0]
These bits specify the start position of the horizontal sync signal with respect to the start of Horizontal Non-Display period (HPS), in pixels.
HPS in pixels = REG[22h] bits 6-0

REG[24h] VS Pulse Width Register (VSW)
Default = 00h Read/Write

7	6	5	4	3	2	1	0
VS Pulse Polarity	n/a	VS Pulse Width bits 5-0					

bit 7 VS Pulse Polarity
This bit selects the polarity of the vertical sync signal. This bit is set according to the vertical sync signal of the panel.
When this bit = 0, the vertical sync signal is active low.
When this bit = 1, the vertical sync signal is active high.

bits 5-0 VS Pulse Width bits [5:0]
These bits specify the width of vertical sync signal for the panel (VSW), in lines. The vertical sync signal is typically VS, depending on the panel type.
VSW in lines = REG[24h] bits 5-0

REG[26h] VS Pulse Start Position Register (VPS)
Default = 00h Read/Write

7	6	5	4	3	2	1	0
VS Pulse Start Position bits 7-0							

bits 7-0 VS Pulse Start Position bits [7:0]
These bits specify the start position of the vertical sync signal with respect to the start of Vertical Non-Display period (VPS), in lines.
VPS in lines = REG[26h] bits 7-0

REG[28h] PCLK Polarity Register
Default = 00h Read/Write

7	6	5	4	3	2	1	0
PCLK Polarity	n/a						

bit 7 PCLK Polarity
This bit selects the polarity of PCLK.
When this bit = 0, data is output on the rising edge of PCLK.
When this bit = 1, data is output on the falling edge of PCLK.

10.3.4 Input Mode Register

REG[2Ah] Input Mode Register							
Default = 01h							Read/Write
n/a				Input Data Format bits 3-0			
7	6	5	4	3	2	1	0

bits 3-0 Input Data Format bits [3:0]

These bits select the input data format. For further information on Input Data Format and Memory Data Format, see Section 13, “Intel 80, 8-bit Interface Color Formats” on page 75, Section 14, “Intel 80, 16-bit Interface Color Formats” on page 78 and Section 15, “YUV Timing” on page 83.

Table 10-5: Input Data Type Selection

REG[2Ah] bits 3-0	Input Data Type
0000b	Reserved
0001b	RGB 5:6:5
0010b	RGB 6:6:6 Mode 1
0011b	RGB 8:8:8 Mode 1
0100b	Reserved
0101b	Reserved
0110b	RGB 6:6:6 Mode 2
0111b	RGB 8:8:8 Mode 2
1000b	YUV 4:2:2
1001b	YUV 4:2:0
1010b ~ 1111b	Reserved

Note
All input data is stored as 24 bpp.

Note
For YUV 4:2:2 and YUV 4:2:0 settings, the image width must be a multiple of 2 and 4 respectively. For YUV 4:2:0 the height must be a multiple of 2.
For RGB 6:6:6 and RGB 8:8:8 Mode 1, if the image width is odd, the red pixel data in the last word in each line will be ignored. The red pixel data will need to be re-written on the following transfer along with the green data. See Figure 14-2: “18 bpp Mode 1 (R 6-bit, G 6-bit, B 6-bit), 262,144 colors,” on page 79 or Figure 14-4: “24 bpp Mode 1 (R 8-bit, G 8-bit, B 8-bit), 16,777,216 colors,” on page 81.

Note
RGB 6:6:6 mode 2 and RGB 8:8:8 mode 2 settings are not available for 8-bit host interface.

REG[2Ch] Input YUV/RGB Translate Mode Register 0
Default = 00h Read/Write

Reserved	YRC Reset	UV Fix bits 1-0		n/a			
7	6	5	4	3	2	1	0

bit 7 Reserved
The default value for this bit is 0b.

bit 6 YRC Reset
This bit performs a software reset of the YRC (YUV to RGB Converter). To perform a reset, write a 1b to enter reset, and then write a 0b to return from the reset state.
For Reads:
When this bit = 0, the YRC is not in a reset state.
When this bit = 1, the YRC is in a reset state.
For Writes:
Writing a 0 to this bit returns the YRC from the reset state.
Writing a 1 to this bit initiates a software reset of the YRC.

bits 5-4 UV Fix Select bits [1:0]
These bits control the UV input to the YRC (YUV to RGB Converter).

Table 10-6: UV Fix Selection

REG[2Ch] Bits 5-4	UV Input to the YRC
00b	Original U data, original V data
01b	U data = REG[32h] bits 7-0, original V data
10b	Original U data, V data = REG[34h] bits 7-0
11b	U data = REG[32h] bits 7-0, V data = REG[34h] bits 7-0

REG[2Eh] Input YUV/RGB Translate Mode Register 1
Default = 05h Read/Write

Reserved		YUV Input Data Type Select bits 1-0		Reserved	YUV/RGB Transfer Mode bits 2-0		
7	6	5	4	3	2	1	0

bits 7-6 Reserved
The default value for these bits is 00b.

bits 5-4 YUV Input Data Type Select bits [1:0]
These bits specify the data type of the YUV input to the YUV to RGB Converter (YRC).

Table 10-7: YUV Data Type Selection

REG[2Eh] bits 5-4	YRC Input Data Range
00b	0 ≤ Y ≤ 255 -128 ≤ U ≤ 127 -128 ≤ V ≤ 127
01b	16 ≤ Y ≤ 235 -113 ≤ U ≤ 112 -113 ≤ V ≤ 112
10b	0 ≤ Y ≤ 255 0 ≤ U ≤ 255 0 ≤ V ≤ 255
11b	16 ≤ Y ≤ 235 16 ≤ U ≤ 240 16 ≤ V ≤ 240

bit 3 Reserved
The default value for this bit is 0b.

bits 2-0 YUV/RGB Transfer Mode bits [2:0]

These bits specify the YUV/RGB Transfer mode. Recommended settings are provided for various specifications.

Table 10-8: YUV/RGB Transfer Mode Selection

REG[2Eh] bits 2-0	YUV/RGB Specification
000b	Reserved
001b	Recommended for ITU-R BT.709
010b	Reserved
011b	Reserved
100b	Recommended for ITU-R BT.470-6 System M
101b (Default)	Recommended for ITU-R BT.470-6 System B, G (Recommended for ITU-R BT.601-5)
110b	SMPTE 170M
111b	SMPTE 240M(1987)

REG[30h] U Data Fix Register
Default = 00h Read/Write

U Data Fix bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 U Data Fix bits [7:0]

These bits only have an effect when the UV Fix Select bits are set to 01b or 11b (REG[2Ch] bits 5-4 = 01b or 11b). The U data input to the YRC (YUV to RGB Converter) is fixed to the value of these bits.

REG[32h] V Data Fix Register
Default = 00h Read/Write

V Data Fix bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 V Data Fix bits [7:0]

These bits only have an effect when the UV Fix Select bits are set to 10b or 11b (REG[2Ch] bits 5-4 = 10b or 11b). The V data input to the YRC (YUV to RGB Converter) is fixed to the value of these bits.

10.3.5 Display Mode Registers

REG[34h] Display Mode Register							
Default = 08h							Read/Write
Display Blank	FRM Mode Select bits 2-0			Reserved	n/a	SwivelView Mode Select bits 1-0	
7	6	5	4	3	2	1	0

bit 7 Display Blank
This bit blanks the display by disabling the LCD display pipeline and forcing all LCD data outputs to zero.
When this bit = 0, the LCD display pipeline is enabled and the display is active.
When this bit = 1, the LCD display pipeline is disabled and the display is blanked.

bits 6-4 FRM Mode Select bits [2:0]
These bits select the FRM mode.

Note
When the output is 24 bpp, set REG[34] bits 6-4 = 000b

Table 10-9: FRM Mode Selection

REG[34h] bits 6-4	FRM Mode Selected
000b	Normal mode
001b	18 bpp Bypass
010b	FRM
011b	Reserved
100b	Dithering
101b	Reserved
110b	FRM + Dithering
111b	Reserved

bit 3 Reserved
The default value for this bit is 1b.

bits 1-0 Window SwivelView Mode Select bits [1:0]

These bits select the SwivelView™ orientation that will be applied to the window. Each window on the active display can have independent rotation, as the rotation is performed prior to writing to the display buffer.

Table 10-10: SwivelView Mode Select Options

REG[34h] bits 1-0	SwivelView Orientation
00b	0° (Normal)
01b	90°
10b	180°
11b	270°

REG[36h] Special Effects Register
Default = 00h Read/Write

Window Data Type	Double Buffer Enable	n/a				Window Pixel Sizing bits 1-0	
7	6	5	4	3	2	1	0

bit 7 Window Data Type

This bit is used in conjunction with the Double Buffer Enable bit (REG[36h] bit 6) and determines whether the data being input from the host will be double-buffered. This bit must be set before the window data is written, as the window coordinates will be latched internally to be used by the display pipe during display cycles.

When this bit = 0, the data being written from the Host is intended for single buffer only.

When this bit = 1, the data being written from the Host is intended for double buffer operation.

Table 10-11: Window Data Type / Buffer Selection

REG[36h] Bit 7	REG[36h] Bit 6	Use Case
0b	0b	Single buffered window with no double buffering anywhere on the display.
0b	1b	Use this to write a single buffered window while preventing tearing in a previously defined double buffered window.
1b	0b	Reserved
1b	1b	Use this to write data to be double buffered.

Note

While double buffering is enabled, the window coordinates should not be modified.

Note

If the Input Data Format is YUV 4:2:0 (REG[2Ah] bits 3-0 = 1001b), the Window Data Type bit must not be changed while the YYC is busy (REG[58h] bit 4 = 1b).

bit 6 Double Buffer Enable

This bit is used in conjunction with the Window Data Type bit (REG[36h] bit 7) and controls the Double Buffer architecture. Double buffering is intended to prevent visual tearing when updating the display from streaming input sources. This bit must be set before the window data is written, as the window coordinates will be latched internally to be used by the display pipe during display cycles.
When this bit = 0, the double buffer architecture is disabled.
When this bit =1, the double buffer architecture is enabled. This feature is only available if the memory size resulting from the display size and color depth will fit within the 1/2 the allowable size for the display buffer.

For a summary of Window Data Type / Double Buffer options, see Table 10-11: “Window Data Type / Buffer Selection,” on page 60.

Note
While double buffering is enabled, the window coordinates should not be modified.

Note
Only one window can be double-buffered. All other windows are single buffered.

bits 1-0 Window Pixel Sizing bits [1:0]

These bits control resizing of the window data.

These bits must be set before the window data is written, as the window coordinates will be latched internally to be used by the display pipe during display cycles.

Table 10-12: Window Pixel Sizing

REG[36h] bits 1-0	Result
00b	No Resizing
01b	Pixel Doubling
10b	Pixel Halving
11b	Reserved

Note

Only 1 active window can have pixel doubling enabled. The pixel doubling design uses horizontal and vertical averaging for smooth doubling.

The following figure provides an example of the resizing options. All resizing is performed with respect to the top left corner.

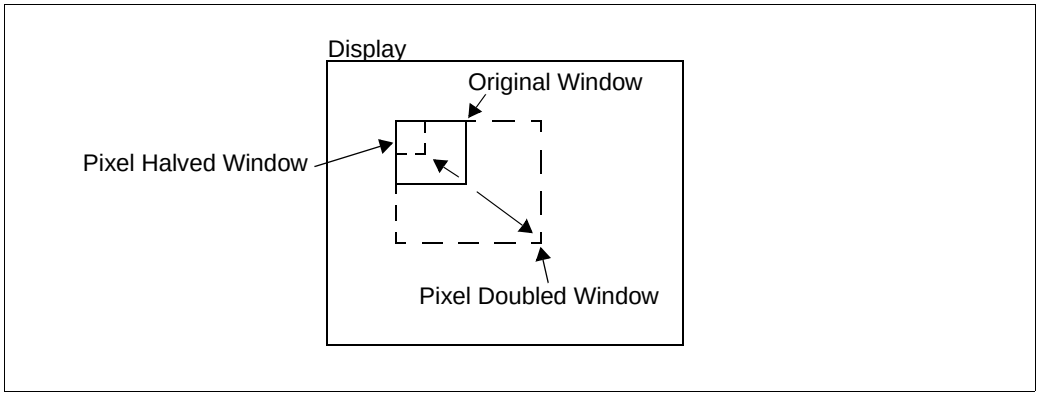


Figure 10-1: Sizing Example

Note

To disable pixel doubling for a window that is currently pixel doubled, either:

1. Overwrite any part of the pixel doubled window with a new window.
2. Write a new pixel doubled window.

10.3.6 Window Settings

REG[38h] Window X Start Position Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Window X Start Position bits 7-0							

REG[3Ah] Window X Start Position Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a						Window X Start Position bits 9-8	

REG[3Ah] bits 1-0
REG[38h] bits 7-0 Window X Start Position bits [9:0]

These bits determine the X start position of the window in relation to the top left corner of the displayed image. Even in a rotated orientation (see REG[34h] bits 1-0), the top left corner is still relative to the displayed image.

Note
When pixel doubling or pixel halving is enabled (see REG[36h] bits 1-0), these bits should be programmed with the pre-resized coordinates.

REG[3Ch] Window Y Start Position Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Window Y Start Position bits 7-0							

REG[3Eh] Window Y Start Position Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a						Window Y Start Position bits 9-8	

REG[3Eh] bits 1-0
REG[3Ch] bits 7-0 Window Y Start Position bits [9:0]

These bits determine the Y start position of the window in relation to the top left corner of the displayed image. Even in a rotated orientation (see REG[34h] bits 1-0), the top left corner is still relative to the displayed image.

Note
When pixel doubling or pixel halving is enabled (see REG[36h] bits 1-0), these registers should be programmed with the pre-resized coordinates.

REG[40h] Window X End Position Register 0
Default = 00h Read/Write

Window X End Position bits 7-0							
7	6	5	4	3	2	1	0

REG[42h] Window X End Position Register 1
Default = 00h Read/Write

n/a						Window X End Position bits 9-8	
7	6	5	4	3	2	1	0

REG[42h] bits 1-0
REG[40h] bits 7-0 Window X End Position bits [9:0]

These bits determine the X end position of the window in relation to the top left corner of the displayed image. Even in a rotated orientation (see REG[34h] bits 1-0), the top left corner is still relative to the displayed image.

Note

When pixel doubling or pixel halving is enabled (see REG[36h] bits 1-0), these registers should be programmed with the pre-resized coordinates.

REG[44h] Window Y End Position Register 0
Default = 00h Read/Write

Window Y End Position bits 7-0							
7	6	5	4	3	2	1	0

REG[46h] Window Y End Position Register 1
Default = 00h Read/Write

n/a						Window Y End Position bits 9-8	
7	6	5	4	3	2	1	0

REG[46h] bits 1-0
REG[44h] bits 7-0 Window Y End Position bits [9:0]

These bits determine the Y end position of the window in relation to the top left corner of the displayed image. Even in a rotated orientation (see REG[34h] bits 1-0), the top left corner is still relative to the displayed image.

Note

When pixel doubling or pixel halving is enabled (see REG[36h] bits 1-0), these registers should be programmed with the pre-resized coordinates.

10.3.7 Memory Access

REG[48h] Memory Data Port Register 0
Default = not applicable — Read/Write

Memory Data Port bits 7-0							
7	6	5	4	3	2	1	0

REG[49h] Memory Data Port Register 1
Default = not applicable — Read/Write

Memory Data Port bits 15-8							
7	6	5	4	3	2	1	0

REG[48h] bits 7-0 Memory Data Port bits [7:0]
These bits specify the lsb of the data word.

REG[49h] bits 15-8 Memory Data Port bits [15:8]
These bits specify the msb of the data word.

Note
If CNF1=0 (8-bit interface), REG[49h] is not used.

Note
Burst data writes are supported through these registers. Register auto-increment is automatically disabled once reaching this address. All writes to this register will auto-increment the internal memory address only.

Note
Panel dimension registers must be set before writing any window data.

Note
Upon writing the last pixel in the defined window, these bits will automatically point back to the first pixel in the window. Therefore, there is no need to re-initialize the pointers.

REG[4Ah] Memory Read Address Register 0
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Memory Read Address bits 7-0							

REG[4Ch] Memory Read Address Register 1
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Memory Read Address bits 15-8							

REG[4Eh] Memory Read Address Register 2
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a					Memory Read Address bit 18-16		

REG[4Eh] bits 2-0
REG[4Ch] bits 7-0
REG[4Ah] bits 7-0 Memory Read Address bits [18:0]

These bits are used for individual memory location reads only. Individual memory location writes are not supported.

After a completed memory access, these bits are automatically incremented.

Note

If 16-bit interface is used (CNF1 = 1), all reads will be on even byte boundaries. Memory Read Address bit 0 is ignored and internally forced to 0b.

10.3.8 Gamma Correction Registers

Note
Gamma correction is implemented as a look-up table. RGB input data (YUV input data is converted to RGB) is used to look-up the values from the programmed tables. The Gamma LUT's are placed on the display read path and the 24-bit output goes to the LCD interface.

Note
The Gamma Correction Tables should not be accessed during display period as this will result in visual anomalies. All updates to the LUTs should be performed during non-display period or when the LUTs are disabled and not in use.

REG[50h] Gamma Correction Enable Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
n/a					Look-Up Table Access Mode bits 1-0		Gamma Correction Enable

bits 2-1 Look-Up Table Access Mode bits [1:0]
These bits specify the mode used to access the Look-Up Table (LUT).

Table 10-13: Look-Up Table Access Mode

REG[50h] bits 2-1	Description
00b	Writing is done to all Red, Green, & Blue tables. Reading is done from the Red table.
01b	Reading and writing are done from/to the Red table.
10b	Reading and writing are done from/to the Green table.
11b	Reading and writing are done from/to the Blue table.

bit 0 Gamma Correction Enable
This bit controls gamma correction.
When this bit = 0, gamma correction is disabled and the input data will bypass the gamma correction look-up table.
When this bit = 1, gamma correction is enabled and the input data will go through the gamma correction look-up table.

Note
The Gamma Correction Tables should not be accessed during display period as this will result in visual anomalies. All updates to the LUTs should be performed during non-display period or when the LUTs are disabled and not in use.

REG[52h] Gamma Correction Table Index Register

Default = 00h — Read/Write

Gamma Correction Table Index bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Gamma Correction Table Index bits [7:0]

These bits specify the index of the gamma correction look-up table where the subsequent read/write will start.

REG[54h] Gamma Correction Table Data Register

Default = not applicable — Read/Write

Gamma Correction Table Data bits 7-0							
7	6	5	4	3	2	1	0

bits 7-0 Gamma Correction Table Data bits [7:0]

When writing to these bits, the index to the internal Gamma Correction Table Data is automatically incremented by 1 for each write to the Gamma Correction Table Data register. This allows the continuous writes to the Gamma Correction Table while only having to write the Gamma Correction Table Index, REG[52h], once before the first write.

Note

When performing auto-increment writes, all 256 positions of each LUT must be written.

10.3.9 Miscellaneous Registers

REG[56h] Power Save Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
PWRSVE Input Pin Function	n/a					Sleep Mode Enable/Disable	Standby Mode Enable/Disable

bit 7 PWRSVE Input Pin Function
This bit determines the functionality of the PWRSVE input pin.
When this bit = 0, the PWRSVE pin is OR'd with the Sleep Mode Enable/Disable bit (REG[56h] bit 1) and setting either to 1 will enable Sleep Mode.
When this bit = 1, the PWRSVE pin is OR'd with the Standby Mode Enable/Disable bit (REG[56h] bit 0) and setting either to 1 will enable Standby Mode.

bit 1 Sleep Mode Enable/Disable
This bit controls the Sleep power save mode. Sleep mode can also be controlled by the PWRSVE pin when REG[56h] bit 7 = 0b.
When this bit = 0, Sleep Mode is disabled (normal operation).
When this bit = 1, Sleep Mode is enabled.

When Sleep Mode is enabled, all internal blocks including the PLL are disabled.
When Sleep Mode is disabled, the PLL requires approximately 10ms lock time before any memory access should be attempted. The PLL Lock bit, REG[04h] bit 7, can be read to verify when the PLL becomes stable.

bit 0 Standby Mode Enable/Disable
This bit controls the Standby power save mode. Standby mode can also be controlled by the PWRSVE pin when REG[56h] bit 7 = 1b.
When this bit = 0, Standby Mode is disabled (normal operation).
When this bit = 1, Standby Mode is enabled.

When Standby Mode is enabled, all internal blocks are disabled except for the PLL.
When Standby Mode is disabled, the chip can be accessed immediately.

REG[58h] Non-Display Period Control / Status Register
Default = 00h — Read/Write

7	6	5	4	3	2	1	0
Vertical Non-Display Period Status (RO)	Horizontal Non-Display Period Status (RO)	VDP OR'd with HDP Status (RO)	YYC Last Line	n/a	TE Output Pin Enable	TE Output Pin Function Select bits 1-0	

bit 7 Vertical Non-Display Period Status (Read Only)
This bit indicates whether the LCD panel output is in a vertical non-display period (VNDP). VNDP is defined as the time between the last pixel on the last line of one frame to the first pixel on the first line of the next frame.
When this bit = 0, the LCD panel output is in a Vertical Display Period.
When this bit = 1, the LCD panel output is in a Vertical Non-Display Period.

bit 6 Horizontal Non-Display Period Status (Read Only)
This bit indicates whether the LCD panel output is in a horizontal non-display period (HNDP). HNDP is defined as the time between the last pixel in line n to the first pixel in line n+1.
When this bit = 0, the LCD panel output is in a Horizontal Non-Display Period.
When this bit = 1, the LCD panel output is in a Horizontal Display Period.

bit 5 VP OR'd with HDP Status (Read Only)
This bit indicates whether the LCD panel is in a display period or a non-display period.
When this bit = 0, the LCD panel is in a Display period.
When this bit = 1, the LCD panel is in either a Horizontal or Vertical Non-Display period.

bit 4 YYC Last Line
This bit indicates the status of the YYC (YUV to YUV Converter). If the Input Data Format is YUV 4:2:0 (REG[2Ah] bits 3-0 = 1001b), this bit goes high 5 MCLKs after the Intel 80 interface completes writing the last pixel of the current window. The bit goes low once the YYC returns to an idle state. At this point, a new window can be written.
When this bit = 0, the YYC is idle.
When this bit = 1, the YYC is converting YUV 4:2:0 data.

When doing back-to-back window writes with a different dimension or format, and the first window is YUV 4:2:0, this bit must be low (0) before starting to write the second window.

bit 2 TE Output Pin Enable
This bit controls the TE output pin.
When this bit = 0, the TE output pin is disabled.
When this bit = 1, the TE output pin is enabled.

bits 1-0 TE Output Pin Function Select bits [1:0]
These bits select which function is indicated by the TE output pin.

Table 10-14: TE Output Pin Function Selection

REG[58h] bits 1-0	TE Output Pin Function
00b	Reserved
01b	Horizontal Non-Display Period
10b	Vertical Non-Display Period
11b	HS OR'd with VS

10.3.10 General Purpose IO Pins Registers

REG[5Ah] General Purpose IO Pins Configuration Register 0
Default =00h — Read/Write

GPIO7 Configuration	GPIO6 Configuration	GPIO5 Configuration	GPIO4 Configuration	GPIO3 Configuration	GPIO2 Configuration	GPIO1 Configuration	GPIO0 Configuration
7	6	5	4	3	2	1	0

bits 7-0 GPIO[7:0] Configuration
These bits configure the corresponding GPIO[7:0] pin between inputs or outputs.
When this bit = 0 (normal operation), the corresponding GPIO pin is configured as an input.
When this bit = 1, the corresponding GPIO pin is configured as an output.

REG[5Ch] General Purpose IO Pins Status/Control Register 0
Default = 00h — Read/Write

GPIO7 Status	GPIO6 Status	GPIO5 Status	GPIO4 Status	GPIO3 Status	GPIO2 Status	GPIO1 Status	GPIO0 Status
7	6	5	4	3	2	1	0

bits 7-0 GPIO[7:0] Status
When the corresponding GPIO[7:0] pin is configured as an output (see REG[5Ah]), writing a 1b to this bit drives GPIOx high and writing a 0b to this bit drives GPIOx low.
When the corresponding GPIO[7:0] pin is configured as an input (see REG[5Ah]), a read from this bit returns the raw status of GPIOx.

REG[5Eh] GPIO Positive Edge Interrupt Trigger Register
Default = 00h — Read/Write

GPIO7 Positive Edge Interrupt Trigger	GPIO6 Positive Edge Interrupt Trigger	GPIO5 Positive Edge Interrupt Trigger	GPIO4 Positive Edge Interrupt Trigger	GPIO3 Positive Edge Interrupt Trigger	GPIO2 Positive Edge Interrupt Trigger	GPIO1 Positive Edge Interrupt Trigger	GPIO0 Positive Edge Interrupt Trigger
7	6	5	4	3	2	1	0

bits 7-0 GPIO[7:0] Positive Edge Interrupt Trigger
This bit determines whether the associated GPIO interrupt is triggered on the positive edge (when the GPIOx pin changes from 0 to 1).
When this bit = 0, the associated GPIO interrupt (GPIO_INT) is not triggered on the positive edge.
When this bit = 1, the associated GPIO interrupt (GPIO_INT) is triggered on the positive edge.

REG[60h] GPIO Negative Edge Interrupt Trigger Register
Default = 00h Read/Write

GPIO7 Negative Edge Interrupt Trigger	GPIO6 Negative Edge Interrupt Trigger	GPIO5 Negative Edge Interrupt Trigger	GPIO4 Negative Edge Interrupt Trigger	GPIO3 Negative Edge Interrupt Trigger	GPIO2 Negative Edge Interrupt Trigger	GPIO1 Negative Edge Interrupt Trigger	GPIO0 Negative Edge Interrupt Trigger
7	6	5	4	3	2	1	0

bits 7-0 GPIO[7:0] Negative Edge Interrupt Trigger

This bit determines whether the associated GPIO interrupt is triggered on the negative edge (when the GPIOx pin changes from 1 to 0).

When this bit = 0, the associated GPIOx interrupt (GPIO_INT) is not triggered on the negative edge.

When this bit = 1, the associated GPIOx interrupt (GPIO_INT) is triggered on the negative edge.

REG[62h] GPIO Interrupt Status Register
Default = 00h Read/Write

GPIO7 Interrupt Status	GPIO6 Interrupt Status	GPIO5 Interrupt Status	GPIO4 Interrupt Status	GPIO3 Interrupt Status	GPIO2 Interrupt Status	GPIO1 Interrupt Status	GPIO0 Interrupt Status
7	6	5	4	3	2	1	0

bits 7-0 GPIO[7:0] Interrupt Status

If GPIOs are configured to generate an Interrupt (see REG[5Eh] and REG[60h]), these status bits will indicate which GPIO generated the interrupt.

To clear the corresponding GPIO[7:0] Interrupt Status bit, write a 1b then a 0b to the bit.

REG[64h] GPIO Pull-down Control Register
Default = FFh Read/Write

GPIO7 Pull-down Control	GPIO6 Pull-down Control	GPIO5 Pull-down Control	GPIO4 Pull-down Control	GPIO3 Pull-down Control	GPIO2 Pull-down Control	GPIO1 Pull-down Control	GPIO0 Pull-down Control
7	6	5	4	3	2	1	0

bits 7-0 GPIO[7:0] Pull-down Control

All GPIO[7:0] pins have internal pull-down resistors. These bits individually control the state of the corresponding pull-down resistor.

When the bit = 0, the pull-down resistor for the corresponding GPIO pin is inactive.

When the bit = 1, the pull-down resistor for the corresponding GPIO pin is active.

11 Frame Rate Calculation

The following formula is used to calculate the display frame rate.

$$\text{FrameRate} = \frac{f_{PCLK}}{(HT) \times (VT)}$$

Where:

f_{PCLK} = PClk frequency (Hz)

HT = Horizontal Total
= Horizontal Display Width + Horizontal Non-Display Period

VT = Vertical Total
= Vertical Display Height + Vertical Non-Display Period

Note

For definitions of panel timing parameters, see Section 7.4, “Display Interface” on page 33.

12 RGB Input Data Conversion

All RGB input data is converted to RGB 8:8:8 and stored as follows. For further information see Section 8, “Memory” on page 38.

Table 12-1: RGB 5:6:5 to RGB 8:8:8 Conversion Memory Format

Pixel Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2	R4	R3	R2	R1	R0	R4	R3	R2
1	G5	G4	G3	G2	G1	G0	G5	G4
0	B4	B3	B2	B1	B0	B4	B3	B2

Table 12-2: RGB 6:6:6 to RGB 8:8:8 Conversion Memory Format

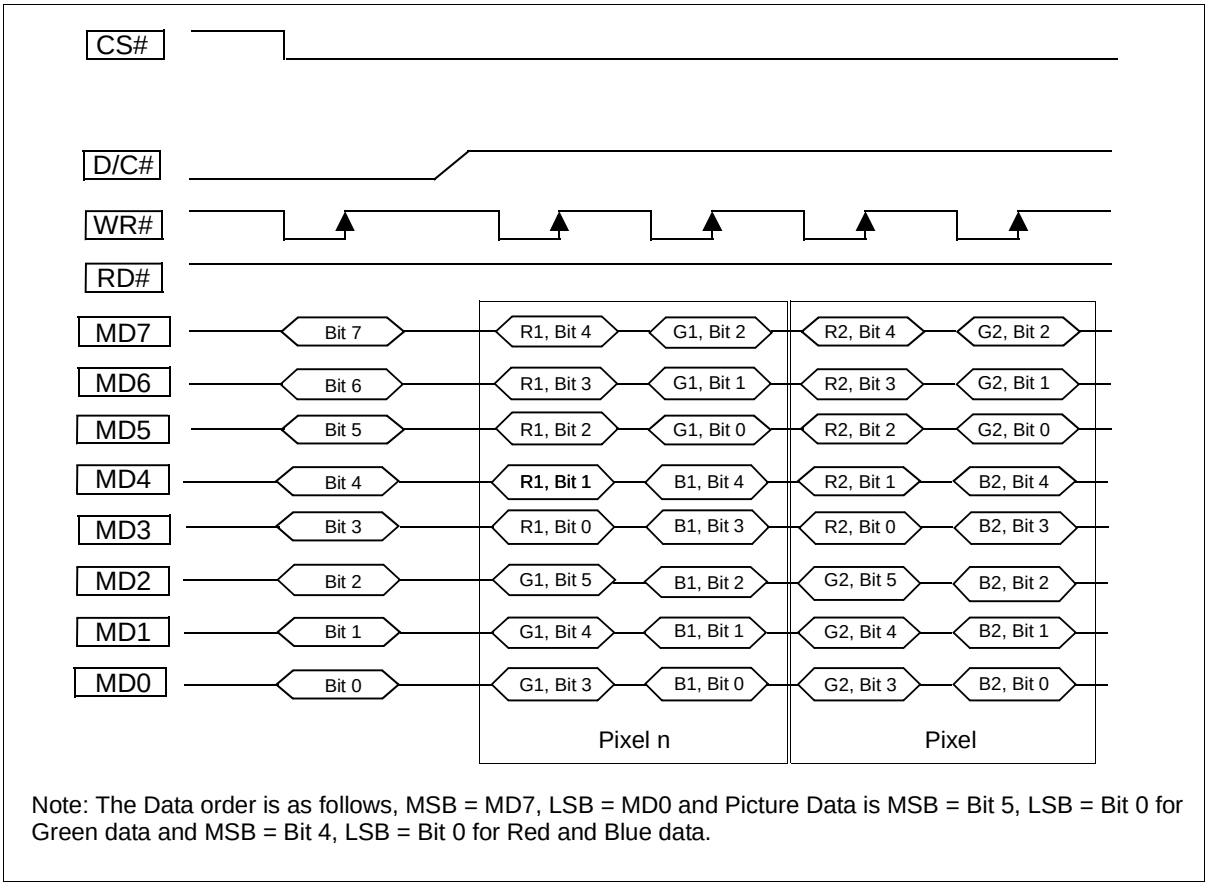
Pixel Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2	R5	R4	R3	R2	R1	R0	R5	R4
1	G5	G4	G3	G2	G1	G0	G5	G4
0	B5	B4	B3	B2	B1	B0	B5	B4

Table 12-3: RGB 8:8:8 Memory Format

Pixel Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2	R7	R6	R5	R4	R3	R2	R1	R0
1	G7	G6	G5	G4	G3	G2	G1	G0
0	B7	B6	B5	B4	B3	B2	B1	B0

13 Intel 80, 8-bit Interface Color Formats

13.1 16 bpp Mode (R 5-bit, G 6-bit, B 5-bit), 65,536 colors



Note: The Data order is as follows, MSB = MD7, LSB = MD0 and Picture Data is MSB = Bit 5, LSB = Bit 0 for Green data and MSB = Bit 4, LSB = Bit 0 for Red and Blue data.

Figure 13-1: 16 bpp Mode (R 5-bit, G 6-bit, B 5-bit), 65,536 colors

13.2 18 bpp (R 6-bit, G 6-bit, B 6-bit), 262,144 colors

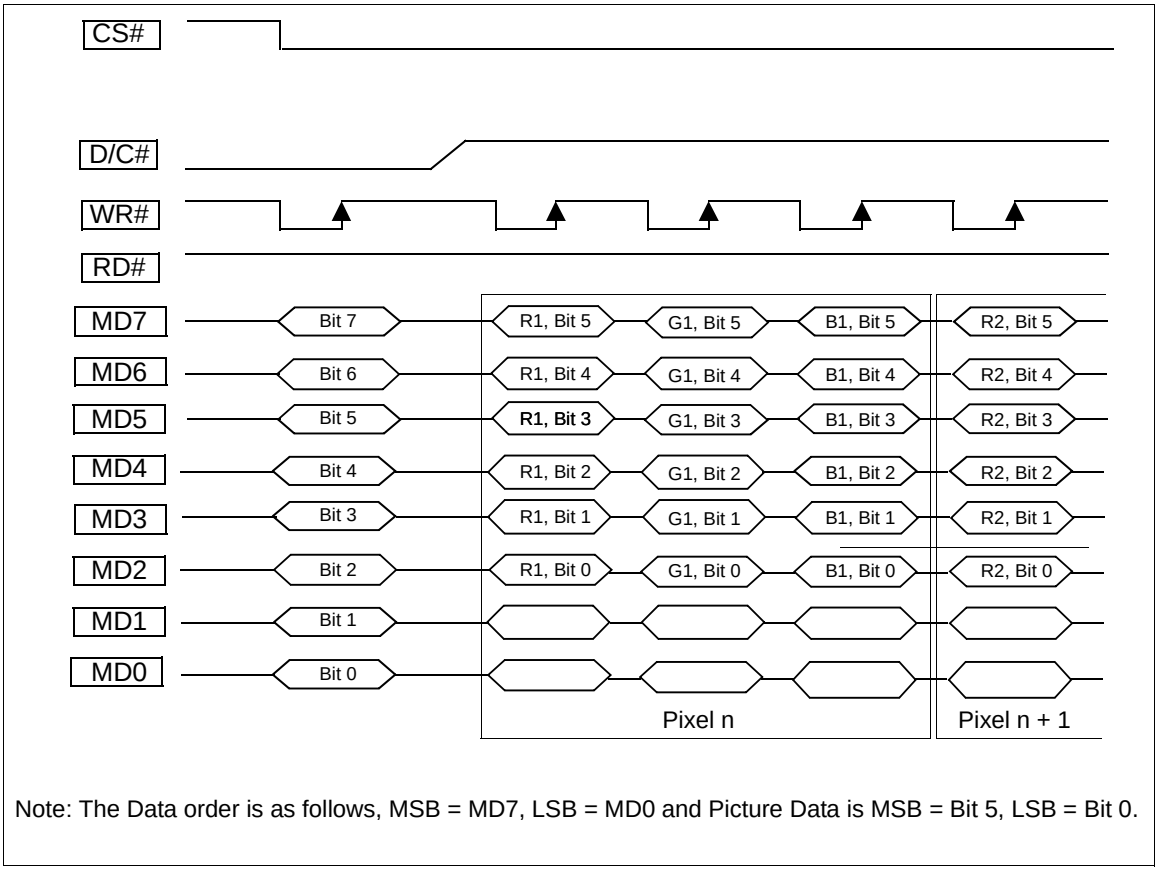
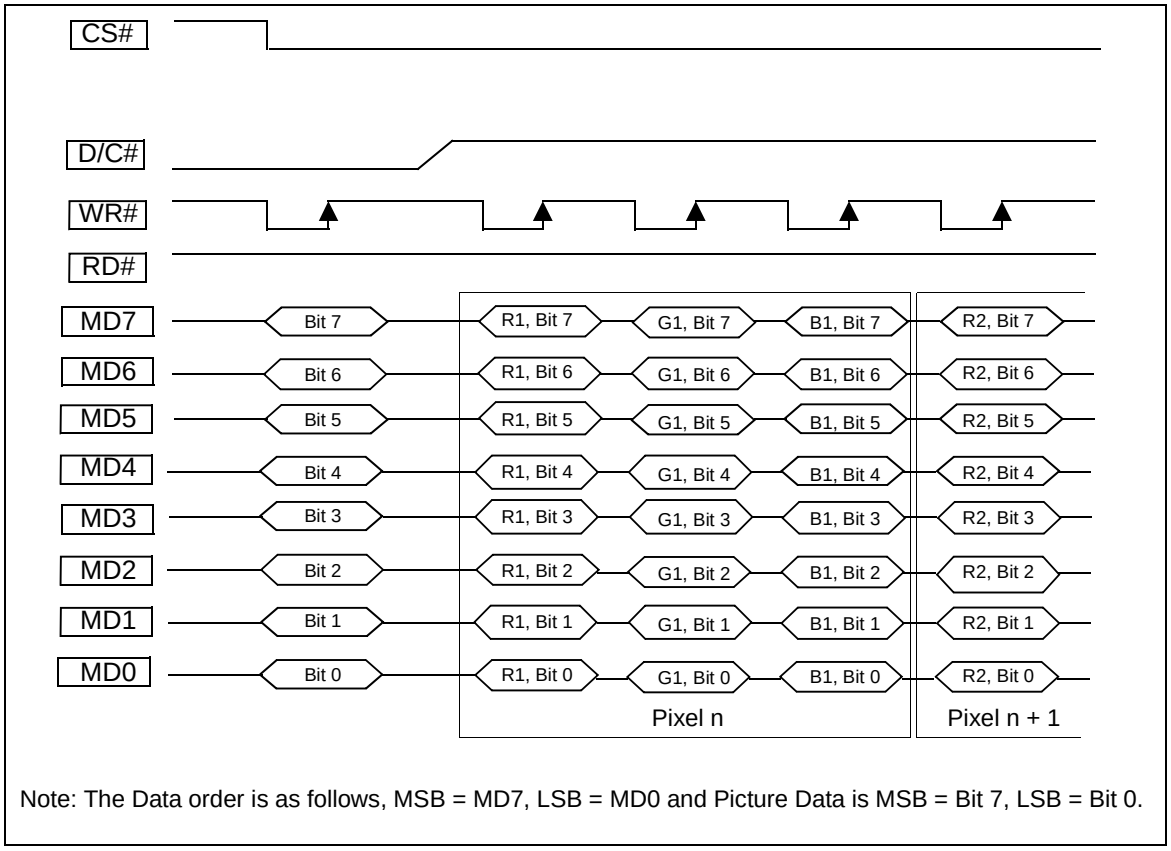


Figure 13-2: 18 bpp (R 6-bit, G 6-bit, B 6-bit), 262,144 colors

13.3 24 bpp (R 8-bit, G 8-bit, B 8-bit), 16,777,216 colors

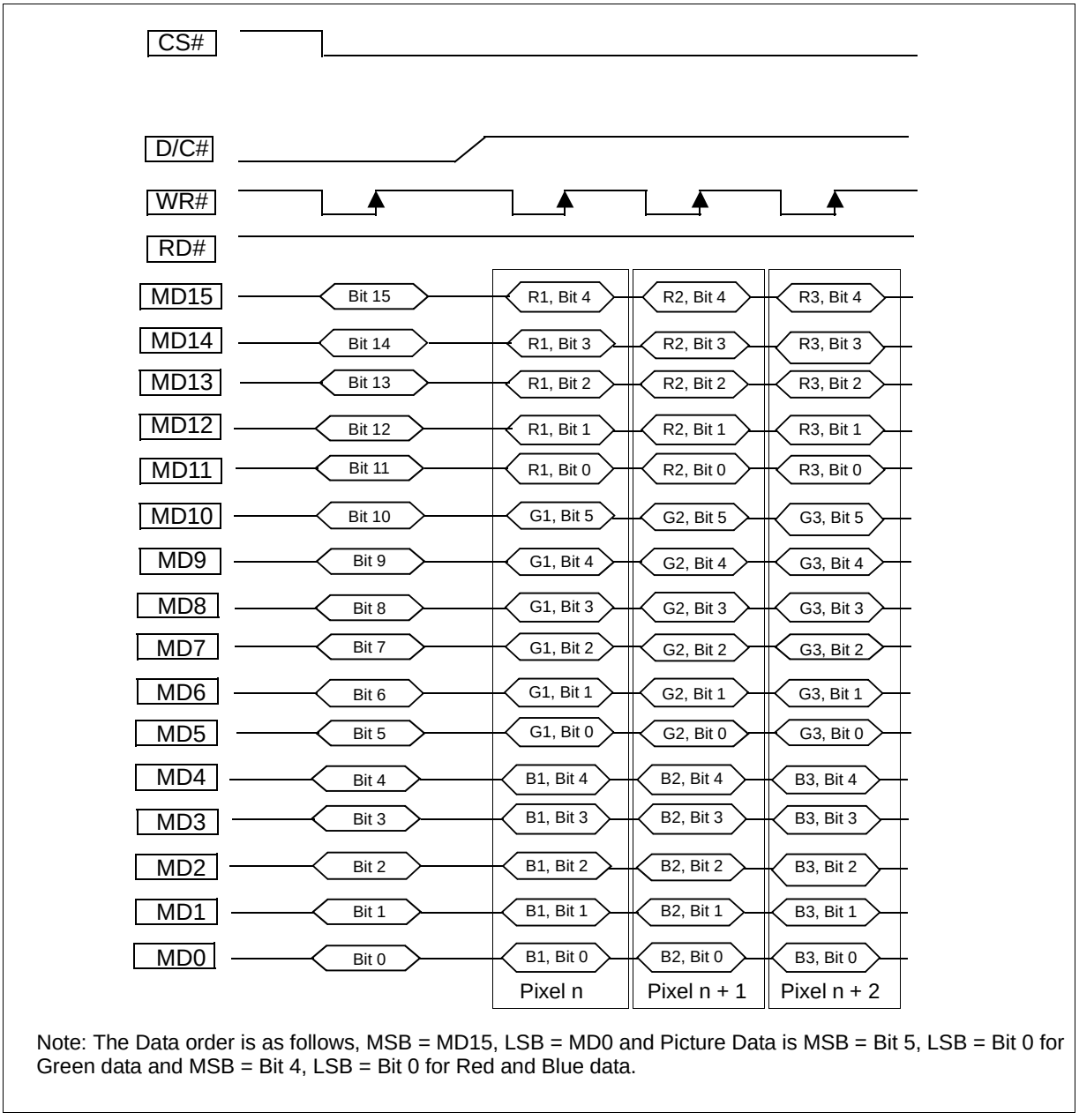


Note: The Data order is as follows, MSB = MD7, LSB = MD0 and Picture Data is MSB = Bit 7, LSB = Bit 0.

Figure 13-3: 24 bpp (R 8-bit, G 8-bit, B 8-bit), 16,777,216 colors

14 Intel 80, 16-bit Interface Color Formats

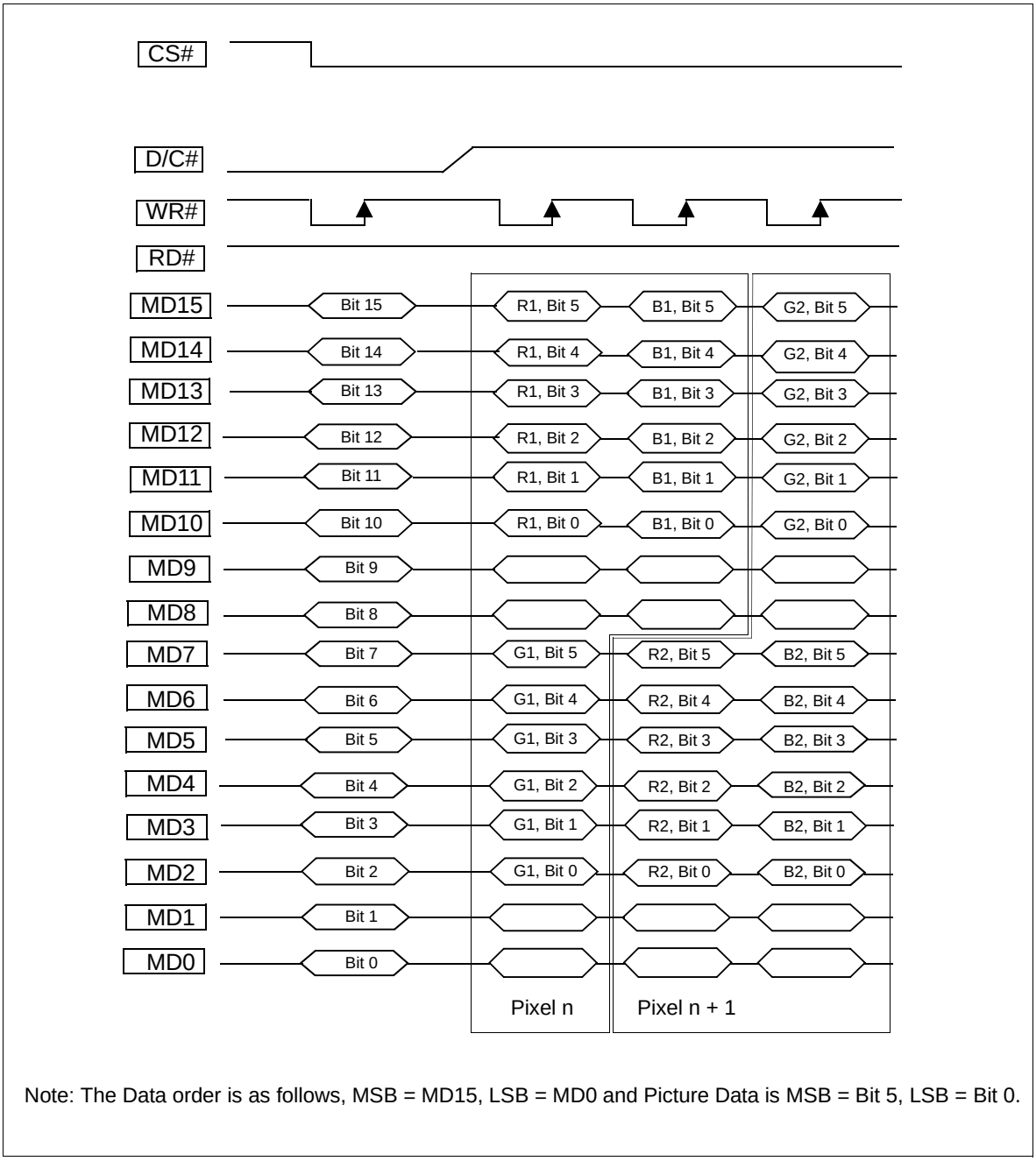
14.1 16 bpp (R 5-bit, G 6-bit, B 5-bit), 65,536 colors



Note: The Data order is as follows, MSB = MD15, LSB = MD0 and Picture Data is MSB = Bit 5, LSB = Bit 0 for Green data and MSB = Bit 4, LSB = Bit 0 for Red and Blue data.

Figure 14-1: 16 bpp (R 5-bit, G 6-bit, B 5-bit), 65,536 colors

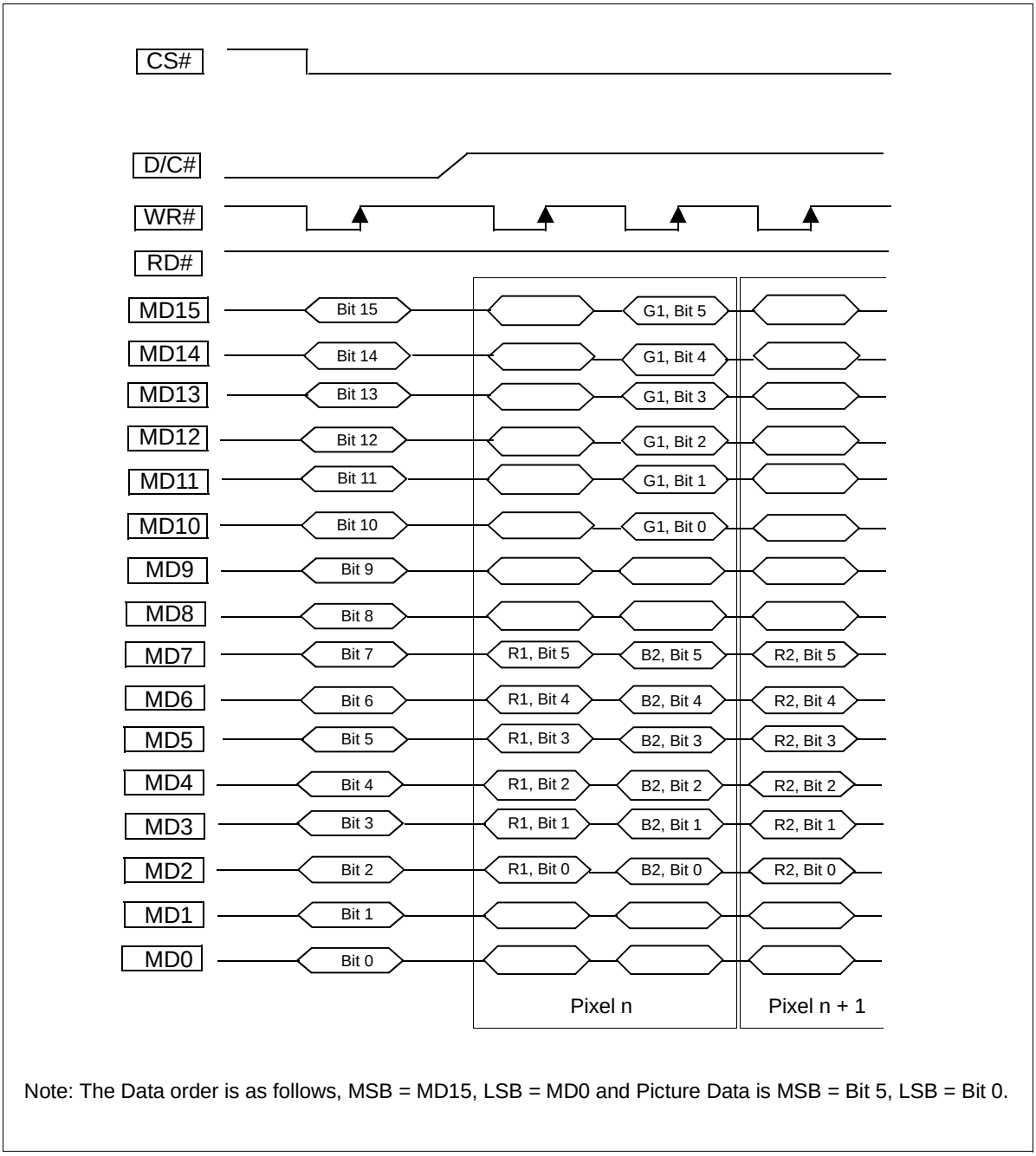
14.2 18 bpp Mode 1 (R 6-bit, G 6-bit, B 6-bit), 262,144 colors



Note: The Data order is as follows, MSB = MD15, LSB = MD0 and Picture Data is MSB = Bit 5, LSB = Bit 0.

Figure 14-2: 18 bpp Mode 1 (R 6-bit, G 6-bit, B 6-bit), 262,144 colors

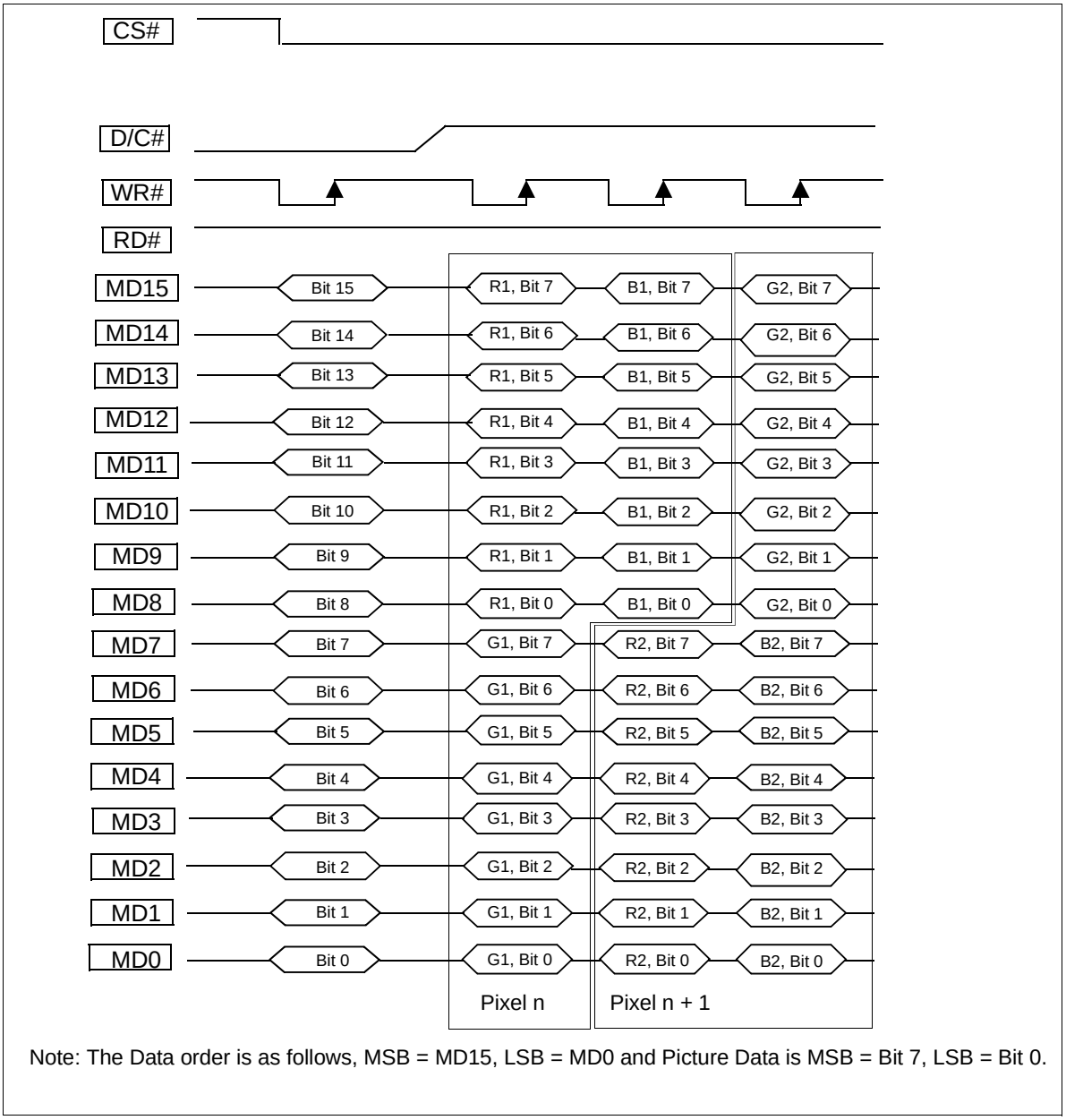
14.3 18 bpp Mode 2 (R 6-bit, G 6-bit, B 6-bit), 262,144 colors



Note: The Data order is as follows, MSB = MD15, LSB = MD0 and Picture Data is MSB = Bit 5, LSB = Bit 0.

Figure 14-3: 18 bpp Mode 2 (R 6-bit, G 6-bit, B 6-bit), 262,144 colors

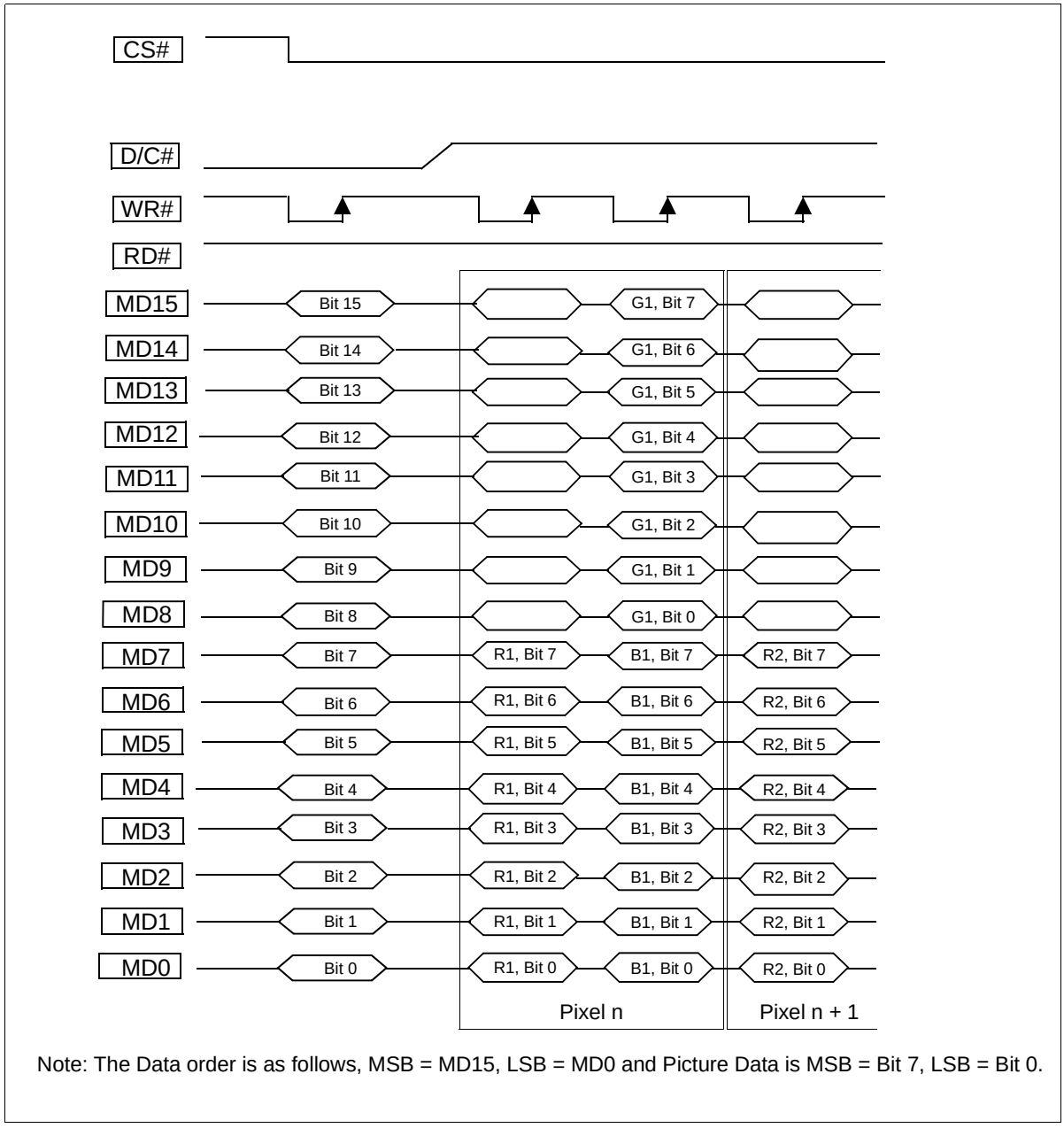
14.4 24 bpp Mode 1 (R 8-bit, G 8-bit, B 8-bit), 16,777,216 colors



Note: The Data order is as follows, MSB = MD15, LSB = MD0 and Picture Data is MSB = Bit 7, LSB = Bit 0.

Figure 14-4: 24 bpp Mode 1 (R 8-bit, G 8-bit, B 8-bit), 16,777,216 colors

14.5 24 bpp Mode 2 (R 8-bit, G 8-bit, B 8-bit), 16,777,216 colors



Note: The Data order is as follows, MSB = MD15, LSB = MD0 and Picture Data is MSB = Bit 7, LSB = Bit 0.

Figure 14-5: 24 bpp Mode 2 (R 8-bit, G 8-bit, B 8-bit), 16,777,216 colors

15 YUV Timing

Format Definition

- The number of pixels per line is always even
- The YC_BC_R colorspace is defined in ITU-R BT601.4
- YUV 4:2:2 format
  $U_{11}Y_{11}V_{11}Y_{12}U_{13}Y_{13}V_{13}Y_{14}$...
- YUV 4:2:0 format
  Odd Line: $UY_{11}Y_{12}$...
  Even Line: $VY_{21}Y_{22}$...

Note
When a window is setup for YUV data, the data must always alternate between odd and even lines, starting with an odd line.

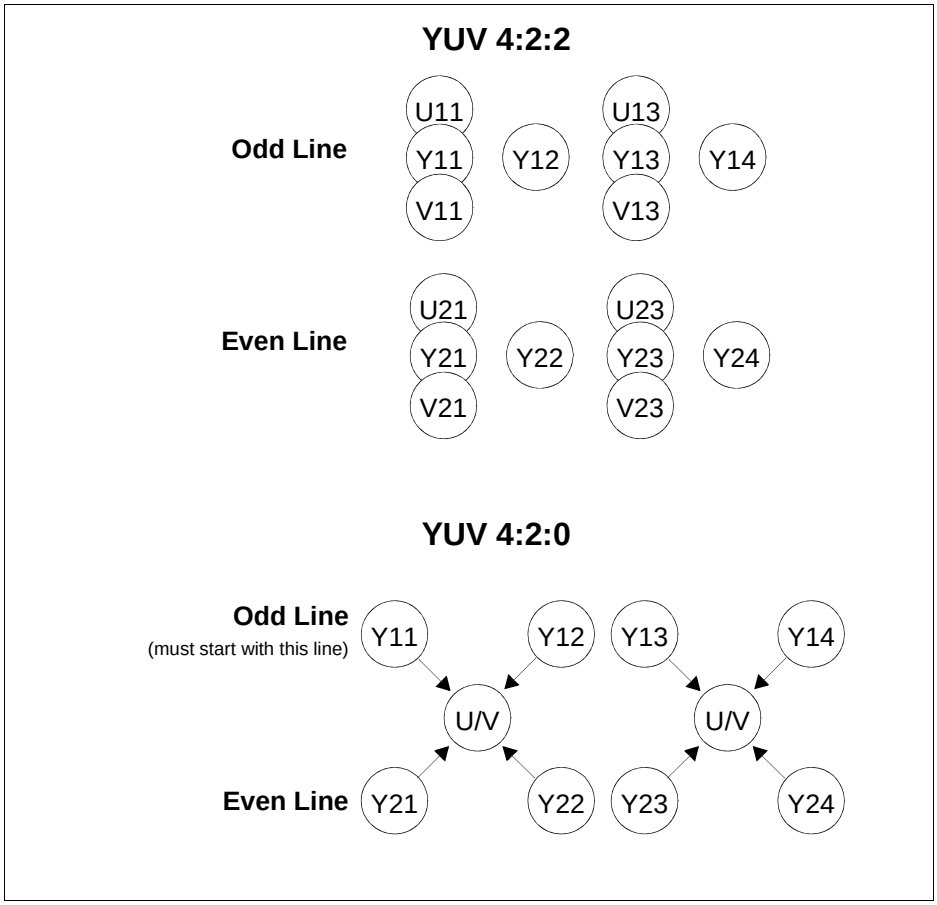


Figure 15-1: YUV Format Definition

15.1 YUV 4:2:2 with Intel 80, 8-bit Interface

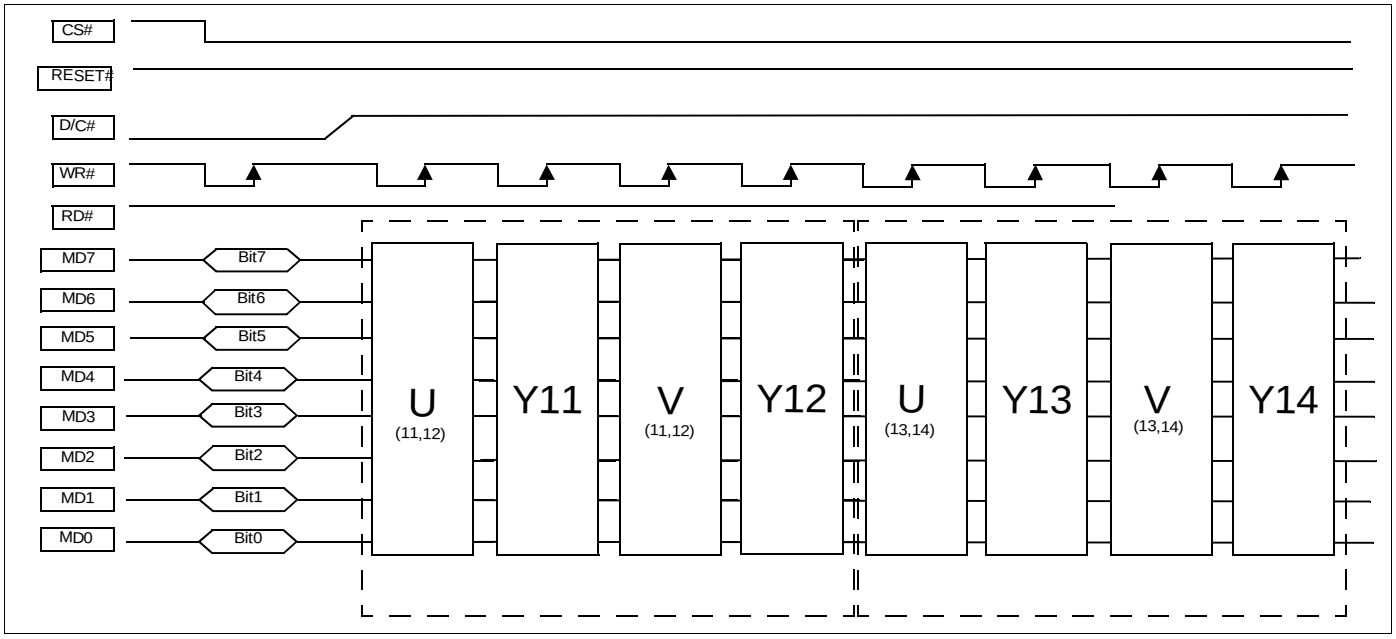


Figure 15-2: YUV 4:2:2 with Intel 80, 8-bit Interface

15.2 YUV 4:2:0 ODD Line with Intel 80, 8-bit Interface

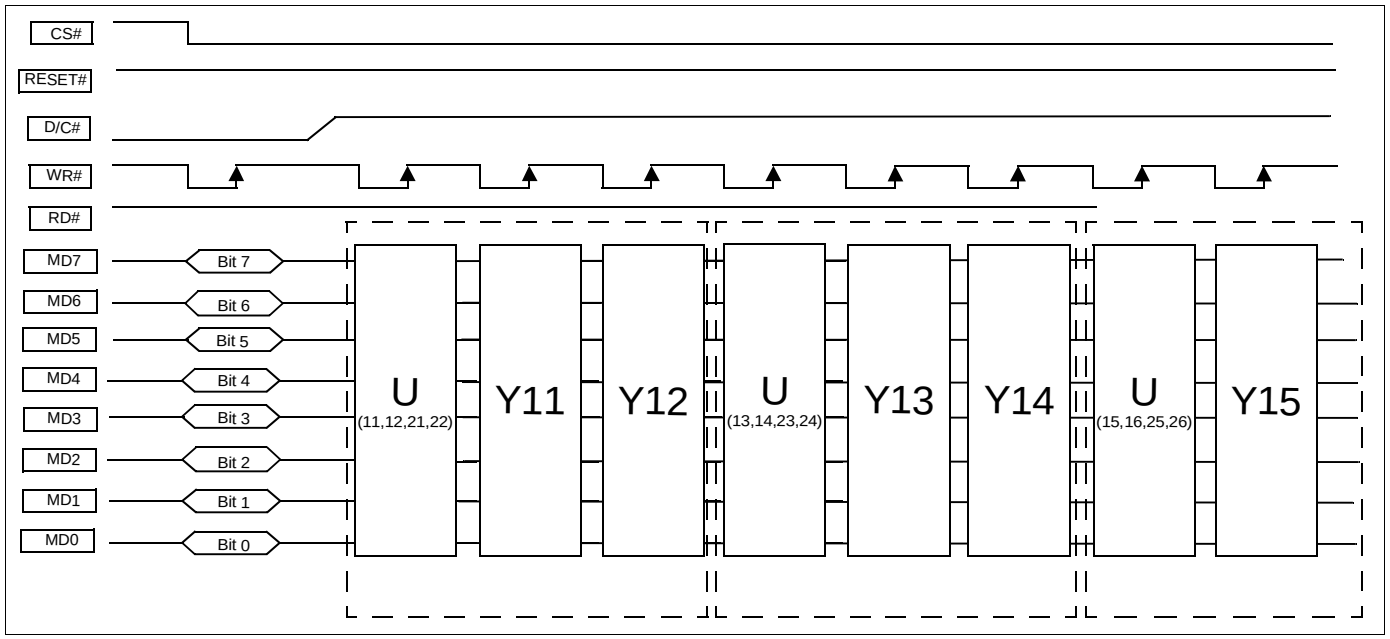


Figure 15-3: YUV 4:2:0 ODD Line with Intel 80, 8-bit Interface

15.3 YUV 4:2:0 EVEN Line with Intel 80, 8-bit Interface

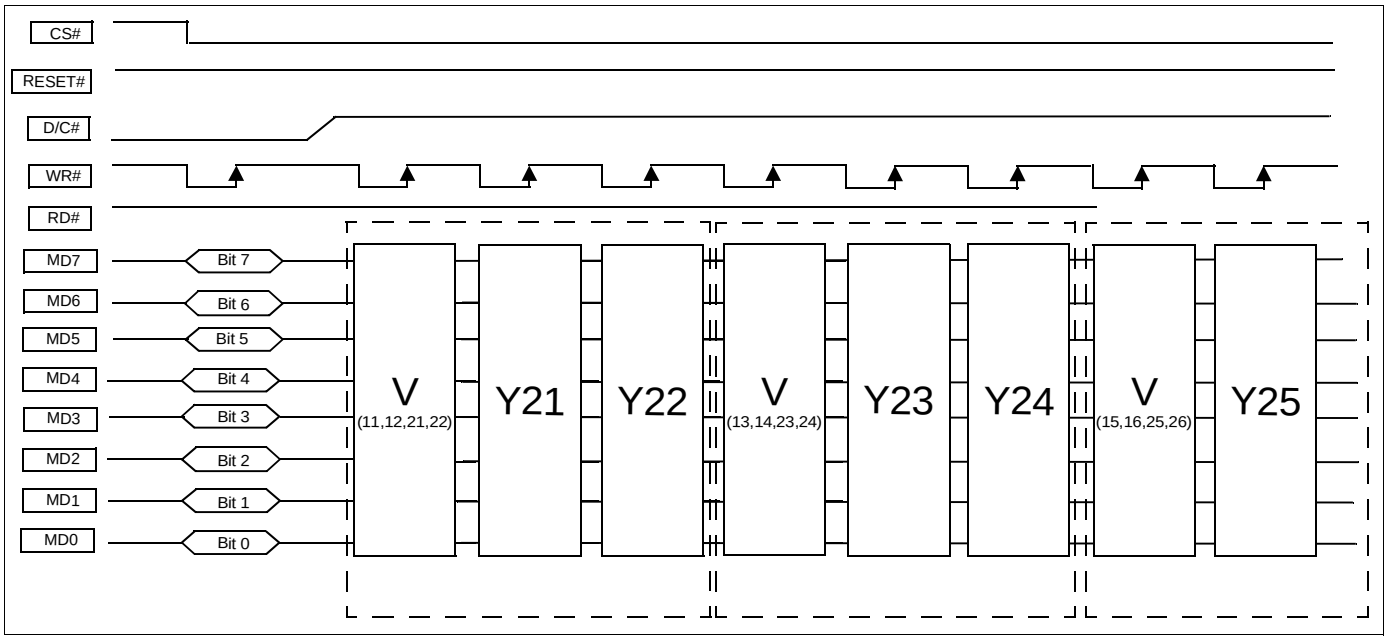


Figure 15-4: YUV 4:2:0 EVEN Line with Intel 80, 8-bit Interface

15.4 YUV 4:2:2 with Intel 80, 16-bit Interface

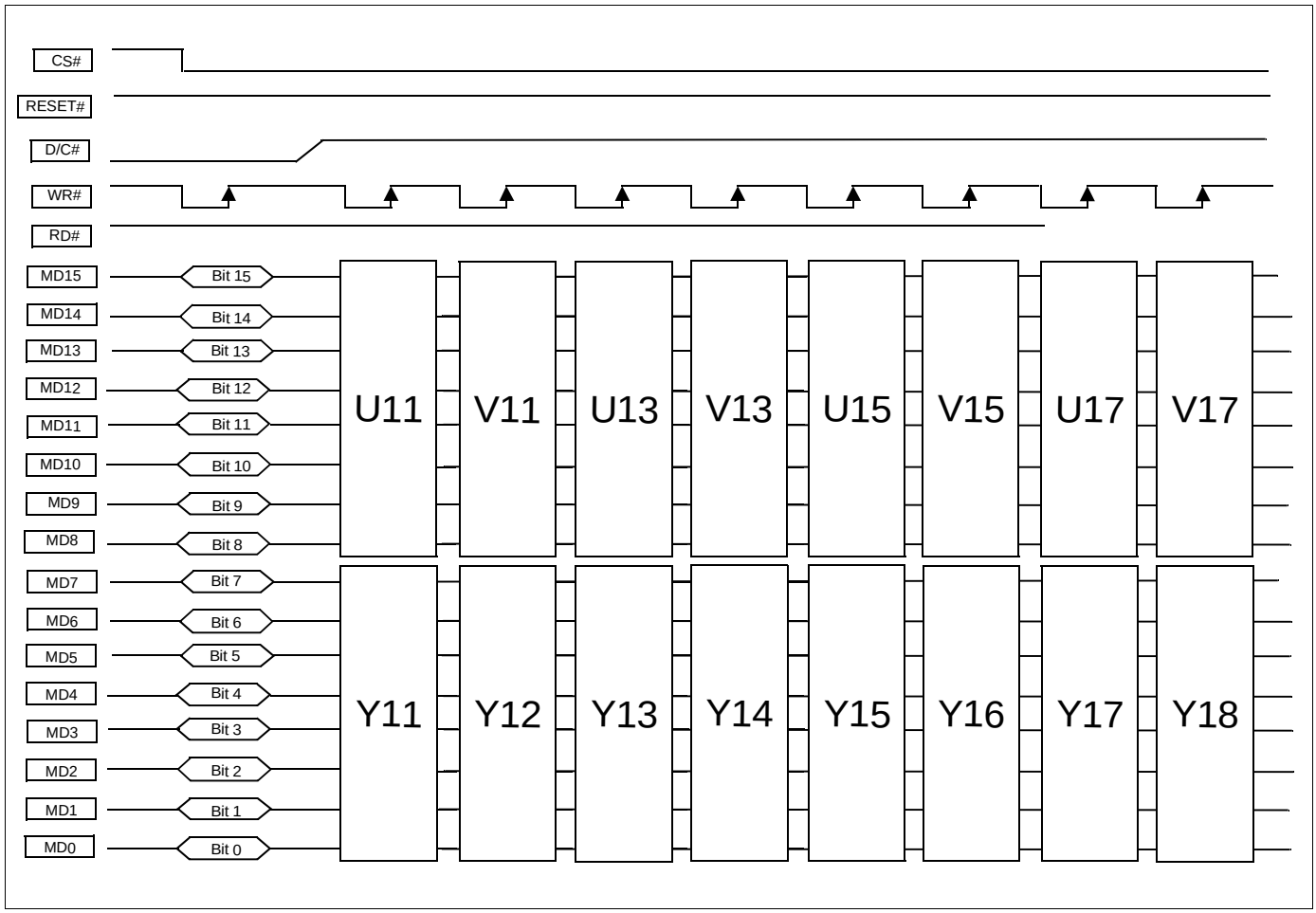


Figure 15-5: YUV 4:2:2 with Intel 80, 16-bit Interface

15.5 YUV 4:2:0 ODD Line with Intel 80, 16-bit Interface

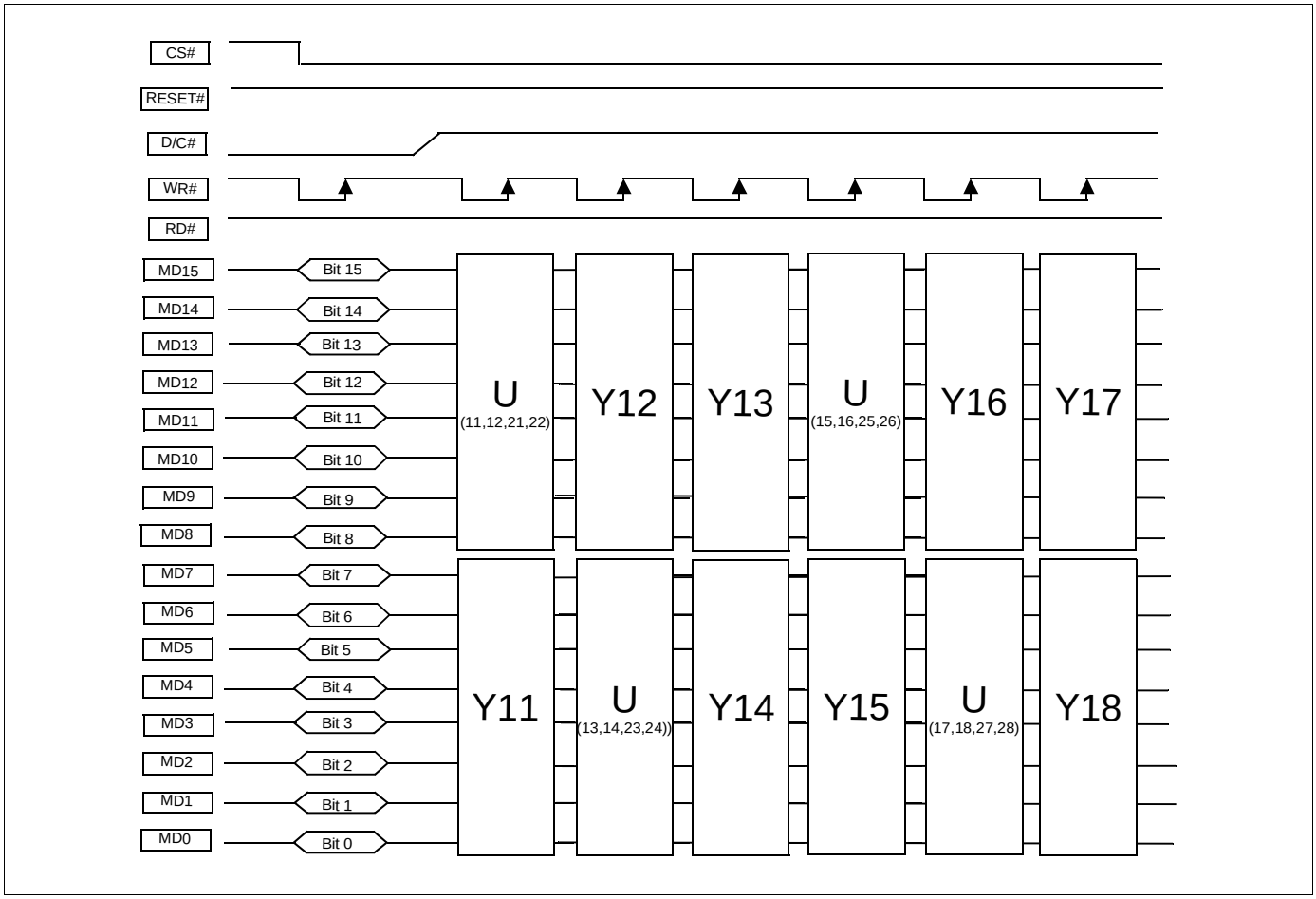


Figure 15-6: YUV 4:2:0 ODD Line with Intel 80, 16-bit Interface

15.6 YUV 4:2:0 EVEN Line with Intel 80, 16-bit Interface

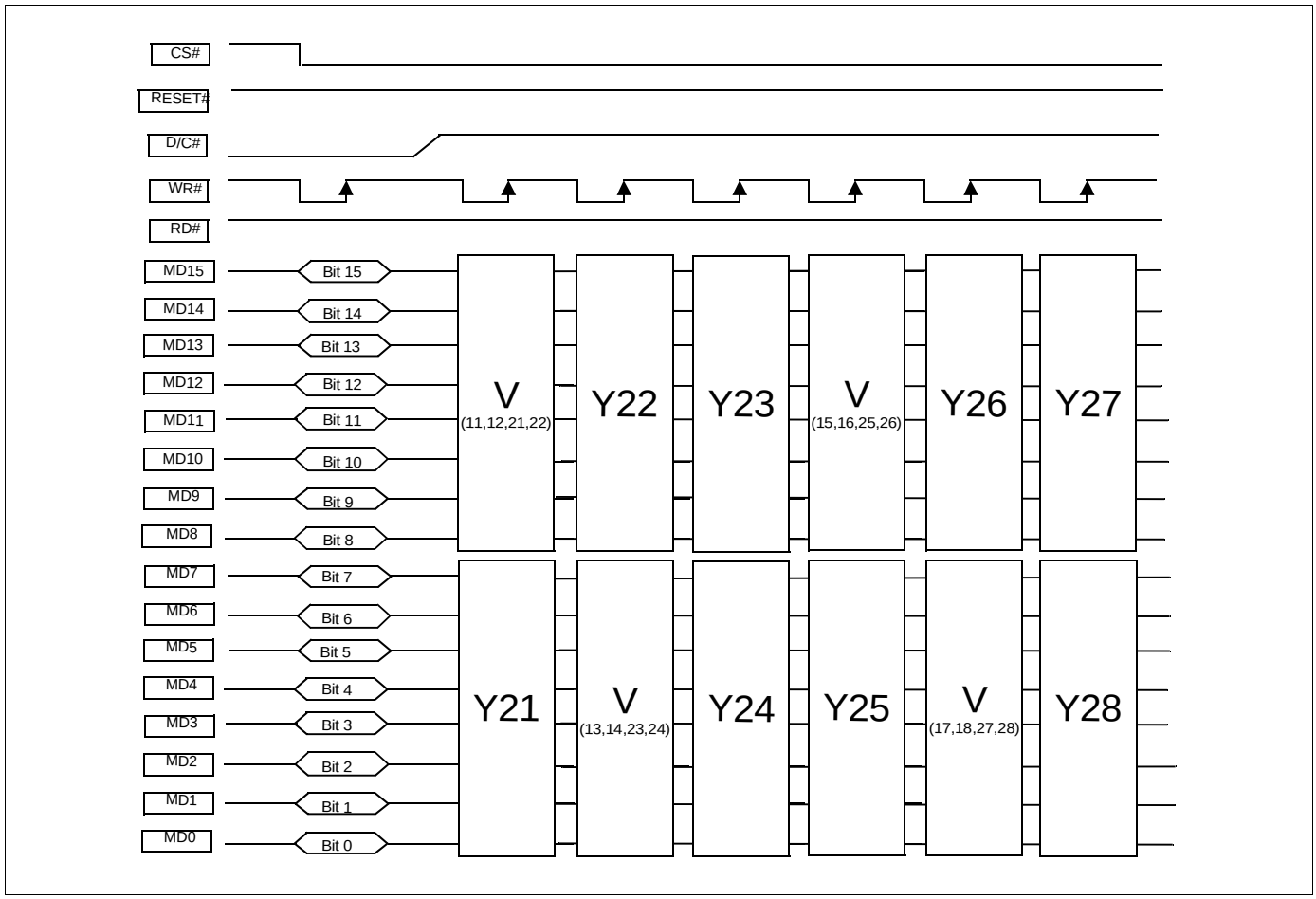


Figure 15-7: YUV 4:2:0 EVEN Line with Intel 80, 16-bit Interface

16 Gamma Correction Look-Up Table Architecture

The following figure is intended to show the display data output path only.

The following diagram shows the architecture for 24 bpp using the LUT.

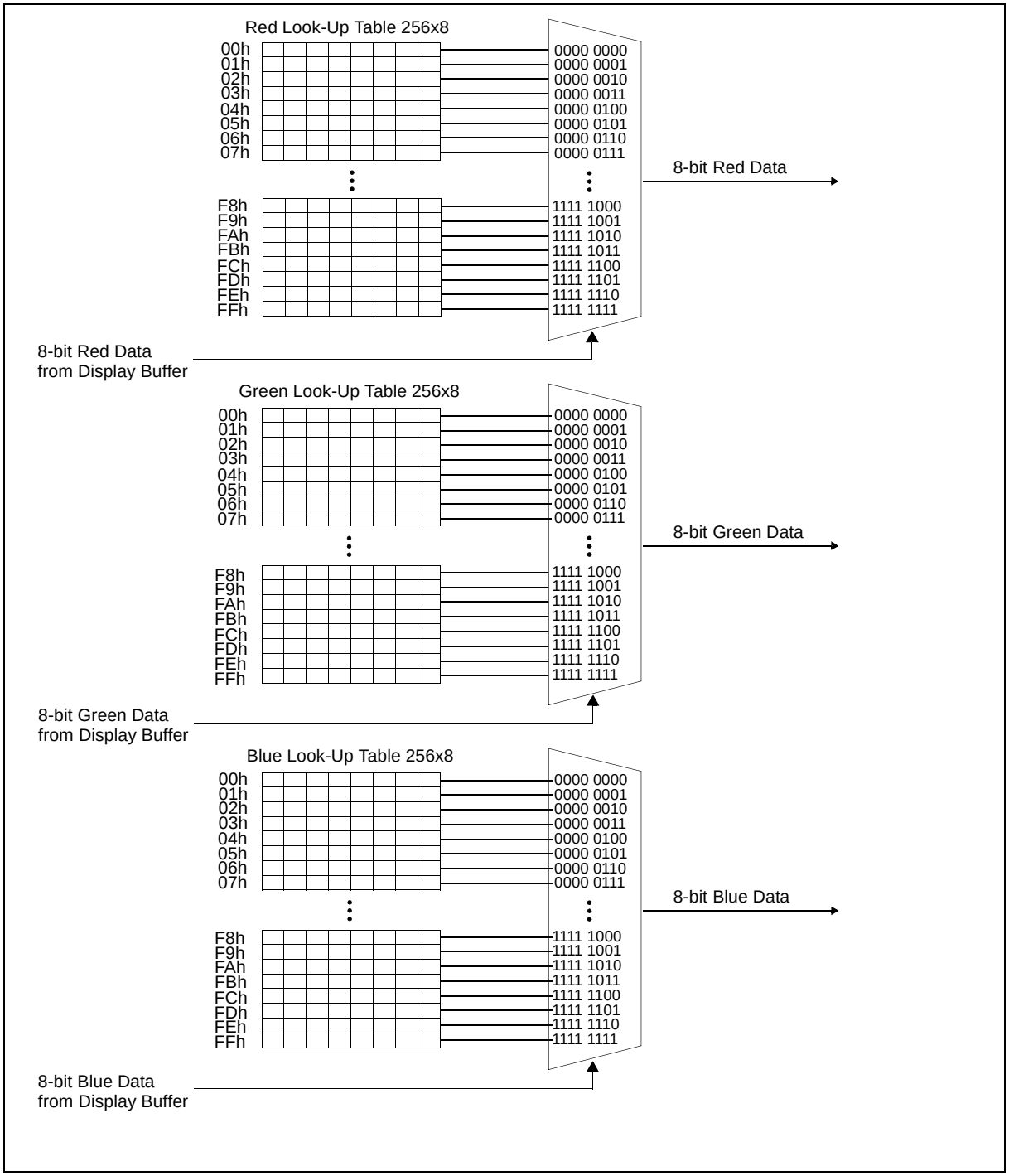


Figure 16-1: Look-Up Table Architecture (24 bpp using LUT)

16.1 Gamma Correction Programming Example

The following procedure should be used to setup and program the Gamma Correction Look-Up Table.

- Disable the LUTs or only access during a non-display period to avoid visual anomalies.
- Write the register “address” for the Gamma Correction Enable register (REG[50h])
- Write data to set the desired LUT Access Mode (see REG[50h] bits 2-1)
- Write data to set the LUT Index to “x” (auto-increment is already enabled, therefore the Gamma Correction Table Index register “address” does not have to be written)
- Write data to the Gamma Correction Table Data register (data value for Index “x”)
- Write data to the Gamma Correction Table Data register (data value for Index “x+1”)
- Continue until all 256 positions have been written
- Enable Gamma Correction (REG[50h] bit 0 = 1)

17 Display Data Format

Table 17-1: 24-Bit Data Format (Non-Swapped, REG[14h] bit 7 = 0b)

Pin Name	Cycle Count				
	1	2	3	...	n
VD23	R_0^7	R_1^7	R_2^7	...	R_n^7
VD22	R_0^6	R_1^6	R_2^6	...	R_n^6
VD21	R_0^5	R_1^5	R_2^5	...	R_n^5
VD20	R_0^4	R_1^4	R_2^4	...	R_n^4
VD19	R_0^3	R_1^3	R_2^3	...	R_n^3
VD18	R_0^2	R_1^2	R_2^2	...	R_n^2
VD17	R_0^1	R_1^1	R_2^1	...	R_n^1
VD16	R_0^0	R_1^0	R_2^0	...	R_n^0
VD15	G_0^7	G_1^7	G_2^7	...	G_n^7
VD14	G_0^6	G_1^6	G_2^6	...	G_n^6
VD13	G_0^5	G_1^5	G_2^5	...	G_n^5
VD12	G_0^4	G_1^4	G_2^4	...	G_n^4
VD11	G_0^3	G_1^3	G_2^3	...	G_n^3
VD10	G_0^2	G_1^2	G_2^2	...	G_n^2
VD9	G_0^1	G_1^1	G_2^1	...	G_n^1
VD8	G_0^0	G_1^0	G_2^0	...	G_n^0
VD7	B_0^7	B_1^7	B_2^7	...	B_n^7
VD6	B_0^6	B_1^6	B_2^6	...	B_n^6
VD5	B_0^5	B_1^5	B_2^5	...	B_n^5
VD4	B_0^4	B_1^4	B_2^4	...	B_n^4
VD3	B_0^3	B_1^3	B_2^3	...	B_n^3
VD2	B_0^2	B_1^2	B_2^2	...	B_n^2
VD1	B_0^1	B_1^1	B_2^1	...	B_n^1
VD0	B_0^0	B_1^0	B_2^0	...	B_n^0

Table 17-2: 24-Bit Data Format (Swapped, REG[14h] bit 7 = 1b)

Pin Name	Cycle Count				
	1	**2**	**3**	**...**	**n**
VD23	B_0^0	B_1^0	B_2^0	...	B_n^0
VD22	B_0^1	B_1^1	B_2^1	...	B_n^1
VD21	B_0^2	B_1^2	B_2^2	...	B_n^2
VD20	B_0^3	B_1^3	B_2^3	...	B_n^3
VD19	B_0^4	B_1^4	B_2^4	...	B_n^4
VD18	B_0^5	B_1^5	B_2^5	...	B_n^5
VD17	B_0^6	B_1^6	B_2^6	...	B_n^6
VD16	B_0^7	B_1^7	B_2^7	...	B_n^7
VD15	G_0^0	G_1^0	G_2^0	...	G_n^0
VD14	G_0^1	G_1^1	G_2^1	...	G_n^1
VD13	G_0^2	G_1^2	G_2^2	...	G_n^2
VD12	G_0^3	G_1^3	G_2^3	...	G_n^3
VD11	G_0^4	G_1^4	G_2^4	...	G_n^4
VD10	G_0^5	G_1^5	G_2^5	...	G_n^5
VD9	G_0^6	G_1^6	G_2^6	...	G_n^6
VD8	G_0^7	G_1^7	G_2^7	...	G_n^7
VD7	R_0^0	R_1^0	R_2^0	...	R_n^0
VD6	R_0^1	R_1^1	R_2^1	...	R_n^1
VD5	R_0^2	R_1^2	R_2^2	...	R_n^2
VD4	R_0^3	R_1^3	R_2^3	...	R_n^3
VD3	R_0^4	R_1^4	R_2^4	...	R_n^4
VD2	R_0^5	R_1^5	R_2^5	...	R_n^5
VD1	R_0^6	R_1^6	R_2^6	...	R_n^6
VD0	R_0^7	R_1^7	R_2^7	...	R_n^7

Table 17-3: 18-Bit Data Format (Non-Swapped, REG[14h] bit 7 = 0b)

Pin Name	Cycle Count				
	1	**2**	**3**	**...**	**n**
VD[23:18]	Low				
VD17	R_0^7	R_1^7	R_2^7	...	R_n^7
VD16	R_0^6	R_1^6	R_2^6	...	R_n^6
VD15	R_0^5	R_1^5	R_2^5	...	R_n^5
VD14	R_0^4	R_1^4	R_2^4	...	R_n^4
VD13	R_0^3	R_1^3	R_2^3	...	R_n^3
VD12	R_0^2	R_1^2	R_2^2	...	R_n^2
VD11	G_0^7	G_1^7	G_2^7	...	G_n^7
VD10	G_0^6	G_1^6	G_2^6	...	G_n^6
VD9	G_0^5	G_1^5	G_2^5	...	G_n^5
VD8	G_0^4	G_1^4	G_2^4	...	G_n^4
VD7	G_0^3	G_1^3	G_2^3	...	G_n^3
VD6	G_0^2	G_1^2	G_2^2	...	G_n^2
VD5	B_0^7	B_1^7	B_2^7	...	B_n^7
VD4	B_0^6	B_1^6	B_2^6	...	B_n^6
VD3	B_0^5	B_1^5	B_2^5	...	B_n^5
VD2	B_0^4	B_1^4	B_2^4	...	B_n^4
VD1	B_0^3	B_1^3	B_2^3	...	B_n^3
VD0	B_0^2	B_1^2	B_2^2	...	B_n^2

Table 17-4: 18-Bit Data Format (Swapped, REG[14h] bit 7 = 1b)

Pin Name	Cycle Count				
	1	**2**	**3**	**...**	**n**
VD[23:18]	Low				
VD17	B_0^2	B_1^2	B_2^2	...	B_n^2
VD16	B_0^3	B_1^3	B_2^3	...	B_n^3
VD15	B_0^4	B_1^4	B_2^4	...	B_n^4
VD14	B_0^5	B_1^5	B_2^5	...	B_n^5
VD13	B_0^6	B_1^6	B_2^6	...	B_n^6
VD12	B_0^7	B_1^7	B_2^7	...	B_n^7
VD11	G_0^2	G_1^2	G_2^2	...	G_n^2
VD10	G_0^3	G_1^3	G_2^3	...	G_n^3
VD9	G_0^4	G_1^4	G_2^4	...	G_n^4
VD8	G_0^5	G_1^5	G_2^5	...	G_n^5
VD7	G_0^6	G_1^6	G_2^6	...	G_n^6
VD6	G_0^7	G_1^7	G_2^7	...	G_n^7
VD5	R_0^2	R_1^2	R_2^2	...	R_n^2
VD4	R_0^3	R_1^3	R_2^3	...	R_n^3
VD3	R_0^4	R_1^4	R_2^4	...	R_n^4
VD2	R_0^5	R_1^5	R_2^5	...	R_n^5
VD1	R_0^6	R_1^6	R_2^6	...	R_n^6
VD0	R_0^7	R_1^7	R_2^7	...	R_n^7

18 SwivelView™

18.1 Concept

Most computer displays are refreshed in landscape orientation – from left to right and top to bottom. Computer images are stored in the same manner. SwivelView™ is designed to rotate the displayed image on a LCD by 90°, 180°, or 270° in a counter-clockwise direction. The rotation is done in hardware and is transparent to the user for all display buffer writes. By processing the rotation in hardware, SwivelView™ offers a performance advantage over software rotation of the displayed image.

The actual address translation is performed during the Host Write and the image data is, therefore, stored in memory in it's rotated orientation. Due to this design of the rotation logic, each Window written to the S1D13743 can be independently rotated with respect to each other.

18.2 90° SwivelView

The following figure shows how the programmer sees a 320x480 portrait image and how the image is being displayed. The application image is written to the S1D13743 in the following sense: A–B–C–D. The display is refreshed in the following sense: B-D-A-C.

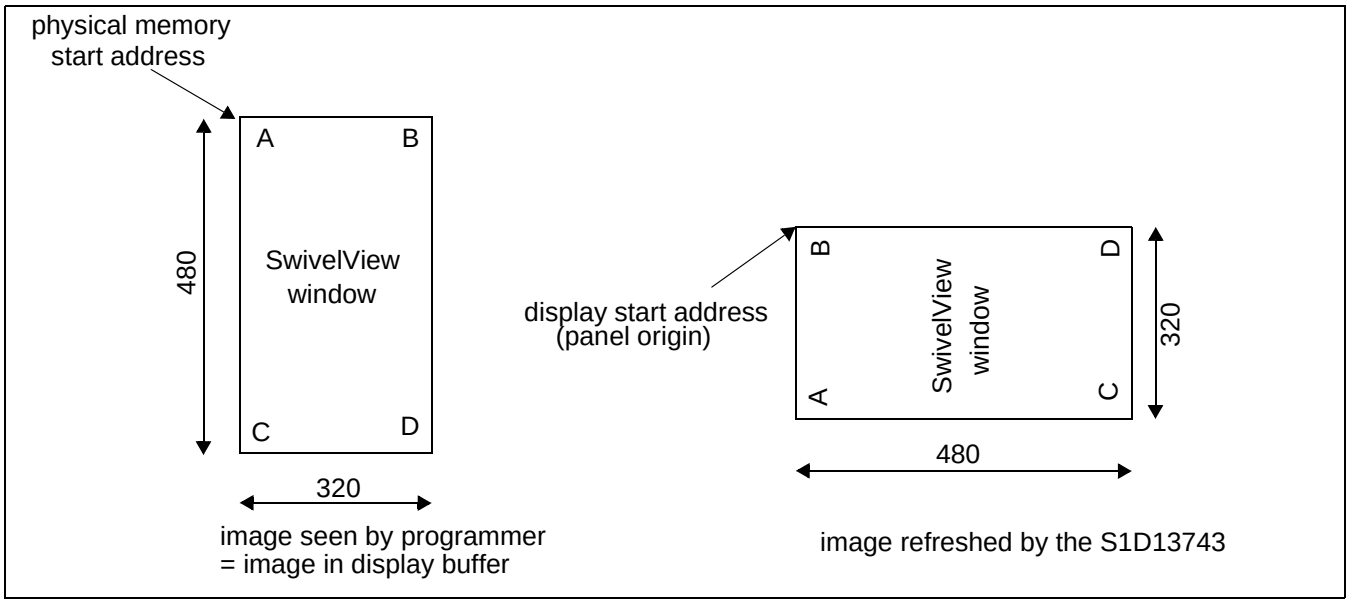


Figure 18-1: Relationship Between The Screen Image and the Image Refreshed in 90° SwivelView

18.2.1 Register Programming

There are no special programming requirements other than simply enabling the rotation itself (see REG[34h] bits 1-0). All Start Addresses and Line Offsets are automatically calculated by hardware.

18.3 180° SwivelView

The following figure shows how the programmer sees a 480x320 landscape image and how the image is being displayed. The application image is written to the S1D13743 in the following sense: A–B–C–D. The display is refreshed in the following sense: D-C-B-A.

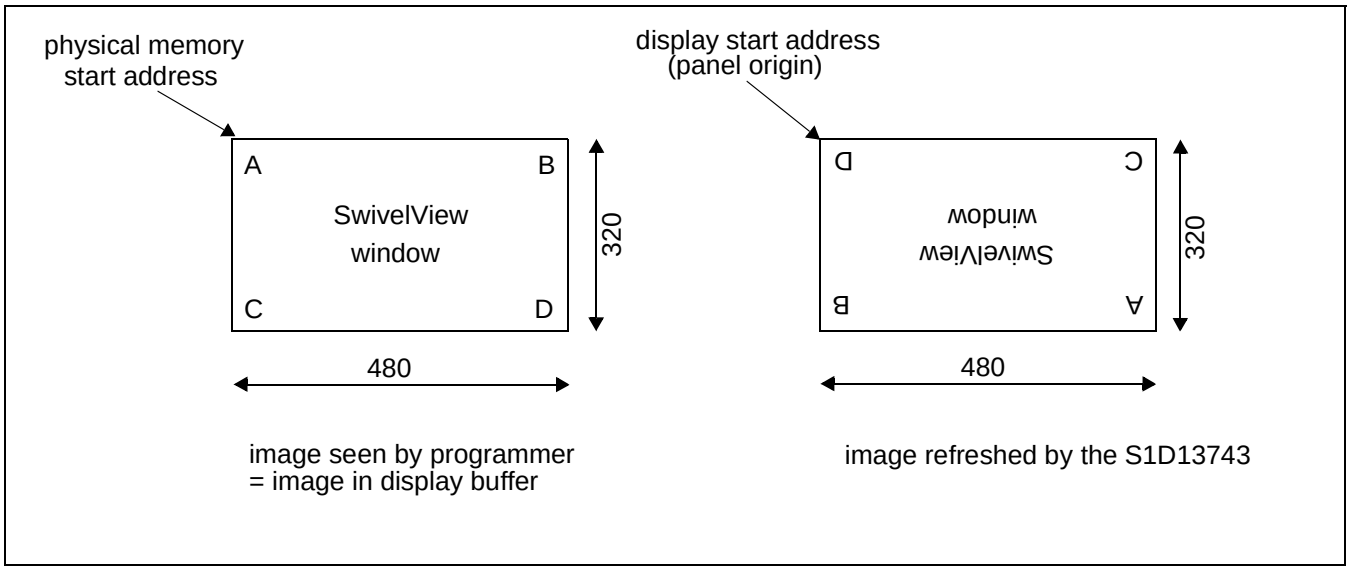


Figure 18-2: Relationship Between The Screen Image and the Image Refreshed in 180° SwivelView

18.3.1 Register Programming

There are no special programming requirements other than simply enabling the rotation itself (see REG[34h] bits 1-0). All Start Addresses and Line Offsets are automatically calculated by hardware.

18.4 270° SwivelView

The following figure shows how the programmer sees a 320x480 portrait image and how the image is being displayed. The application image is written to the S1D13743 in the following sense: A–B–C–D. The display is refreshed in the following sense: C-A-D-B.

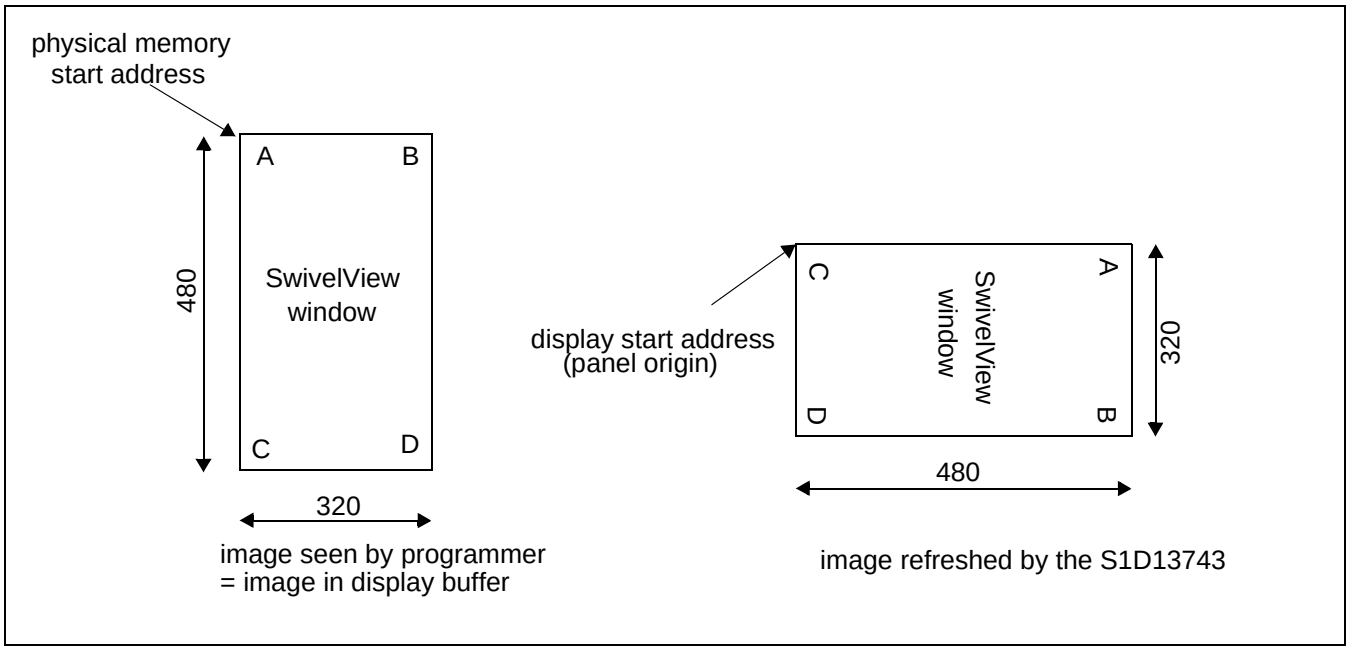


Figure 18-3: Relationship Between The Screen Image and the Image Refreshed in 270° SwivelView

18.4.1 Register Programming

There are no special programming requirements other than simply enabling the rotation itself (see REG[34h] bits 1-0). All Start Addresses and Line Offsets are automatically calculated by hardware.

19 Host Interface

19.1 Using the Intel 80 Interface

Accessing the S1D13743 through the Intel 80 host interface is a multiple step process. All Registers and Memory are accessed through the register space.

Note

All Register accesses are 8-bit only, except for the Memory Data Port. If the Host interface is 16-bits wide (CNF1 = 1b), the lsbs (MD[7:0]) are used for all registers except the Memory Data Port.
For the Memory Data Port (REG[48h, 49h]), both registers are used when the host interface is 16-bits wide (CNF1 = 1b) and only REG[48h] is used when it is 8-bits wide (CNF1 = 0b).

First, perform a single "Address Write" to setup the register address. Next, perform a "Data Read/Write" to specify the data to be stored or read from the registers or memory specified in the "Address Write" cycle. Subsequent data read/writes without an Address Write to change the register address, will automatically "auto" increment the register address, or the internal memory address if accessing the Memory Data Port (REG[48h], REG[49h]).

To write display data to a Window Aperture, specify the Window coordinates followed by burst data writes to the Memory Data Port to fill the window. In this sequence, the internal memory addressing is automatic (see examples). The Memory Data Port is located directly following the Window coordinates to minimize the number of Address Writes.

To read display data, perform an Address Write to the Memory Address Port (3 bytes) and then read data from the Memory Data Port. Sequential reads will auto-increment the internal memory address

19.1.1 Register Write Procedure

1. Perform an address write to setup register address bits 7-0.
2. Perform a data write to update the register.
3. Additional data writes can be performed as the register addresses will be auto-incremented.

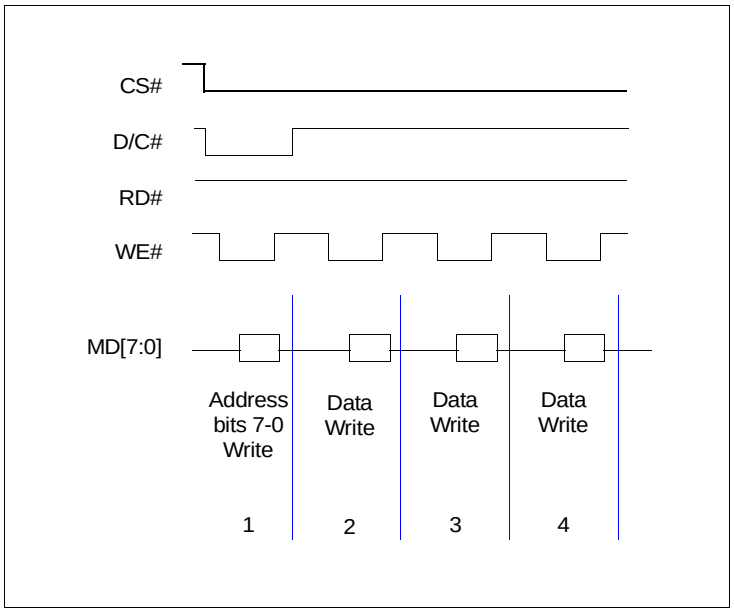


Figure 19-1: Register Write Example Procedure

19.1.2 Register Read Procedure

1. Perform an address write to setup register address bits 7-0.
2. Perform a data read to get the register value.
3. Additional data reads can be performed as the register addresses will be auto-incremented.

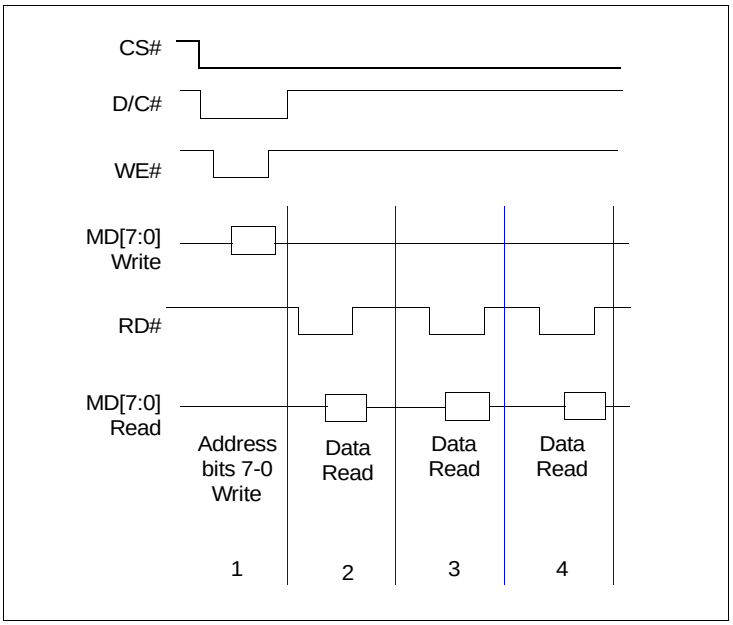


Figure 19-2: Register Read Example Procedure

19.1.3 New Window Aperture Write Procedure

The S1D13743 has a special procedure to minimize setup accesses when bursting window data.

1. Set the panel dimension registers before writing any window data.
2. Perform an address write to point to the first window register (Window X Start Position Register 0, REG[38h]).
3. Perform "data" writes to the next eight, 8-bit registers (REG[38h] ~ REG[46h]). This will setup all the window coordinates.

Note
The register addresses will be auto-incremented after each data write and will point at Memory Data Port Register 0 (REG[48h]) when done.

4. Perform burst data writes to fill the window (the register address will already be pointing at the Memory Data Port).

The Memory Data Port Register is located in the 9th register address after the Window X Start Position. Writes to the Memory Data Port will auto-increment the internal memory address only.

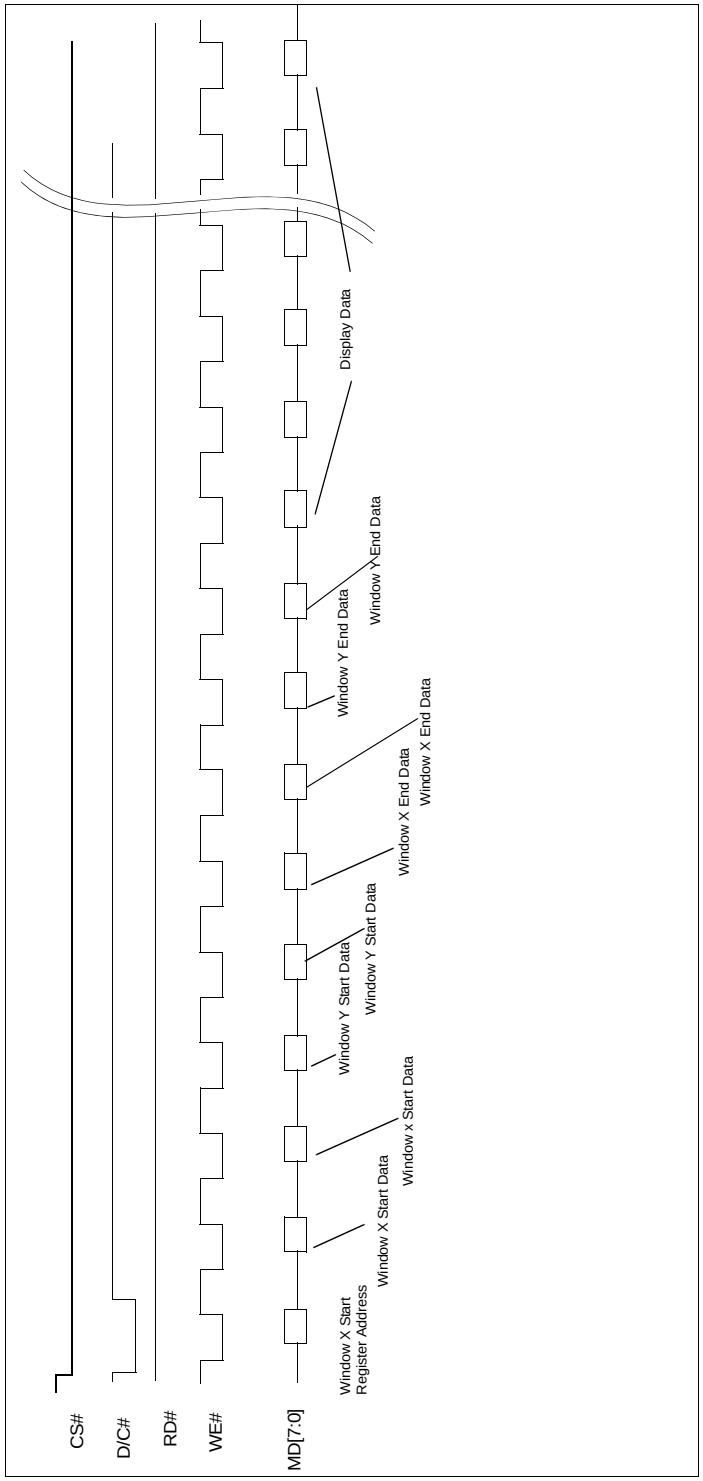


Figure 19-3: Sequential Memory Write Example

19.1.4 Opening Multiple Windows

1. Repeat the steps outlined in Section 19.1.3, “New Window Aperture Write Procedure” on page 102 with new window coordinates for each new window.
2. Non-pixel doubled windows can overlap with the last one being written considered the top.

19.1.5 Update Window using existing Window Coordinates

1. Perform an address write to point to Memory Data Port Register 0 (REG[48h]).
2. Perform burst data writes to fill the window.

Note
In this case, the previous coordinates of the Window Aperture are used. Each write to the Memory Data Port will auto-increment the internally memory address only.

19.1.6 Individual Memory Location Reads

Note
This function is for test purposes only and serves no practical use in a system.

1. Write the physical address of the memory location to read from to the Memory Read Address Registers (REG[4Ah] ~ REG[4Eh]). For a 16-bit bus, the LSB of this address is ignored.
2. Perform a read from the Memory Data Port (REG[48h] ~ REG[49h]).
3. Continuous reads from the Memory Data Port will cause the address in the Memory Read Address registers to increment, thereby supporting burst reads.

Note
To access the 8 lsb’s for each 24-bit value, you must know the physical address as they are stored at different locations as compared to the upper 16-bits.

20 Double Buffering

20.1 Double Buffer Controller

Double buffering is provided to prevent tearing of streaming video data. All static (non-video) image data will always be written to the upper half (Buffer 1) of the frame buffer. When video is being input, the first frame will be written to the lower half (Buffer 2) of the double buffer. The second frame will be written to Buffer 1. While video data is being input, the static part of the image going to the LCD will still always come from Buffer 1. The source of the video window will come from either Buffer 1 or Buffer 2, depending on which one was the last to be completely updated.

The switching of the buffer read/write pointers can only occur once per frame, at the beginning of the vertical non-display period. The pointers will only switch if: a video frame had completed being updated within the last output frame period, and no new video frame is currently being written. Because of this, each time the user finishes writing a frame of video data, they should wait until the next vertical non-display period before writing the next frame. This can be accomplished by using the TE pin or by polling the Vertical Display Period Status (REG[58h] bit 7). Alternatively, if the user can guarantee that the maximum input video frame rate is 1/2 the LCD frame rate and that the burst length for writing a video frame is less than one LCD frame period, then no checking for the vertical non-display period is required. If attention is not paid to allowing the pointers to switch, then frames may be dropped.

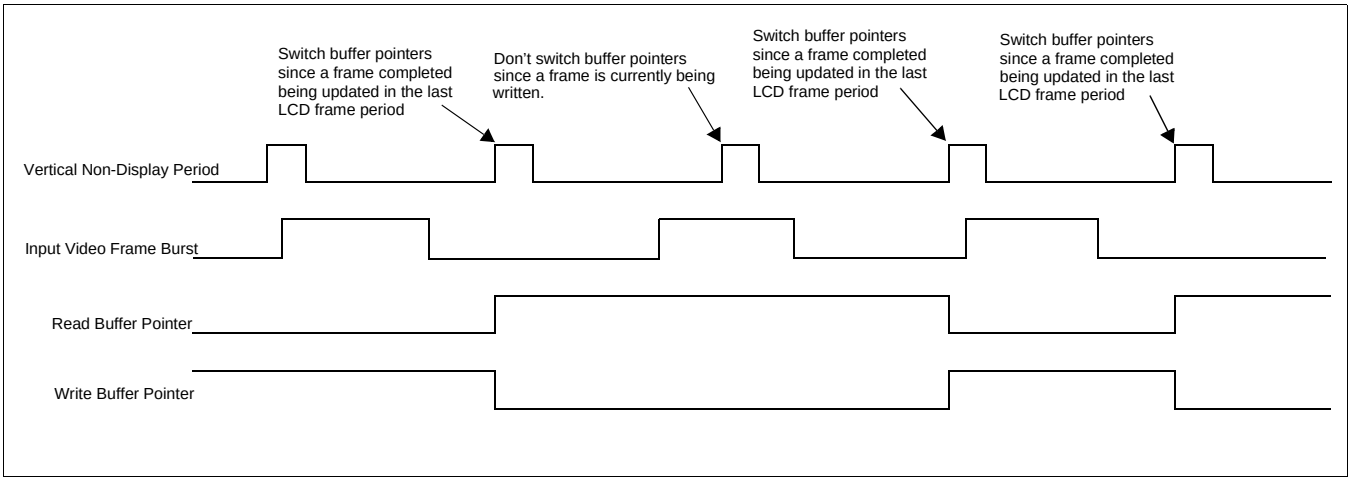


Figure 20-1: Switching of Buffer Pointers

To use the double buffer feature:

- Set appropriate bits in the Special Effects Register, REG[36h] bits 7-6 to 11b.
- Setup the Window Position Registers, REG[38h] ~ REG[46h].
- Write the video data to the Memory Data Port, REG[48h] ~ REG[49h].

It is also possible to update a static window while double buffering is enabled, even in the middle of a video stream. To do this:

- Write the last pixel of the current frame of video data.
- Set the appropriate bits in the Special Effects Register, REG[36h] bits 7-6 to 01b.
- Setup the Window Position Registers, REG[38h] ~ REG[46h].
- Write the static data to the Memory Data Port, REG[48h] ~ REG[49h].

This allows a static image to be written at any time, while still preventing the double buffered window from tearing. Once the static window has been written, the user can go back to writing the streaming video data by following the steps described above for using the double buffer feature.

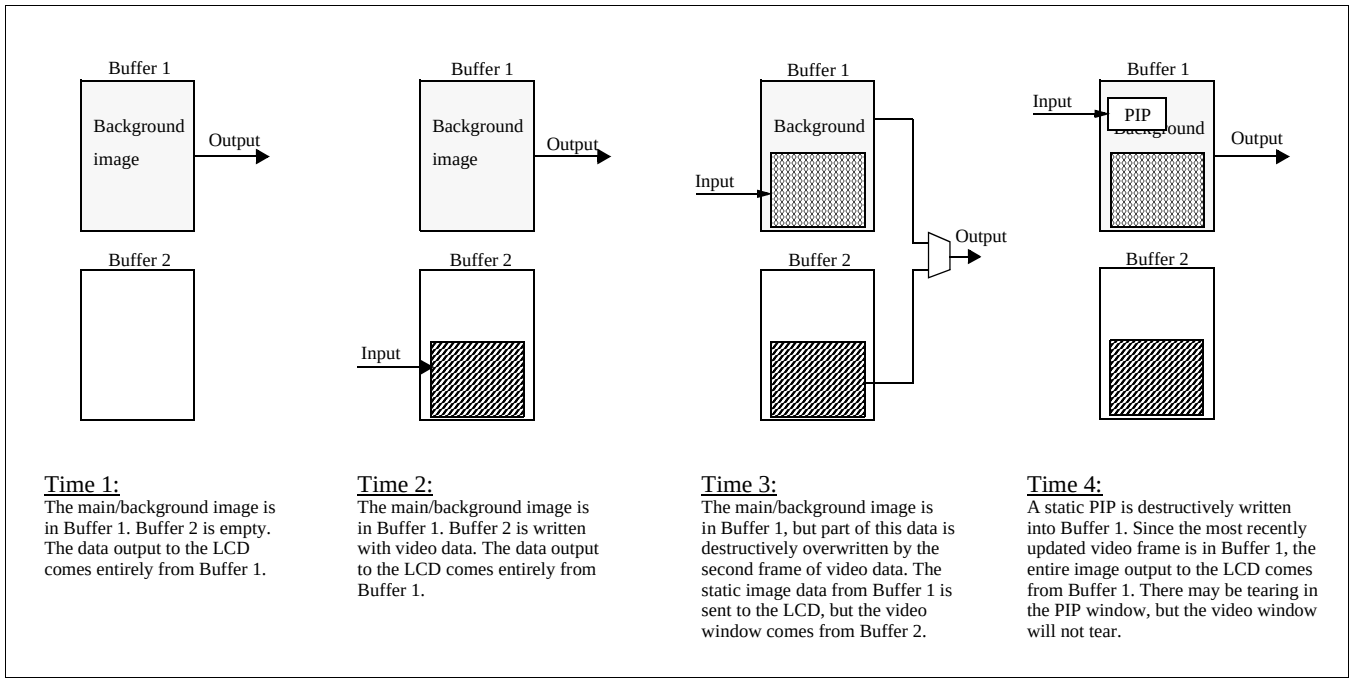


Figure 20-2: Double Buffer Example

20.2 Double Buffering Limitations

There are some limitations to double buffering:

- Consider the case where there is a video stream being input and the user wants to place a static PIP over all or some part of the video window. The user can write the PIP, but when the video stream is continued, it will destructively overwrite the PIP, so that it will appear as though the PIP is under the video window.
- Consider the case where there is a video stream which stops after the last frame of video is sent. The final frame of video will continue to be displayed on the LCD. Assume that this last frame is stored in Buffer 2. Now, if the user disables double buffering, the buffer read pointer will immediately reset to Buffer 1. This means that the 2nd to last frame will now be displayed instead of the last frame.
- The user must either wait for a vertical non-display period between writing frames of video data, or guarantee that their maximum input frame rate is 1/2 the LCD frame rate and that the length of time it takes to burst write a frame of video data is less than one LCD frame period.
- Only one window can be double buffered at a time.

21 Interfacing the S1D13743 and a TFT Panel

This section describes the hardware and software environment required to interface the S1D13743 Mobile Graphics Engine and a 352x416 TFT Panel.

The designs described in this section are presented only as examples of how such interfaces might be implemented.

21.1 Overview

The S1D13743 was designed to directly support the Sanyo LC13015 and requires no additional hardware and minimal programming. The S1D13743 register settings and electrical interface is described below.

21.1.1 Electrical Interface

Table 21-1: Pin Mapping

S1D13743 Pin Name	S1D13743 Pin Number	LCD13015 Pin Name
HS	D9	HS
VS	D10	VS
PCLK	D11	PCLK
DE	C11	DE
VD[17:0]	J8, J9, J10, J11, K4, K5, K6, K7, K8, K9, K10, L3, L4, L5, L6, L7, L8, L9	R5, R4, R3, R2, R1, R0, G5, G4, G3, G2, G1, G0, B5, B4, B3, B2, B1, B0

21.1.2 S1D13743 Register Settings for 352x416 TFT Panel

Note
The registers listed below are only those associated with panel specific timing issues All other registers are not shown here.

Note
When a window is setup for YUV data, the data must always alternate between odd and even lines, starting with an odd line.

Table 21-2: Example Register Settings for 352x416 TFT Panel

Register	Value	Comment
All	default	Come out of reset - all registers set to default values
REG[56h]	02h	enter sleep mode (or use PWRSVE pin)
REG[04h]	12h	set PLL M-Divider. CLKI = 19.2MHz, PLL input clock = CLKI/19 = 1.01MHz.
REG[06h]	F8h	
REG[08h]	80h	
REG[0Ah]	28h	
REG[0Ch]	00h	
REG[0Eh]	2Fh	LL = 48, resulting SYSCLK = LL x PLL input clock = 48MHz
REG[12h]	19h	set PCLK divide, PCLK = 12.1MHz set SYSCLK source = PLL
REG[14h]	0h	no panel data swap, 18-bit panel
REG[16h]	2Ch	HDP = 352 pixels
REG[18h]	5Ah	HNDP = 90 pixels
REG[1Ah]	A0h	VDP = 416 lines
REG[1Ch]	01h	
REG[1Eh]	06h	VNDP = 6 lines
REG[20h]	14h	HS Pulse Width = 20 pixels
REG[22h]	2Dh	HS Start Position = 45 pixels
REG[24h]	02h	VS Width = 2 lines
REG[26h]	01h	VS Start Position (VFP) = 1 line
REG[28h]	80h	PCLK Polarity: data output on falling edge
REG[2Ah]	01h	set input data mode to RGB 5:6:5
REG[56h]	00h	disable sleep mode
REG[04h] bit 7	—	wait for PLL to lock - poll REG[04h] bit 7
REG[38h]	00h	Window X Start Position = 0
REG[3Ah]	00h	
REG[3Ch]	00h	Window Y Start Position = 0
REG[3Eh]	00h	
REG[40h]	5Fh	Window X End Position = 351
REG[42h]	01h	

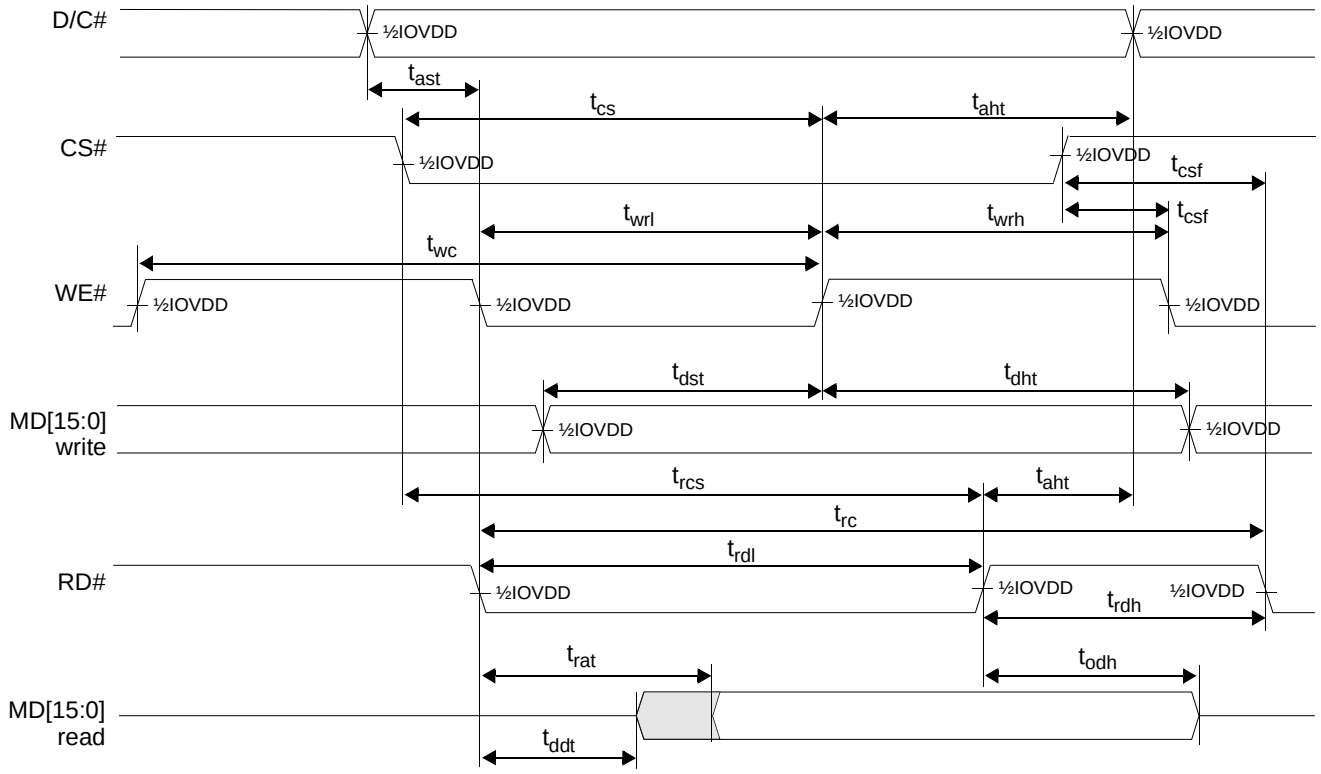
Table 21-2: Example Register Settings for 352x416 TFT Panel (Continued)

Register	Value	Comment
REG[44h]	9Fh	Window Y End Position = 415
REG[46h]	01h	
REG[48h]	Write the image data to the Memory Data Port, REG[48h] and REG[49h]. The image will immediately begin to appear on the LCD.	
REG[49h]		

Note

The above values are intended as examples. This example assumes that CLKI = 19.2MHz and that the PLL is used to generate SYSCLK. Actual settings can vary and still remain within the LCD panel timing requirements.

21.2 Host Bus Timing



Note: The D/C# input pin is used to distinguish between Address and Data.

Note: The register address will auto-increment in word increments for all register access except the Gamma Correction Table Data register and Memory Data Port. Writes to the Gamma Correction Table Data register and Memory Data Port will not increment the register address to support burst data writes to the gamma correction table and to memory.

Figure 21-1: Intel 80 Input A.C. Characteristics

21.2.1 Host Bus Timing for 352x416 TFT Panel

Table 21-3: Intel 80 Input A.C. Characteristics (352x416 Panel Timings)

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/C#	t_{ast}	Address setup time	1.4	—	ns	
	t_{aht}	Address hold time	0.3	—	ns	
CS#	t_{cs}	Chip Select setup time (write)	0.6 + twrl	—	ns	
	t_{rcs}	Chip Select setup time (read)	1.3 + trdl	—	ns	
	t_{csf}	Chip Select Wait time	9.2	—	ns	
WE#	t_{wc}	Write cycle (rising edge to next rising edge)	42.6	—	ns	
	t_{wrh}	Pulse high duration	Note 1	—		
	t_{wrl}	Pulse low duration	0.1	—	ns	
RD#	t_{rc}	Read cycle for Registers	42.6	—	ns	
		Read cycle for Memory	122.1 + trdh	—	ns	
		Read cycle for LUT	108.1 + trdh	—	ns	
	t_{rdh}	Pulse high duration	Note 2	—		
	t_{rdl}	Pulse low duration for Registers	10.2	—	ns	
		Pulse low duration for Memory	122.1	—	ns	
		Pulse low duration for LUT	108.1	—	ns	
MD[15:0]	t_{dst}	Data setup time	0.3	—	ns	For maximum CL=30pF For minimum CL=8pF
	t_{dht}	Data hold time	6.4	—	ns	
	t_{rat} (See note)	Read falling edge to Data valid for Registers	—	12.2	ns	
		Read falling edge to Data valid for Memory	—	122.1	ns	
		Read falling edge to Data valid for LUT	—	108.1	ns	
	t_{odh} (See note)	Read hold time	10.7	32.1	ns	
	t_{ddt} (See note)	Read falling edge to Data driven	3.0	12.3	ns	

SYSCLK = 48MHz, PCLK = 12MHz, CLKI = 12MHz

1. t_{wrh} min = long enough to satisfy t_{wc}
2. t_{rdh} min = long enough to satisfy t_{rc}

21.3 Panel Timing

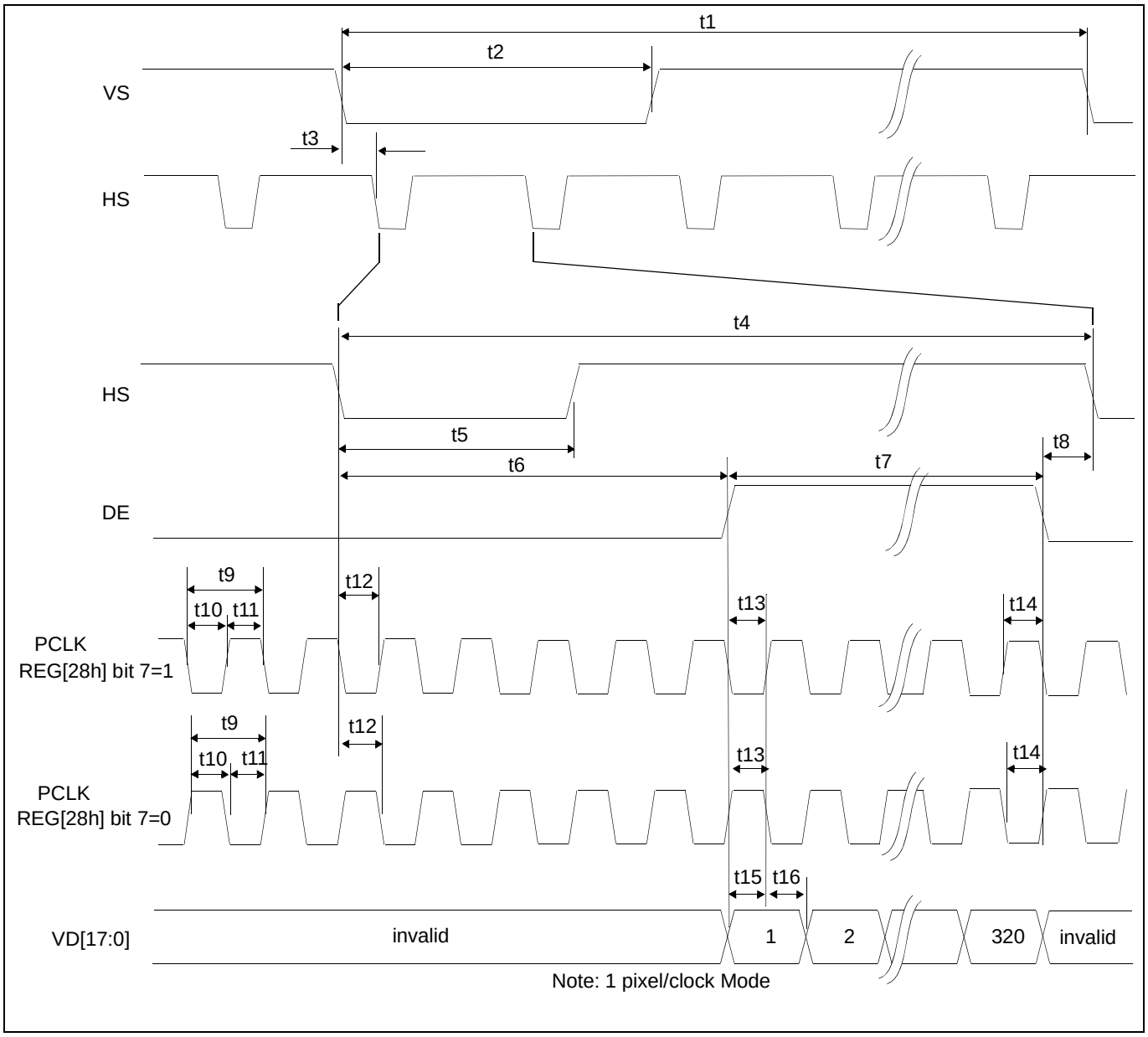


Figure 21-2: 18-Bit TFT A.C. Timing

21.3.1 Panel Timing for 352x416 Panel

Table 21-4: 18-Bit TFT A.C. Timing (352x416 Panel Timing)

Symbol	Parameter	Min	Typ	Max	Units
t1	VS cycle time	—	15.54	—	ms
t2	VS pulse width low	—	73.67	—	us
t3	VS falling edge to HS falling edge phase difference	0	—	36.75	us
t4	HS cycle time	—	36.83	—	us
t5	HS pulse width low	—	1.67	—	us
t6	HS Falling edge to DE active	—	3.75	—	us
t7	DE pulse width	—	29.3	—	us
t8	DE falling edge to HS falling edge	—	3.75	—	us
t9	PCLK period	83.3	—	—	ns
t10	PCLK pulse width low	41.7	—	—	ns
t11	PCLK pulse width high	41.7	—	—	ns
t12	HS setup to PCLK falling edge	41.7	—	—	ns
t13	DE to PCLK rising edge setup time	41.7	—	—	ns
t14	DE hold from PCLK rising edge	41.7	—	—	ns
t15	Data setup to PCLK rising edge	41.7	—	—	ns
t16	Data hold from PCLK rising edge	41.7	—	—	ns

1. Ts = pixel clock period = 83.3 ns (12MHz PCLK)

21.4 Example Play.exe Scripts

The following example scripts are written for the PLAY.EXE program. The script Demo.txt will initialize the S1D13743, then display horizontal bars at different rotations, and then display a PIP+ window.

Demo.txt

```
verbose cmd:off out:on set:off
halt 0

'================================================================================
' _DEMO_.txt - Play script for 13743 to demonstrate various features.
'
' This demonstration code is written in the Play.exe script language so that
' various steps can be easily observed. Some steps such as the initialization
' and the memory fills use Play intrinsic commands. These operation of these
' commands are easily determined.
'================================================================================


' Initialize the registers to the default state by
' running the register list generated by 13743CFG
'-------------------------------------------------------
init

' Set the window to the full screen and clear the display
'-------------------------------------------------------
SetWin.txt
```

```
f WIN 0


' ROTATE 0
'-------------------------------------------------------
print "Color bars at SwivelView 0\n"
x 34 0
DrawBarsA.txt
Pause.txt


' ROTATE 90
' NOTE:  There is a bug with the Fill WINdow command in
'        Play which causes the 90 and 270 degree fills
'        to be filled incorrectly. This will be corrected.
'-------------------------------------------------------
print "Color bars at SwivelView 90\n"
x 34 1
DrawBarsB.txt
Pause.txt


' ROTATE 180
'-------------------------------------------------------
print "Color bars at SwivelView 180\n"
x 34 2
DrawBarsA.txt
Pause.txt


' ROTATE 270
' NOTE:  There is a bug with the Fill WINdow command in
'        Play which causes the 90 and 270 degree fills
'        to be filled incorrectly. This will be corrected.
'-------------------------------------------------------
print "Color bars at SwivelView 270\n"
x 34 3
DrawBarsB.txt
Pause.txt


' PIP
'-------------------------------------------------------
print "Draw Color bars in a PIP (small window)\n"

x 34 0
SetWin.txt
f WIN 0

DrawBarsA.txt
DrawPIP.txt 50 50 100 128
Pause.txt


section END
```

DrawBarsA.txt

```
verbose cmd:off out:on set:off

'================================================================================
' DrawBars.txt - Play script for the 13743
'
' This script draws eight equally sized horizontal
' bars on the display.
'================================================================================

set $Height ((reg[1C] << 8) + (reg[1A]))
set $Lines  ($Height / 8)
set $StartX 0
set $StartY 0
set $EndX    width
set $EndY   $Lines

set $Color  0
set $Bars   8

section LOOP

SetWin.txt $StartX $StartY $EndX $EndY

f WIN $Color

set $StartY ($StartY + $Lines)
set $EndY   ($EndY   + $Lines)
set $Color  ($Color + 0821)

set $Bars ($Bars - 1)
if $Bars!=0 then goto LOOP
```

DrawBarsB.txt

```
verbose cmd:off out:on set:off

'================================================================================
' DrawBarsB.txt - Play script for the 13743
'
' This script draws horizontal bars in SwivelView 90 and SwivelView 270
' display modes.
'================================================================================

set $Height (reg[16] * 8)
set $Lines  ($Height / 8)
set $StartX 0
set $StartY 0
set $EndX    height
set $EndY   $Lines

set $Color  0
set $Bars   8

section LOOP

SetWin.txt $StartX $StartY $EndX $EndY

f WIN $Color

set $StartY ($StartY + $Lines)
set $EndY   ($EndY   + $Lines)
set $Color  ($Color + 0821)

set $Bars ($Bars - 1)
if $Bars!=0 then goto LOOP
```

DrawPIP.txt

```
verbose cmd:off out:on set:off

'=============================================================================
' DrawPIP.txt - Play script for the 13743
'
' This script draws eight equally sized horizontal bars on the display.
'=============================================================================

set $StartX arg[1].nt
set $StartY arg[2].nt
set $Width   arg[3].nt
set $Height arg[4].nt

set $Lines ($Height / 8)

set $Color  0
set $Bars   8


section LOOP

SetWin.txt $StartX  $StartY  $Width  $Lines

f WIN $Color

set $StartY ($StartY + $Lines)
set $Color  ($Color + 0821)

set $Bars ($Bars - 1)
if $Bars!=0 then goto LOOP
```

Pause.txt

```
verbose cmd:off out:on set:off
halt 0

print "Paused . . . press any key to continue\n"
input line
```

SetWin.txt

```
verbose cmd:off out:on set:off

'--------------------------------------------------------------------------------
' SetWin.txt - Play script for the 13743
'
' This script is functionally identical to the Play command 'win'. Call this
' script to set the 13743 window co-ordinates as specified by the arguments.
'
'   Syntax:  SetWin X Y W H
'   Where:   X  - Left edge window X position
'            Y  - Top edge window Y position
'            W- Window width
'            H  - Window height
'
'   Example: SetWin 0 0 100 100
'            Sets the window to start at 0,0 and end at 100, 100
'
'            SetWin
'            Sets the window size to the size of the display
'
'   win SX:0 SY:0 EX:width EY:height
'--------------------------------------------------------------------------------

' Set the default window values to the display size.
set $SX 0
set $SY 0
set $EX (width  - 1)
SET $EY (height - 1)

' Use non-default values ONLY if all four arguments are given
if (argn!=5) then goto SETWINDOW

set $SX arg[1].n
set $SY arg[2].n
set $EX (arg[1].n + arg[3].n - 1)
set $EY (arg[2].n + arg[4].n - 1)

section SETWINDOW

' Change the register window settings

x 38  $SX
x 3A ($SX >> 8)

x 3C  $SY
x 3E ($SY >> 8)

x 40  $EX
x 42 ($EX >> 8)

x 44  $EY
x 46 ($EY >> 8)
```

22 PLL Power Supply Considerations

The PLL circuit is an analog circuit which is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible.

The following are guidelines which, if followed, will result in cleaner power to the PLL, this will result in a cleaner and more stable clock. Even a partial implementation of these guidelines will give results.

22.1 Guidelines for PLL Power Layout

The PLL circuit is an analog circuit and is very sensitive to noise on the input clock waveform or the power supply. Noise on the clock or the supplied power may cause the operation of the PLL circuit to become unstable or increase the jitter.

Due to these noise constraints, it is highly recommended that the power supply traces or the power plane for the PLL be isolated from those of other power supplies. Filtering should also be used to keep the power as clean as possible.

The following are guidelines which, if followed, will result in cleaner power to the PLL, resulting in a cleaner and more stable clock. Even a partial implementation of these guidelines will give results.

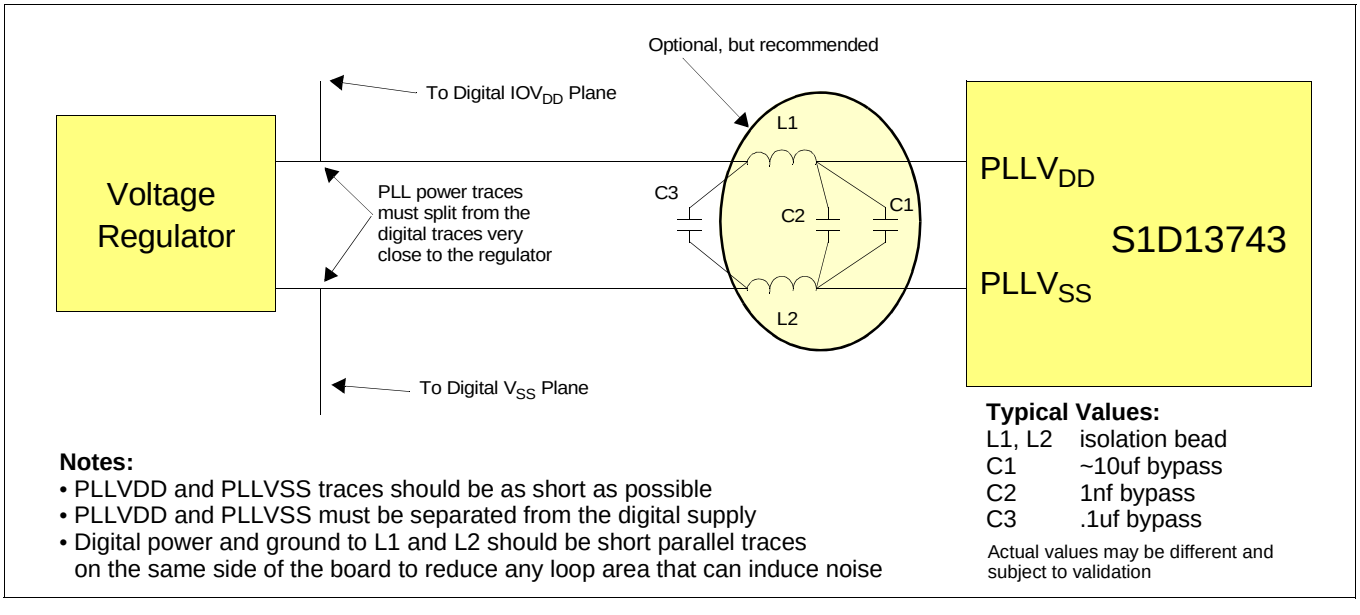


Figure 22-1: PLL Power Layout

- Place the ferrite beads (L1 and L2) parallel to each other with minimal clearance between them. Both bypass caps (C2 and C3) should be as close as possible to the inductors. The traces from C3 to the power planes should be short parallel traces on the same side of the board with just the normal small clearance between them. Any significant loop area here will induce noise. If there is a voltage regulator on the board, try to run these power traces directly to the regulator instead of dropping to the power planes (still follow above rules about parallel traces).
- The analog ground point where bypass cap (C2) connects to the ground isolation inductor (L2) becomes the analog ground central point for a ground star topology. None of the components connect directly to the analog ground pin of the MGE ($PLLV_{SS}$) except for a single short trace from C2 to the $PLLV_{SS}$ pin. The ground side of the large bypass capacitor (C1) should also have a direct connection to the star point.
- The same star topology rules used for analog ground apply to the analog power connection where L2 connects to C2.
- All of the trace lengths should be as short as possible.
- If possible, have all the PLL traces on the same outside layer of the board. The only exception is C1, which can be put on the other side of the board if necessary. C1 does not have to be as close to the analog ground and power star points as the other components.
- If possible, include a partial plane under the PLL area only (area under PLL components and traces). The solid analog plane should be grounded to the C2 (bypass) pad. This plane won't help if it is too large. It is strictly an electrostatic shield against coupling from other layers' signals in the same board area. If such an analog plane is not possible, try to have the layer below the PLL components be a digital power plane instead of a signal layer.
- If possible, keep other board signals from running right next to PLL pin vias on any layer.
- Wherever possible use thick traces, especially with the analog ground and power star connections to either side of C2. Try to make them as wide as the component pads – thin traces are more inductive.

It is likely that manufacturing rules will prohibit routing the ground and power star connections as suggested. For instance, four wide traces converging on a single pad could have reflow problems during assembly because of the thermal effect of all the copper traces around the capacitor pad. One solution might be to have only a single trace connecting to the pad and then have all the other traces connecting to this wide trace a minimum distance away from the pad. Another solution might be to have the traces connect to the pad, but with thermal relief around the pad to break up the copper connection. Ultimately the board must also be manufacturable, so best effort is acceptable.

23 Mechanical Data

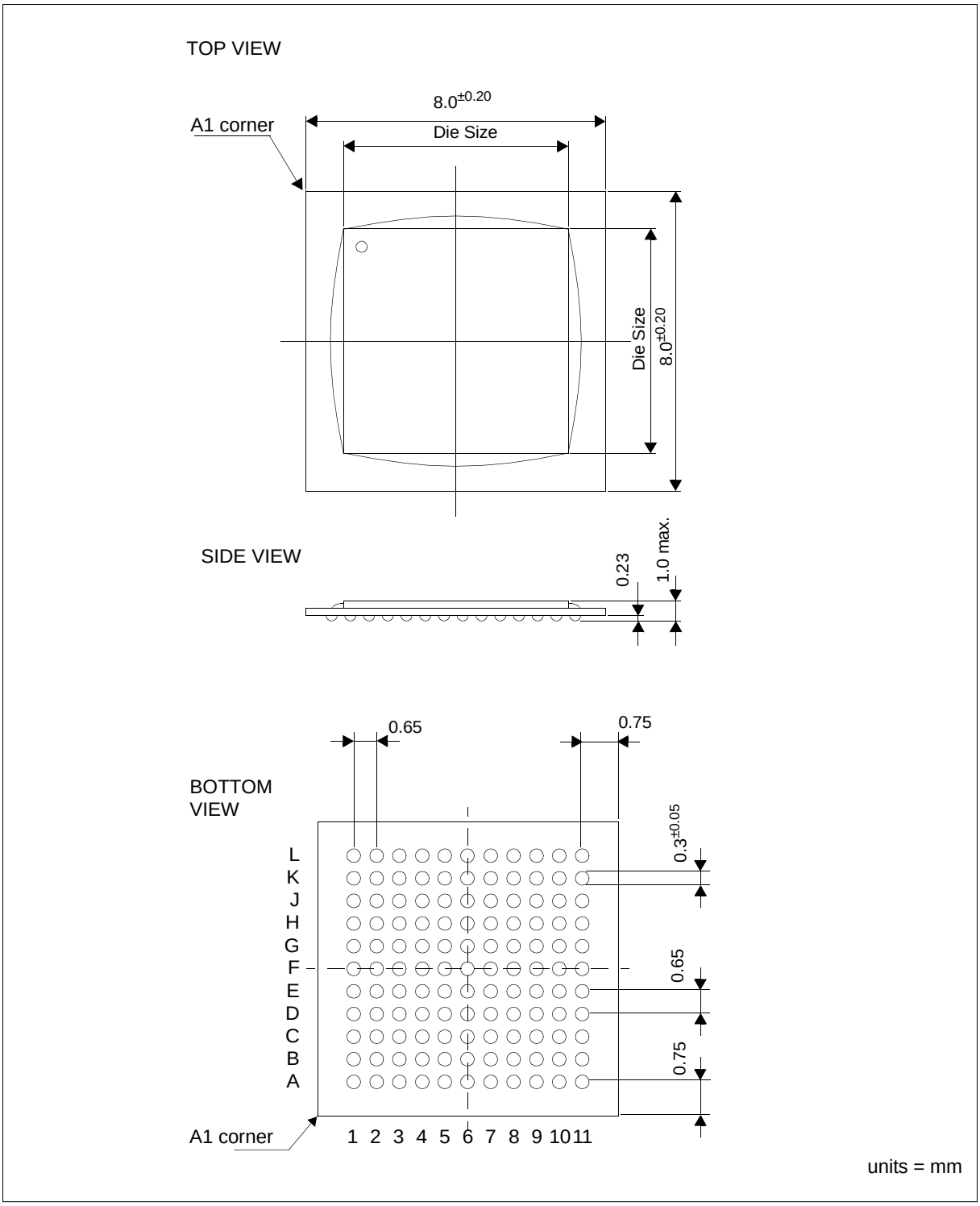
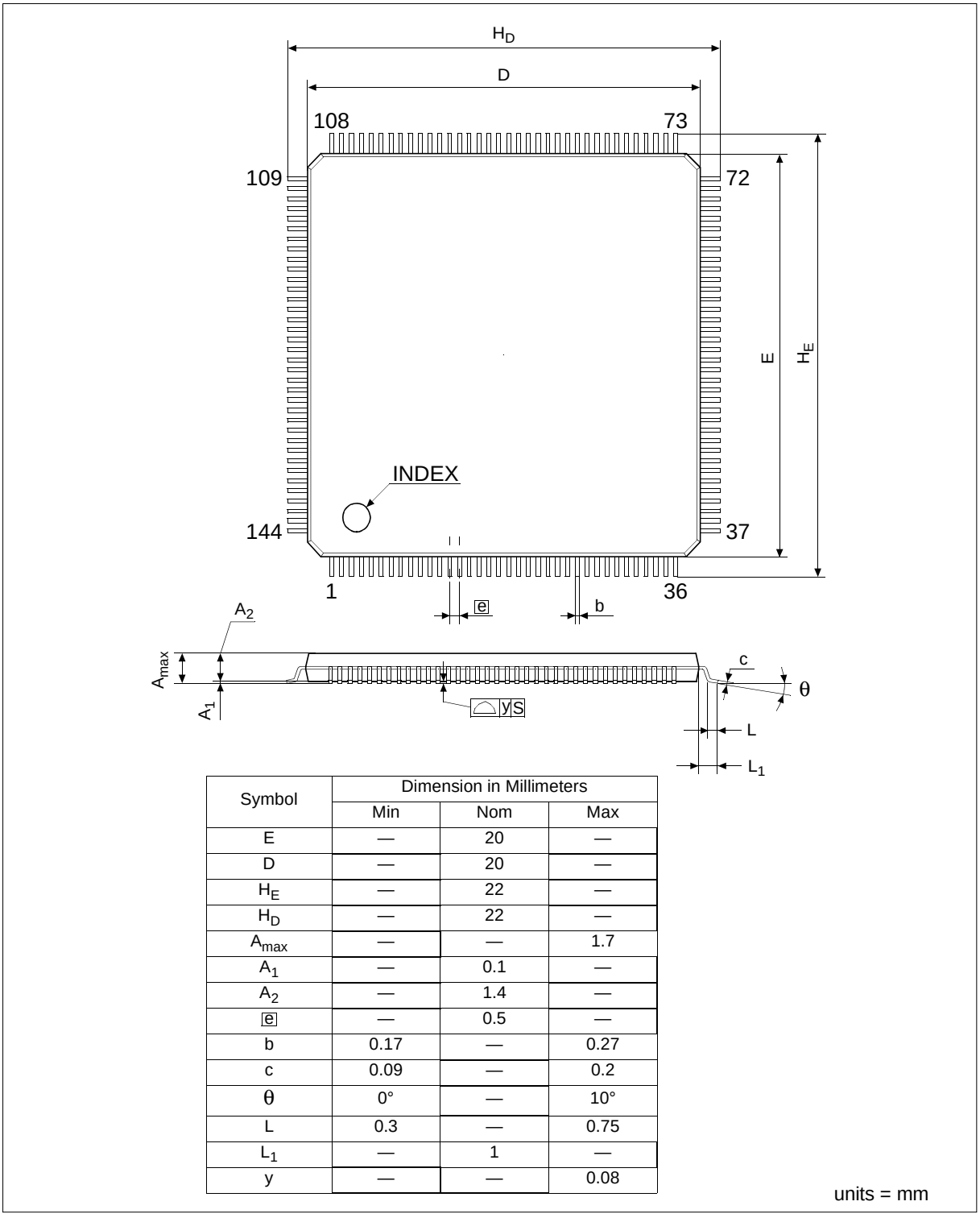


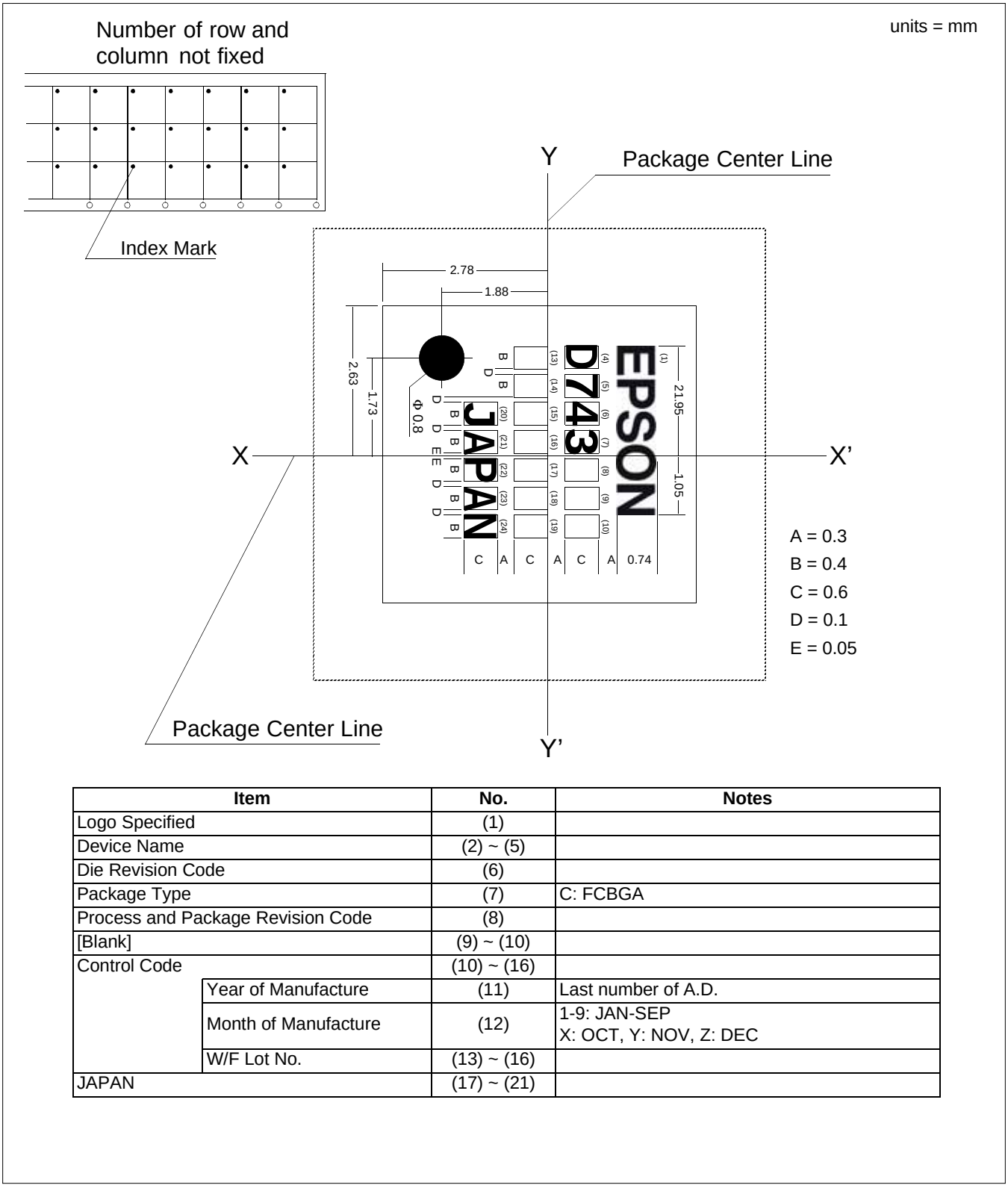
Figure 23-1: S1D13743 FCBGA 121-pin Package



Symbol	Dimension in Millimeters		
	Min	Nom	Max
E	—	20	—
D	—	20	—
H_E	—	22	—
H_D	—	22	—
A_{max}	—	—	1.7
A_1	—	0.1	—
A_2	—	1.4	—
e	—	0.5	—
b	0.17	—	0.27
c	0.09	—	0.2
θ	0°	—	10°
L	0.3	—	0.75
L_1	—	1	—
y	—	—	0.08

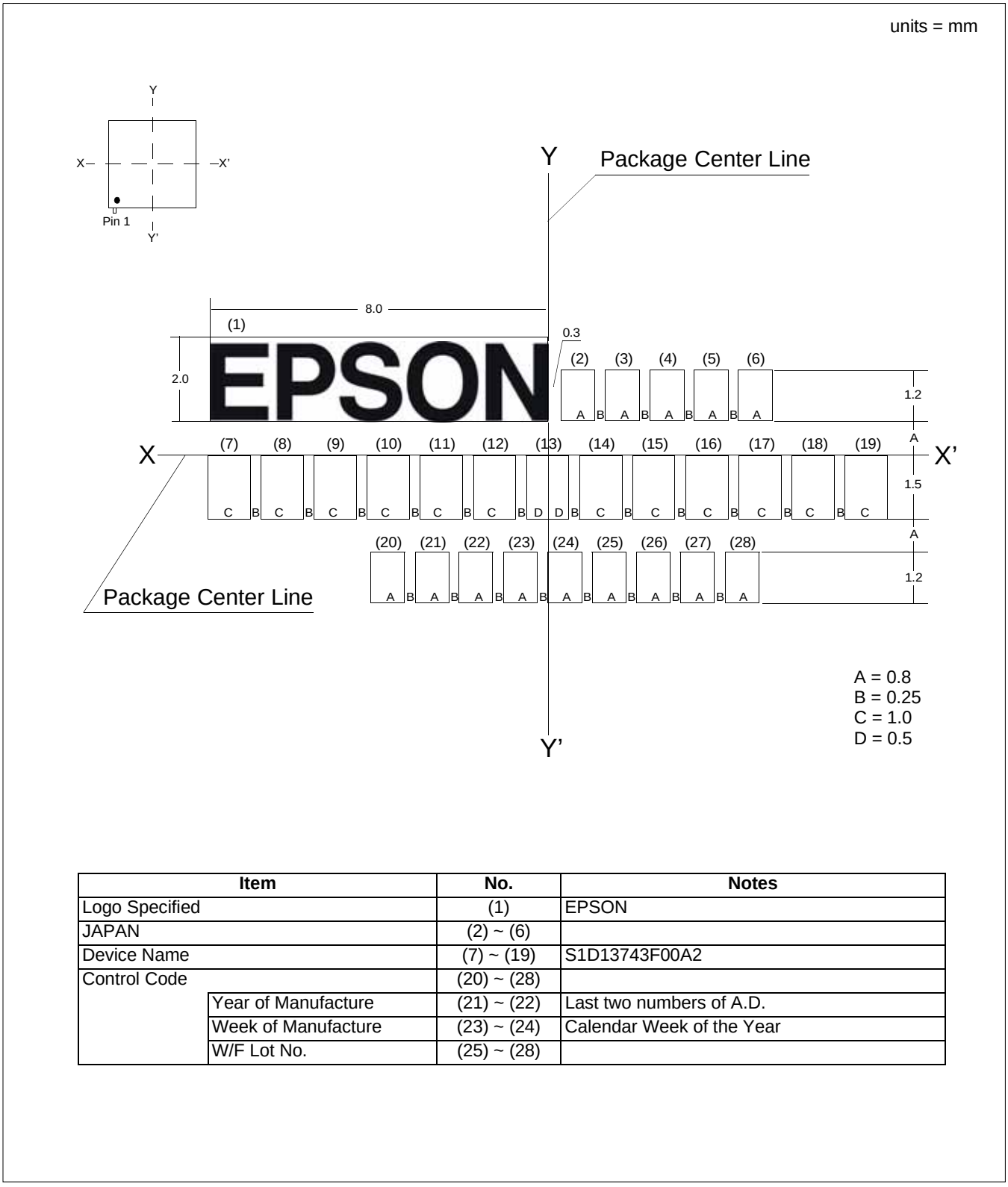
units = mm

Figure 23-2: S1D13743 QFP20 144-pin Package



Item		No.	Notes
Logo Specified		(1)	
Device Name		(2) ~ (5)	
Die Revision Code		(6)	
Package Type		(7)	C: FCBGA
Process and Package Revision Code		(8)	
[Blank]		(9) ~ (10)	
Control Code		(10) ~ (16)	
	Year of Manufacture	(11)	Last number of A.D.
	Month of Manufacture	(12)	1-9: JAN-SEP X: OCT, Y: NOV, Z: DEC
	W/F Lot No.	(13) ~ (16)	
JAPAN		(17) ~ (21)	

Figure 23-3: S1D13743 FCBGA 121-pin Package Marking



Item		No.	Notes
Logo Specified		(1)	EPSON
JAPAN		(2) ~ (6)	
Device Name		(7) ~ (19)	S1D13743F00A2
Control Code		(20) ~ (28)	
	Year of Manufacture	(21) ~ (22)	Last two numbers of A.D.
	Week of Manufacture	(23) ~ (24)	Calendar Week of the Year
	W/F Lot No.	(25) ~ (28)	

Figure 23-4: S1D13743 QFP 144-pin Package Marking

24 References

The following documents contain additional information related to the S1D13743. Document numbers are listed in parenthesis after the document name. All documents can be found at the Epson Research and Development Website at **www.erd.epson.com**.

- S1D13743 Product Brief (X70A-C-001-xx)
- S5U13743P00C100 Evaluation Board User Manual (X70A-G-001-xx)

25 Sales and Technical Support

AMERICA

EPSON ELECTRONICS AMERICA, INC.
2580 Orchard Parkway
San Jose , CA 95131,USA
Phone: +1-800-228-3964 FAX: +1-408-922-0238

EUROPE

EPSON EUROPE ELECTRONICS GmbH
Riesstrasse 15, 80992 Munich,
GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

ASIA

EPSON (CHINA) CO., LTD.
7F, Jinbao Bldg., No.89 Jinbao St.,
Beijing 100005, CHINA
Phone: +86-10-8522-1199 FAX: +86-10-8522-1125

SHANGHAI BRANCH
7F, Block B, High-Tech Bldg., 900, Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5577 FAX: +86-21-5423-4677

SHENZHEN BRANCH
12F, Dawning Mansion, Keji South 12th Road,
Hi-Tech Park, Shenzhen 518057, CHINA
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON HONG KONG LTD.
20/F, Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110, TAIWAN
Phone: +886-2-8786-6688 FAX: +886-2-8786-6660

EPSON SINGAPORE PTE., LTD.
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORP.
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

SEIKO EPSON CORP.
SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.
IC International Sales Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

25.1 Ordering Information

To order the S1D13743 Mobile Graphics Engine, contact the Epson sales representative in your area.

Change Record

X70A-A-001-02 Revision 2.7 - Issued: 2010/05/18

- section 4.2.3 Clocks - remove “Input frequency range: 1MHz ~ 33MHz” from CLKI description
- section 7.1.1 Input Clocks - in table 7-1 Clock Input Requirements (CLKI), change fosc Input clock frequency - PLL used for System Clock max value to “33” from “66”

X70A-A-001-02 Revision 2.6 - Issued: 2009/09/29

- all changes from the last revision are highlighted in Red
- section 6.3 Electrical Characteristics - in Table 6-4, change Operational Peak Current max value to “74 uA”
- section 7.4.3 Generic 18/24-Bit TFT Panel Timing - in figure 7-10, 18/24-Bit TFT A.C. Timing, remove references to 1 pixel/clock and 2 pixel/clock modes, remove VD[23:0] timing waveform, add VD[23:0] to VD[17:0] timing waveform
- section 8 Memory - for Tables 8-1 and 8-2, change red data to odd addresses and green data to even addresses
- section 9.4 Setting SYSCLK and PCLK - add CLKI information to this section
- section 9.4 Setting SYSCLK and PCLK - remove “5 x 9.5” from “For example, if the...”
- section 23 - in Figure 23-1, change Side View ball height to 0.23mm
- section 26 Sales and Technical Support - changes to Epson offices and addresses

X70A-A-001-02 Revision 2.5 - Issued: 2008/05/07

- all changes from the last revision are highlighted in Red
- Set revision to 2.5 to align with Japan revision numbering
- section 8 Memory - add this section and renumber all following sections
- REG[48h] ~ REG[49h] - remove “The data read back from memory will be byte swapped (i.e. if 12 34 56 78 is written to memory, data read back will be 34 12 78 56)” from the first note
- REG[4Ah] ~ REG[4Eh] - add note “If 16-bit interface is used (CNF1 = 1), all reads will...”
- section 12 RGB Input Data Conversion - delete paragraph “The actual data storage is complex due to the memory structure...” and add reference to section 8

X70A-A-001-02 Revision 2.04 - Issued: 2007/09/18

- all changes from the last revision of the spec are highlighted in Red
- section 7.3.1 ~ 7.3.2, added note and clarified the usage of MD[15:8] pins in the Host Timing figures and tables

- section 18.1.3, updated the X/Y Start/End data order in the Sequential Memory Write Example Sequence figure and moved it to section 18.1.3
- section 24, added References
- section 25, added Sales and Technical Support addresses

X70A-A-001-02 Revision 2.03 (Issued 2006/09/25)

- all changes from the last revision of the spec are highlighted in Red
- section 11 RGB Input Data Conversion - add this section and re-number following sections

X70A-A-001-02 Revision 2.02 (Issued 2006/08/23)

- all changes from the last revision of the spec are highlighted in Red
- globally add QFP20 144-pin package information
- section 4.2.4 Miscellaneous - change PWRSVE pin Powersave status to “Pull-down Active” and change description to “This pin has an internal...”
- section 5.2 LCD Interface Data Pins - correct typos in table 5-3, change Hi-Z to Driven Low
- section 6.3 Electrical Characteristics - add table 6-4 Electrical Characteristics for IOVDD or PIOVDD = 3.3V ± 0.3V
- section 7.2 RESET# Timing - add CLKI signal to figure
- section 7.3.1 Intel 80 Interface Timing - 1.8 Volt - rewrite section for 1.8 volts
- section 7.3.2 Intel 80 Interface Timing - 3.3 Volt - add this section

X70A-A-001-02 Revision 2.01 (Issued 2006/04/28)

- all changes from the last revision of the spec are highlighted in Red
- updated EPSON tagline
- section 4.2.1 Intel 80 Host Interface - for GPIO_INT add reference to General Purpose IO Pins Registers to pin description.
- section 4.2.4 Miscellaneous - for GPIO[7:0] rewrite pin description, for PWRSVE rewrite pin description for no pull-down resistor
- section 4.2.4, change SCANEN pin description IO Voltage from “VSS” to “IOVDD”
- section 7.2 RESET# Timing - add this section
- section 17.1.2, for the Host Interface section changed the references in the figure from “D[15:0]” to “MD[15:0]”

X70A-A-001-02 Revision 2.0

- section 6.3 Electrical Characteristics - in table 6-3, define the conditions for Quiescent Current

X70A-A-001-01 Revision 1.07

- All changes from the previous Revision are in red
- section 7.3.3 Generic 18/24-Bit TFT Panel Timing - correct typos in section, change 36-bit to 24-bit, change VD[35:0] to VD[23:0] in figure

X70A-A-001-01 Revision 1.06

- All changes from the previous Revision are in red text
- section 6.3 Electrical Characteristics - table 6-3 Electrical Characteristics for IOVDD or PIOVDD = 1.8V ± 0.15V, break P_{Total} out to separate power types (P_{CORE}, P_{PLL}, P_{PIO}, P_{HIO}) and make change to note under table

X70A-A-001-01 Revision 1.05

- figure 21-2 S1D13743 Package Marking - add process condition change to Package Revision Code
- table 21-1 S1D13743 Product Marking - add ES information to table
- section 22 ESD Test Results - add this section

X70A-A-001-01 Revision 1.04

- section 6.3 Electrical Characteristics - add max value for I_{CORE} and rewrite note at bottom of table

X70A-A-001-01 Revision 1.03

- section 21 Mechanical Data - Table 21-1 S1D13743 Product Marking, correct typo in second row first column - change TS1 to TS2

X70A-A-001-01 Revision 1.02

- section 21 Mechanical Data - add Table 21-1 S1D13743 Product Marking

X70A-A-001-01 Revision 1.01

- section 21 Mechanical Data - add Figure 21-2 S1D13743 Package Marking

X70A-A-001-01 Revision 1.0

- Release as Revision 1.0 (2005/01/18)

X70A-A-001-00 Revision 0.07

- section 4.2.2 LCD Interface - change PCLK RESET# State to CLKI
- section 6 D.C. Characteristics - add PIOVDD to tables and update Table 6-3 Electrical Characteristics, change section 6.2 note “There are no special Power On/Off requirements...” and add section 6.3 note “1. Typical Operating Current Environment...”
- section 7.3.3 18/24-Bit TFT Panel Timing - add t17 and t18 to figure and table, remove t3 min and max, change t3 typ to “HPS”, and correct typo - t8 typ to “HPS” from “HSS” in table
- section 8.4 Setting SYSCLK and PCLK - change first equation to “$14.94ns < T_{SYSCLK} < (T_{BBC} - 0.976) \times 0.485ns$” from “$14.94ns < T_{SYSCLK} < (T_{BBC} - 0.976) \div 2.06ns$”

- REG[04h] - change register name from “PLL M-Divider Register 0” to “PLL M-Divider Register”
- REG[18h] - change minimum register value in note to 3
- REG[2Ah] - add note “For YUV 4:2:2 and YUV 4:2:0 settings, the width...”
- REG[2Ah] - add note “RGB 6:6:6 mode 2 and RGB 8:8:8 mode 2...”
- REG[34h] bits 6-4 - for 000b change FRM Mode Selected to Normal Mode, and add note “When the output is 24 bpp...”
- REG[36h] bit 7 - add note “While double buffering is enabled...”
- REG[36h] bit 6 - add note “While double buffering is enabled...”
- REG[48h] ~ REG[49h] - add note “Data read back from memory will be byte swapped”
- REG[56h] bit 1, fixed reference to REG[56h] bit 7 state, should be “Sleep mode can also be controlled by the PWRSVE pin when REG[56h] bit 7 = 0b.” instead of “Sleep mode can also be controlled by the PWRSVE pin when REG[56h] bit 7 = 1b.”
- REG[56h] bit 0, fixed reference to REG[56h] bit 7 state, should be “Standby mode can also be controlled by the PWRSVE pin when REG[56h] bit 7 = 1b.” instead of “Standby mode can also be controlled by the PWRSVE pin when REG[56h] bit 7 = 0b.”
- REG[58h] bit 6 - swap “When this bit =...” descriptions
- REG[58h] bit 5 - rename bit to “VP OR’d with HDP Status (Read Only)”
- section 12 Intel 80, 16-bit Interface Color Formats - remove color from all Figures in section
- section 13 YUV Timing - add format definition to this section
- section 13 YUV Timing - remove color from all Figures in section
- section 13.1 YUV 4:2:2 with Intel 80, 8-bit Interface, figure 13-1, correct U, V figure
- section 15 Display Data Format - Table 15-3 18-Bit Data Format (Non-Swapped, REG[14h] bit 7 = 0b), and Table 15-4 18-Bit Data Format (Swapped, REG[14h] bit 7 = 1b) change VD[23:18] value from Hi-Z to Low
- section 19.1.2 S1D13743 Register Settings for 352x416 TFT Panel - change REG[06h] value to F8h and REG[0Ah] value to 28h
- section 19.1.2 S1D13742 Register Settings for 352x416 TFT Panel - add note “When a window is setup for YUV data...”

X70A-A-001-00 Revision 0.06

- figure 4-1, changed “S1D13743 Proposed Pinout...” to “S1D13743 Pinout...”
- section 7.1.1 Input Clocks - Table 7-1 Clock Input Requirements (CLKI) - change fOSC Input clock frequency - PLL used for System Clock max to 66 MHz
- section 7.3, corrected the formulas for HNDP (should be “REG[18h] bits 6-0” instead of “REG[18h] bits 5-0”), HSW (should be “REG[20h] bits 6-0” instead of “REG[20h] bits 5-0”), and VSW (should be “REG[24h] bits 5-0” instead of “REG[24h] bits 6-0”)

- section 7.3.1, added information about PWRSVE pin to TFT Power-On sequence note 1
- section 7.3.1, in second note changed LCD pins VD[35:0] to VD[23:0]
- section 7.3.2, added information about PWRSVE pin to TFT Power-Off sequence note 1
- section 7.3.2, in second note changed LCD pins VD[35:0] to VD[23:0]
- section 7.3.3, added 18-bit panel data (VD[17:0])
- section 7.3.3, fixed REG reference for PCLK Polarity, should be “REG[28h] bit 7” instead of “REG[2Ah] bit 7”
- section 8.1, removed arrow pointing down from the Clock Source Select
- section 9.2, added register set summary table
- REG[04h] bits 5-0, updated the M-Divide Ratio table to read “REG[04h] bits 5-0” instead of “bits 6-0” and changed the maximum value from 7Fh to 3Fh
- REG[06h] ~ REG[0Ch], changed the bit descriptions for the PLL Setting Registers 0-3, reserved all individual bit descriptions and added specific programming values for each register
- REG[14h] bit 7, combined the note under the VD Data Swap bit into the main bit description and added references to the exact tables
- REG[2Ah] - remove text “bit 7-4 Reserved”
- REG[2Ch] bit 6, updated the YRC Reset bit description
- REG[34h] bit 7, updated the Display Blank bit description
- REG[48h] ~ REG[49h], changed the default value for the Memory Data Port Registers to “not applicable”
- REG[54h], changed the default value for the Gamma Correction Table Data Register to “not applicable”
- REG[58h] bit 4, updated the YYC Last Line bit description and removed reference to the MESSI interface (should be Intel 80 interface)
- REG[5Ah] ~ REG[64h], minor wording clarifications to the GPIO registers
- section 10, changed “Horizontal Period” to “Horizontal Display Width” and “Vertical Period” to “Vertical Display Height”
- section 10, added cross reference to Display Interface timing section for Panel Timing Parameter definitions
- section 11, updated the Intel 80, 8-bit Interface Color Formats diagrams to use the proper 13743 pin names
- section 12, updated the Intel 80, 16-bit Interface Color Formats diagrams to use the proper 13743 pin names
- section 13, updated the YUV Timing diagrams to use the proper 13743 pin names
- section 14, added data input to LUT

- section 14.1, reworded some of the steps in the Gamma Correction Programming Example
- section 17, minor wording changes to clarify the Host Interface usage examples

X70A-A-001-00 Revision 0.05

- section 7.1.1 Input Clocks - Table 7-1 Clock Input Requirements (CLKI) - change Input clock frequency - PLL max to 66.53 MHz, and Input clock frequency - CLKI max to 68.59 MHz.
- section 7.1.2 PLL Clock - change all PLL output min to 44.28 MHz. and all PLL output max to 66.53 MHz,
- section 7.2.1 Intel 80 Interface Timing - Table 7-3 Intel 80 Input A.C. Characteristics - change t_{odh} min to 11.0, and t_{ddt} min to 2.7 and max to 18.0
- section 8.4 Setting SYSCLK and PCLK - change first equation to "15.03ns < T_{SYSCLK} < (T_{BBC} - 0.976) ÷ 2.06 ns", second equation to "15.03ns < T_{SYSCLK} < 22.584ns", and third equation to "44.28MHz < f_{SYSCLK} < 66.53MHz"

X70A-A-001-00 Revision 0.04

- section 2.6 Display Features -change third bullet text paragraph "... must fit inside 232K bytes..." to "... must fit inside 228K bytes..."
- section 7.1.1 Input Clocks - Table 7-1 Clock Input Requirements (CLKI) - change f_{OSC} Max, t3 max, t4 max, t5 min/max, t6 min/max, add note 6
- section 7.1.2 PLL Clock - Figure 7-2 PLL Start-Up Time, Table 7-2 PLL Clock Requirements - change PLL output to min 44.26, max 66.95
- section 7.2.1 Intel 80 Interface Timing - Table 7-3 Intel 80 Input A.C. Characteristics - change t_{odh} and t_{ddt} min and max
- section 8.4 Setting SYSCLK and PCLK - replace numbers in equations with new, replace Figure 8-3 Setting of SYSCLK for a Desired PCLK
- section 9 Registers - correct register address typos in introduction
- section 9.1 Register Mapping- correct register address typos
- REG[18h] - add to note "Minimum value of this register = 4 Pixels"
- REG[34h] - add bits 6-3 and change register default to 08h
- REG[54h] - change register default to ??h
- section 17 Host Interface - correct register address typos in introduction note
- section 17.1.5 Individual Memory Location Reads - delete step 1 and re-number steps, changes to note

X70A-A-001-00 Revision 0.03

- Engineering changes added

X70A-A-001-00 Revision 0.01

- initial draft of the S1D13743 specification

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Display Drivers & Controllers ***category:***

Click to view products by Epson ***manufacturer:***

Other Similar products are found below :

ICB2FL01G HV5812PJ-G-M904 TW8813-LB2-GR TW8811-PC2-GR MAX1839EEP+ TW9907-TA1-GR LX27901IDW SSD2828QN4 ICB2FL01GXUMA2 DLP2000FQC PAD1000YFFR S1D13746F01A600 FIN324CMLX AD8387JSVZ DLPC6421ZPC HV852K7-G HV859K7-G HV857K7-G DIO2133CT14 S1D13506F00A200 S1D13L03F00A100-40 TW2836-BA1-GR SSD2829QL9 MAX749CSA+T MAX4820EUP+T ICL7135CAI+ ICL7135CMH+D ICL7137CMH+D MAX25221BATJ/V+ S1D13748B00B100 MAX3738ETG+T MAX8722CEEG+ MAX749CPA+ MAX8785AETI+ ICL7135CQI+ HV518PJ-G-M903 HV5812P-G HV5812PJ-G HV5812WG-G HV7224PG-G HV853K7-G HV860K7-G HV6810WG-G HV857MG-G HV833MG-G HV857LMG-G HV850MG-G HV859MG-G FMS6363ACSX FMS6364AMTC14X