MF1444-04

S1D15711 Series

Rev.1.0a

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1. DESCRIPTION

The S1D15711 Series is a single-chip dot matrix liquid crystal display driver that can be connected directly to a microprocessor bus. Eight-bit parallel or serial display data transmitted from the microprocessor is stored in the internal display data RAM, and the chip generates liquid crystal drive signals, independently of the microprocessor.
It has a on-chip 9 × 200-bits display data RAM, and there is a one-to-one correspondence between the dot pixel on the liquid crystal panel pixels and internal RAM bit. This feature ensures implementation of highly free display.
The S1D15711 Series incorporate 9 common and 200 segment driver circuits. A single chip can drive a 9 × 200 dots display. Further, display capacity can be extended by designing two chips in a master/slave configuration.
The S1D15711 Series can read and write RAM data with the minimum current consumption because it does not require any external operation clock. Also it incorporates a LCD power supply featuring a very low current consumption, a LCD drive power voltage regulator resistor and a display clock CR oscillator circuit. This allows the display system of a high-performance for handy equipment to be realized at the minimum power consumption and minimum component configuration.

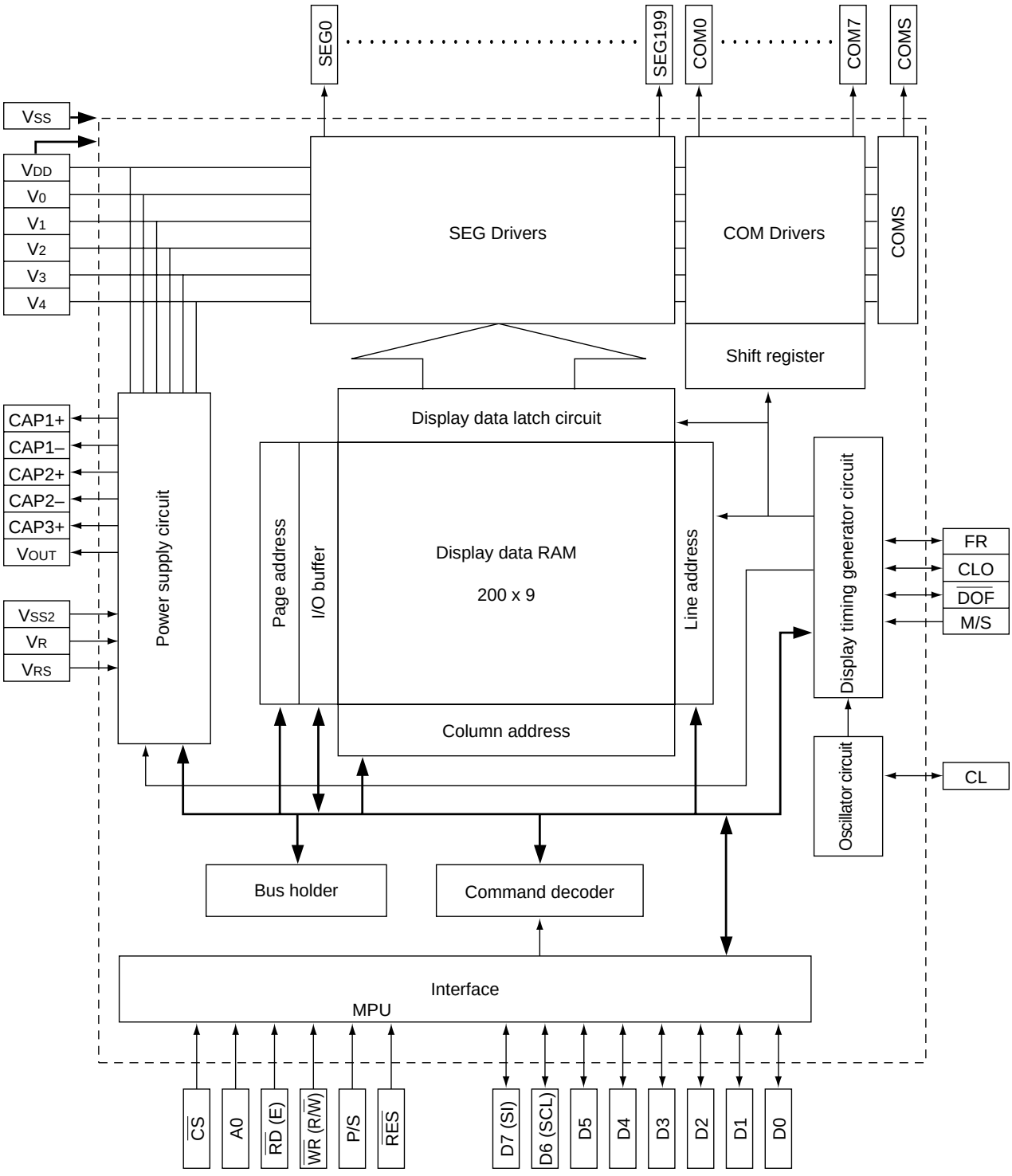
2. FEATURES

- Direct display of RAM data using the display data RAM
  RAM bit data "1" .... goes on.
  "0" .... goes off (at display normal rotation).
- RAM capacity
  9 × 200 = 1,800 bits
- Liquid crystal drive circuits
  9 common outputs and 200 segment outputs
- High-speed 8-bit MPU interface (Both the 80 and 68 series MPUs can directly be connected.)/serial interface enabled
- Abundant command functions
  Display Data Read/Write, Display ON/OFF, Display Normal Rotation/Reversal, Page Address Set, Display Start Line Set, column address set, Power Supply Save Display All Lighting ON/OFF, LCD Bias Set, Read Modify Write, Segment Driver Direction Select, Electronic Control, V_0 Voltage Adjusting Built-in Resistance Ratio Set, Static Indicator, n Line Alternating Current Reversal Drive, and Common Output State Selection
- Built-in power supply circuit for low power supply liquid crystal drive
  Booster circuit (Boosting magnification - double, triple, quadruple, boosting reference power supply external input enabled)
- High accuracy alternating current voltage adjusting circuit (Temperature gradient: –0.05%/°C)
  Built-in V_0 voltage adjusting resistor, built-in V_1 to V_4 voltage generation split resistors, built-in electronic control function, and voltage follower
- Built-in CR oscillator circuit (external clock input enabled)
- Power supplies
  Logic power supply: $V_{DD} – V_{SS}$ = 1.8 to 5.5 V
  Boosting reference power supply: $V_{DD} – V_{SS}$ = 1.8 to 5.0 V
  Liquid crystal drive power supply: $V_0 – V_{DD}$ = 4.5 to 9.0 V
- Wide operating temperature range –40 to +85°C
- CMOS process
- Shipping form: Bare chip
- No light-resistant and radiation-resistant design are provided.

Series specification

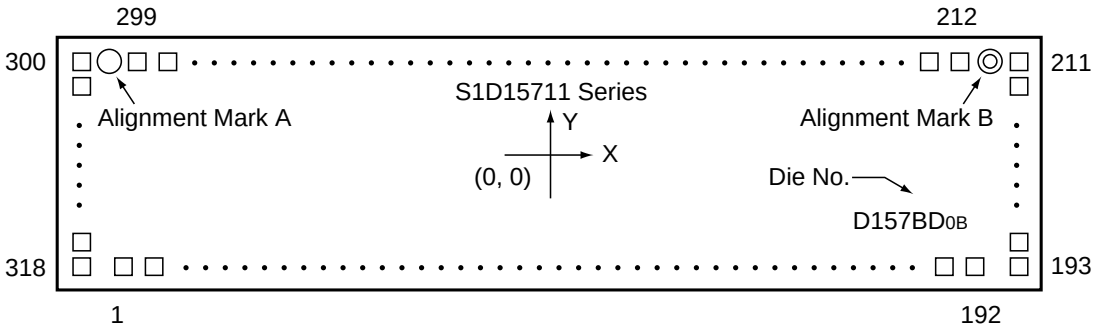
Product name	Duty	Bias	SEG Dr	COM Dr	V_{REG} temperature gradient	Shipping form	Bump height
S1D15711D00B000	1/9	1/5, 1/6	200	9	–0.1%/°C	Bare chip	17.0μm Typ.
S1D15711D00C000	1/9	1/5, 1/6	200	9	–0.1%/°C	Bare chip	22.5μm Typ.

3. BLOCK DIAGRAM



4. PAD ASSIGNMENT

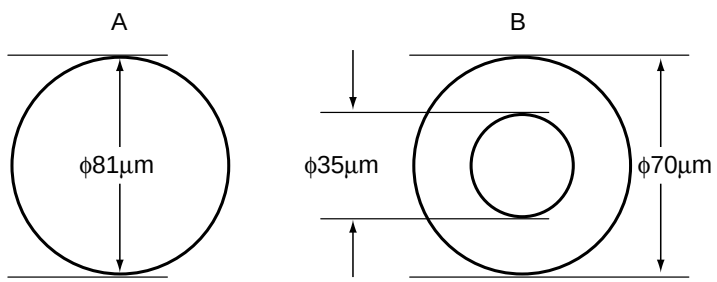
Chip Specification



Chip Outline, Bump

Item		Size X		Size Y	Unit
Chip size		11.92	×	1.85	mm
Chip thickness		0.625			mm
Bump pitch		60 (Min.)			μm
Bump size	PAD No.1	85	×	74	μm
	PAD No.2 to 189	41	×	85	μm
	PAD No.190	85	×	74	μm
	PAD No.191 to 210	85	×	45	μm
	PAD No.211	85	×	74	μm
	PAD No.212 to 299	85	×	85	μm
	PAD No.300	85	×	74	μm
	PAD No.301 to 318	85	×	45	μm
Bump height		17 (Typ.) or 22.5 (Typ.)			μm

Alignment Marks

Center coordinates (x, y)	A : (-5616μm, 770μm), B : (5616μm, 770μm)
Size	

Pad Central Coordinates

Unit: µm

Pad No.	Pin Name	X	Y
1	NC	–5807	–776
2	NC	–5658	–770
3	NC	–5598	
4	NC	–5539	
5	SEG0	–5479	
6	SEG1	–5419	
7	SEG2	–5359	
8	SEG3	–5299	
9	SEG4	–5239	
10	SEG5	–5180	
11	SEG6	–5120	
12	SEG7	–5060	
13	SEG8	–5000	
14	SEG9	–4940	
15	SEG10	–4880	
16	SEG11	–4821	
17	SEG12	–4761	
18	SEG13	–4701	
19	SEG14	–4641	
20	SEG15	–4581	
21	SEG16	–4521	
22	SEG17	–4461	
23	SEG18	–4402	
24	SEG19	–4342	
25	SEG20	–4282	
26	SEG21	–4222	
27	SEG22	–4162	
28	SEG23	–4102	
29	SEG24	–4043	
30	SEG25	–3983	
31	SEG26	–3923	
32	SEG27	–3863	
33	SEG28	–3803	
34	SEG29	–3743	
35	SEG30	–3684	
36	SEG31	–3624	
37	SEG32	–3564	
38	SEG33	–3504	
39	SEG34	–3444	
40	SEG35	–3384	
41	SEG36	–3325	
42	SEG37	–3265	
43	SEG38	–3205	
44	SEG39	–3145	
45	SEG40	–3085	
46	SEG41	–3025	
47	SEG42	–2965	
48	SEG43	–2906	
49	SEG44	–2846	
50	SEG45	–2786	
51	SEG46	–2726	–770
52	SEG47	–2666	
53	SEG48	–2606	
54	SEG49	–2547	
55	SEG50	–2487	
56	SEG51	–2427	
57	SEG52	–2367	
58	SEG53	–2307	
59	SEG54	–2247	
60	SEG55	–2188	
61	SEG56	–2128	
62	SEG57	–2068	
63	SEG58	–2008	
64	SEG59	–1948	
65	SEG60	–1888	
66	SEG61	–1829	
67	SEG62	–1769	
68	SEG63	–1709	
69	SEG64	–1649	
70	SEG65	–1589	
71	SEG66	–1529	
72	SEG67	–1469	
73	SEG68	–1410	
74	SEG69	–1350	
75	SEG70	–1290	
76	SEG71	–1230	
77	SEG72	–1170	
78	SEG73	–1110	
79	SEG74	–1051	
80	SEG75	–991	
81	SEG76	–931	
82	SEG77	–871	
83	SEG78	–811	
84	SEG79	–751	
85	SEG80	–692	
86	SEG81	–632	
87	SEG82	–572	
88	SEG83	–512	
89	SEG84	–452	
90	SEG85	–392	
91	SEG86	–333	
92	SEG87	–273	
93	SEG88	–213	
94	SEG89	–153	
95	SEG90	–93	
96	SEG91	–33	
97	SEG92	27	
98	SEG93	86	
99	SEG94	146	
100	SEG95	206	
101	SEG96	266	–770
102	SEG97	326	
103	SEG98	386	
104	SEG99	445	
105	SEG100	505	
106	SEG101	565	
107	SEG102	625	
108	SEG103	685	
109	SEG104	745	
110	SEG105	804	
111	SEG106	864	
112	SEG107	924	
113	SEG108	984	
114	SEG109	1044	
115	SEG110	1104	
116	SEG111	1163	
117	SEG112	1223	
118	SEG113	1283	
119	SEG114	1343	
120	SEG115	1403	
121	SEG116	1463	
122	SEG117	1523	
123	SEG118	1582	
124	SEG119	1642	
125	SEG120	1702	
126	SEG121	1762	
127	SEG122	1822	
128	SEG123	1882	
129	SEG124	1941	
130	SEG125	2001	
131	SEG126	2061	
132	SEG127	2121	
133	SEG128	2181	
134	SEG129	2241	
135	SEG130	2300	
136	SEG131	2360	
137	SEG132	2420	
138	SEG133	2480	
139	SEG134	2540	
140	SEG135	2600	
141	SEG136	2659	
142	SEG137	2719	
143	SEG138	2779	
144	SEG139	2839	
145	SEG140	2899	
146	SEG141	2959	
147	SEG142	3019	
148	SEG143	3078	
149	SEG144	3138	
150	SEG145	3198	

Unit: µm

Pad No.	Pin Name	X	Y
151	SEG146	3258	–770
152	SEG147	3318	
153	SEG148	3378	
154	SEG149	3437	
155	SEG150	3497	
156	SEG151	3557	
157	SEG152	3617	
158	SEG153	3677	
159	SEG154	3737	
160	SEG155	3796	
161	SEG156	3856	
162	SEG157	3916	
163	SEG158	3976	
164	SEG159	4036	
165	SEG160	4096	
166	SEG161	4155	
167	SEG162	4215	
168	SEG163	4275	
169	SEG164	4335	
170	SEG165	4395	
171	SEG166	4455	
172	SEG167	4515	
173	SEG168	4574	
174	SEG169	4634	
175	SEG170	4694	
176	SEG171	4754	
177	SEG172	4814	
178	SEG173	4874	
179	SEG174	4933	
180	SEG175	4993	
181	SEG176	5053	
182	SEG177	5113	
183	SEG178	5173	
184	SEG179	5233	
185	SEG180	5292	
186	SEG181	5352	
187	SEG182	5412	
188	SEG183	5472	
189	NC	5532	
190	NC	5807	–770
191	NC	5592	–770
192	NC	5651	–776
193	NC	5807	–681
194	SEG184		–601
195	SEG185		–520
196	SEG186		–440
197	SEG187		–360
198	SEG188		–280
199	SEG189		–200
200	SEG190		–120

Pad No.	Pin Name	X	Y
201	SEG191	5807	–40
202	SEG192		40
203	SEG193		120
204	SEG194		200
205	SEG195		280
206	SEG196		360
207	SEG197		440
208	SEG198		520
209	SEG199		601
210	NC		681
211	NC		776
212	NC	5411	770
213	NC	5291	
214	NC	5170	
215	NC	5049	
216	TEST0	4928	
217	TEST1	4808	
218	V_{SS}	4687	
219	V_{SS}	4566	
220	TEST2	4446	
221	TEST3	4325	
222	FR	4204	
223	CLO	4084	
224	$\overline{DOF}$	3963	
225	$\overline{RES}$	3842	
226	$\overline{CS}$	3721	
227	V_{SS}	3601	
228	V_{SS}	3480	
229	CL	3359	
230	$\overline{WR}$, R/$\overline{W}$	3239	
231	$\overline{RD}$, E	3118	
232	V_{DD}	2997	
233	V_{DD}	2877	
234	A0	2756	
235	D7	2635	
236	D6	2514	
237	D5	2394	
238	D4	2273	
239	D3	2152	
240	D2	2032	
241	D1	1911	
242	D0	1790	
243	D7	1670	
244	V_{DD}	1549	
245	V_{DD}	1428	
246	V_{DD2}	1307	
247	V_{DD2}	1187	
248	V_{DD2}	1066	
249	V_{DD2}	945	
250	V_{DD}	825	

Pad No.	Pin Name	X	Y
251	V_{DD}	704	770
252	P/S	583	
253	C86	463	
254	V_{SS}	342	
255	V_{SS}	221	
256	M/S	100	
257	V_{DD}	–20	
258	V_{DD}	–141	
259	TEST4	–318	
260	TEST5	–495	
261	TEST6	–671	
262	V_{SS}	–792	
263	V_{SS}	–913	
264	V_{SS}	–1033	
265	TEST7	–1210	
266	TEST8	–1387	
267	TEST9	–1564	
268	TEST10	–1741	
269	V_{OUT}	–1861	
270	V_{OUT}	–1982	
271	V_{SS}	–2103	
272	V_{SS}	–2223	
273	V_R	–2344	
274	V_0	–2465	
275	V_1	–2586	
276	V_2	–2706	
277	V_3	–2827	
278	V_4	–2948	
279	V_{DD}	–3068	
280	V_{DD}	–3189	
281	V_{DD2}	–3310	
282	V_{DD2}	–3430	
283	V_{OUT}	–3551	
284	V_{OUT}	–3672	
285	CAP2+	–3793	
286	CAP2+	–3913	
287	CAP2–	–4034	
288	CAP2–	–4155	
289	CAP1+	–4275	
290	CAP1+	–4396	
291	CAP1–	–4517	
292	CAP1–	–4637	
293	CAP3+	–4758	
294	CAP3+	–4879	
295	V_{OUT}	–5000	
296	V_{OUT}	–5120	
297	NC	–5241	
298	NC	–5362	
299	NC	–5482	
300	NC	–5807	776

Unit: μm

Pad No.	Pin Name	X	Y
301	COMS	–5807	681
302	COM7		601
303	COM7		520
304	COM6		440
305	COM6		360
306	COM5		280
307	COM5		200
308	COM4		120
309	COM4		40
310	COM3		–40
311	COM3		–120
312	COM2		–200
313	COM2		–280
314	COM1		–360
315	COM1		–440
316	COM0		–520
317	COM0		–601
318	COMS		–681

5. PIN DESCRIPTION

Power Supply Pin

Pin name	I/O	Description	Number of pins
V_{DD}	Power supply	Commonly used with the MPU power supply pin V_{CC}.	10
V_{SS}	Power supply	0 V pin connected to the system ground (GND)	11
V_{DD2}	Power supply	Boosting circuit reference power supply for liquid crystal drive	6
V_0, V_1, V_2 V_3, V_4	Power supply	Multi-level power supply for liquid crystal drive. The voltage specified according to liquid crystal cells is impedance-converted by a split resistor or operation amplifier (OP amp) and applied. The potential needs to be specified based on V_{SS} to establish the relationship of dimensions shown below: $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$ Master operation When the power supply is ON, the following voltages are applied to V_1 to V_4 from the built-in power supply circuit. The selection of the voltages is determined using the LCD bias set command. V_1 4/5•V_0 5/6•V_0 V_2 3/5•V_0 4/6•V_0 V_3 2/5•V_0 2/6•V_0 V_4 1/5•V_0 1/6•V_0	1 each

LCD Power Supply Circuit Pin

Pin name	I/O	Description	Number of pins
CAP1+	O	Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP1– pin.	2
CAP1–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1+ pin.	2
CAP2+	O	Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP2– pin.	2
CAP2–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP2+ pin.	2
CAP3+	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1– pin.	2
V_{OUT}	I/O	Boosting output pin. Connects a capacitor between the pin and V_{DD2}.	6
V_R	I	Voltage adjusting pin. Applies voltage between V_0 and V_{SS} using a split resistor. Valid only when the V_0 voltage adjusting internal resistor is not used V_0 resistance ratio set command (D2, D1, D0) = (1, 1, 1) To use a resistor for adjusting the V_0 voltage, open the circuit.	1

System Bus Connecting Pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>D7 to D0
(SI)
(SCL)</td><td>I/O</td><td>An 8-bit bidirectional data bus is used to connect an 8-bit or 16-bit standard MPU data bus.
When the serial interface is selected (P/S=LOW),
D7: Serial data entry pin (SI)
D6: Serial clock input pin (SCL)
In this case, D0 to D5 are set to high impedance.
When Chip Select is in the non-active state, D0 to D7 are set to high impedance.</td><td>9</td></tr>
<tr><td>A0</td><td>I</td><td>Normally the lowest order bit of the MPU address bus is connected to discriminate data / commands.
A0=HIGH: Indicates that D0 to D7 are display data.
A0=LOW: Indicates that D0 to D7 are control data.</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Initialized by setting $\overline{RES}$ to LOW.
Reset operation is performed at the $\overline{RES}$ signal level.</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>Chip Select signal. When $\overline{CS}$=LOW, this signal becomes active and the input/output of data/commands is enabled.</td><td>1</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>• When the 80 series MPU is connected, active LOW is set.
Pin that connects the $\overline{RD}$ signal of the 80 series MPU. When this signal is LOW, the S1D15711 Series data bus is set in the output state.
• When the 68 series MPU is connected, active HIGH is set.
68 series MPU enable clock input pin</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>• When the 80 series MPU is connected, active LOW is set.
Pin that connects the $\overline{WR}$ signal of the 80 series MPU. The data bus signal is latched on the leading edge of the $\overline{WR}$ signal.
• When the 68 series MPU is connected,
Read/write control signal input pin
R/$\overline{W}$=HIGH: Read operation
R/$\overline{W}$=LOW: Write operation</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>MPU interface switching pin
C86=HIGH: 68 series MPU interface
C86=LOW: 80 series MPU interface</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Switching pin for parallel data entry/serial data entry
P/S=HIGH: Parallel data entry
P/S=LOW: Serial data entry
According to the P/S state, the following table is given.
<table>
<tr><th>P/S</th><th>Data/ command</th><th>Data</th><th>Read/write</th><th>Serial clock</th></tr>
<tr><td>HIGH</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td></td></tr>
<tr><td>LOW</td><td>A0</td><td>SI (D7)</td><td>Write-only</td><td>SCL (D6)</td></tr>
</table>
When P/S=LOW, D0 to D5 are set to high impedance. D0 to D5 can be HIGH, LOW, or “OPEN”.
$\overline{RD}$(E) and $\overline{WR}$ (R/$\overline{W}$) are fixed to HIGH or LOW.
For the serial data entry, RAM display data cannot be read.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CL</td><td>I</td><td>Pin that selects the validity/invalidity of the built-in oscillator circuit for display clocks.
CL=HIGH: Built-in oscillator circuit valid
The display clock can also be input from outside the CL Pin.
To stop the external clock, fix the CL Pin to LOW.
When the S1D15711 Series is used for the master/slave configuration, fix the slave side to LOW.</td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>Pin that selects the master/slave operation for the S1D15711 Series. The liquid crystal display system is synchronized by outputting the timing signal required for the liquid crystal display for the master operation and inputting the timing signal required for the liquid crystal display for the slave operation.
M/S=HIGH: Master operation
M/S=LOW: Slave operation
According to the M/S and CL states, the following table is given.
<table>
<tr><th>M/S</th><th>CL</th><th>Oscillator circuit</th><th>Power supply circuit</th><th>CLO</th><th>FRS</th><th>DOF</th></tr>
<tr><td>HIGH</td><td>HIGH
LOW</td><td>Valid
Invalid</td><td>Valid
Valid</td><td>Output
Output</td><td>Output
Output</td><td>Output
Output</td></tr>
<tr><td>LOW</td><td>LOW</td><td>Invalid</td><td>Invalid</td><td>Input</td><td>Input</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CLO</td><td>I/O</td><td>Display clock I/O pin
According to the M/S and CLS states, the following table is given.
When the S1D15711 Series is used for the master/slave configuration, each CLO pin is connected.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td>HIGH</td><td>HIGH
LOW</td><td>Output
Output</td></tr>
<tr><td>LOW</td><td>LOW</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>Liquid crystal alternating current signal I/O pin
M/S=HIGH: Output
M/S=LOW: Input
When the S1D15711 Series is used for the master/slave configuration, each FR pin is connected.</td><td>1</td></tr>
<tr><td>$\overline{DOF}$</td><td>I/O</td><td>Liquid crystal display blanking control pin
M/S=HIGH: Output
M/S=LOW: Input
When the S1D15711 Series is used for the master/slave configuration, each $\overline{DOF}$ pin is connected.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>SEG0
to
SEG199</td><td>O</td><td>Output pins for the LCD segment drive. Contents of the display RAM and FR signal are combined to select a desired level among V_0, V_2, V_3 and V_{SS}.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">FR</th><th colspan="2">Output voltage</th></tr>
<tr><th>Display normal operation</th><th>Display reversal</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_0</td><td>V_2</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_{SS}</td><td>V_3</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_2</td><td>V_0</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_3</td><td>V_{SS}</td></tr>
<tr><td>Power save</td><td>—</td><td>V_{SS}</td><td></td></tr>
</table></td><td>200</td></tr>
<tr><td>COM0
to
COM7</td><td>O</td><td>Output pins for the LCD common drive. Scan data and FR signal are combined to select a desired level among V_0, V_1, V_4 and V_{SS}.
<table>
<tr><th>Scanning data</th><th>FR</th><th>Output voltage</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_{SS}</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_0</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_1</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_4</td></tr>
<tr><td>Power save</td><td>—</td><td>V_{DD}</td></tr>
</table></td><td>8</td></tr>
<tr><td>COMS</td><td>O</td><td>Indicator dedicated COM output pin
Set to OPEN when not used
When COMS is used for the master/slave configuration, the same signal is output to both the master and slave.</td><td>2</td></tr>
</table>

Test Pin

Pin name	I/O	Description	Number of pins
TEST 1 to TEST 10	I	Pins for testing IC chips. Use care to keep these pins free from loads like capacity and set them to OPEN.	11

Total : 291 pins

6. FUNCTION DESCRIPTION

MPU Interface

Selection of interface type

The S1D15711 Series transfers data through 8-bit bidirectional data buses (D7 to D0) or serial data input (SI). By setting the polarity of the P/S pin to either HIGH or LOW, the 8-bit parallel data entry or serial data entry can be selected as listed in Table 1.

Table 1

P/S	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
HIGH: Parallel data entry	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
LOW: Serial data entry	$\overline{CS}$	A0	—	—	—	SI	SCL	(HZ)

Fix — to HIGH or LOW . HZ indicates the high impedance state.

Parallel interface

When the parallel interface is selected (P/S=HIGH), the S1D15711 Series can directly be connected to the MPU bus of either the 80 or 68 series MPU by setting the C86 pin to HIGH or LOW as listed in Table 2.

Table 2

C86	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
HIGH: 68 series MPU bus	$\overline{CS}$	A0	E	R/$\overline{W}$	D7 to D0
LOW: 80 series MPU bus	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

In addition, the data bus signal can be identified according to the combinations of the A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals as listed in Table 3.

Table 3

Common	68 series	80 series		
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	Function
1	1	0	1	Display data read
1	0	1	0	Display data write
0	0	1	0	Control data write (command)

Serial interface

When the serial interface is selected (P/S=LOW), the serial data entry (SI) and serial clock input(SCL) can be accepted with the chip in the non-active state ($\overline{CS}$=LOW). The serial interface consists of an 8-bit shift register and a 3-bit counter. Serial data is fetched from the serial data entry pin in the order of D7, D6, ..., and D0 on the leading edge of the serial clock and converted into 8-bit parallel data on the leading edge of the 8th serial clock, then processed.
Whether to identify that the serial data entry is display data or command is judged by the A0 input, and A0=HIGH indicates display data and A0=LOW indicates the command. After the chip is set to the non-active state, the A0 input is read and identified at the timing on the 8 × n-th leading edge of the serial clock. Fig. 1 shows the signal chart of the serial interface.

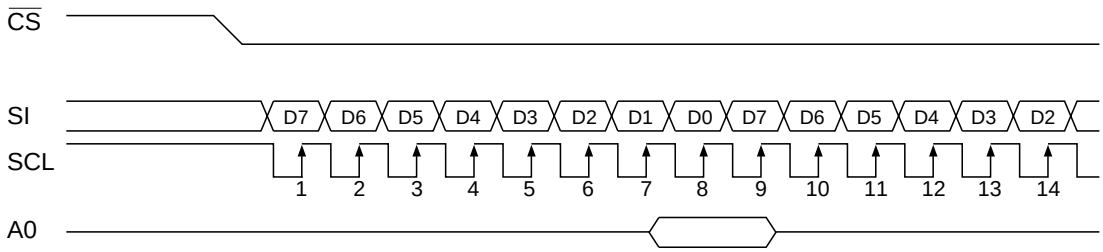


Fig. 1

- When the chip is in the non-active state, both the shift register and counter are reset to the initial state.
- Cannot be read for the serial interface.
- For the SCL signal, pay careful attention to the terminating reflection of lines and external noise. The operation confirmation using actual equipment is recommended.

Chip select

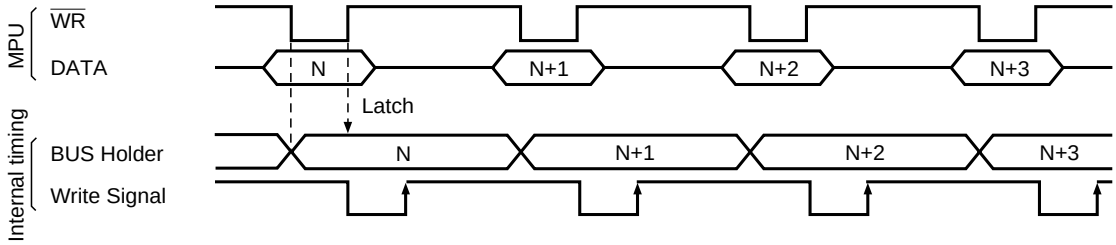
The S1D15711 Series has a chip select pins $\overline{CS}$ and enables the MPU interface or serial interface only when $\overline{CS}$=LOW.
When Chip Select is in the non-active state, D0 to D7 are in the high impedance state and the A0, $\overline{RD}$, and $\overline{WR}$ inputs become invalid. When the serial interface is selected, the shift register and counter are reset.

Display data RAM and internal register access

Since the S1D15711 Series access viewed from the MUP side satisfies the cycle time and does not require the wait time, high-speed data transfer is enabled.
The S1D15711 Series performs a kind of inter-LSI pipeline processing through the bus holder attached to the internal data bus when it performs the data transfer with the MPU.
For example, when data is written on the display data RAM, the data is first held in the bus holder and written on the display data RAM up to the next data write cycle. Further, when the MPU reads the contents of display data RAM, the read data at the first data read cycle (dummy) is held in the bus holder and read on the system bus from the bus holder up to the next data read cycle. The read sequence of the display data RAM is restricted. When the address is set, note that the specified address data is not output to the subsequent read instruction and output at the second data read. Therefore single dummy read is required after the address set and write cycle. Fig. 2 shows this relationship.

Function description

• Write



• Read

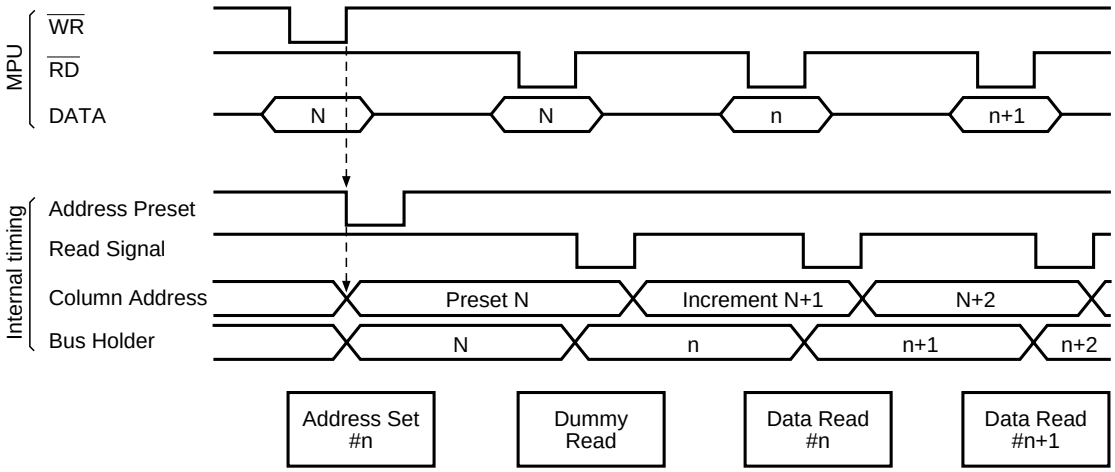


Fig. 2

Display Data RAM

Display data RAM

This display data RAM stores display dot data and consists of 9 (1 pages × one 8 bit + 1) × 200 bits. Desired bits can be accessed by specifying page and column addresses.
Since the MPU display data D7 to D0 correspond to the common direction of the liquid crystal display, the restrictions at display data transfer is reduced and the display configuration with the high degree of freedom can easily be obtained when the S1D15711 Series is used for the multiple chip configuration.
Besides, the read/write operation to the display data RAM is performed through the I/O buffer from the MPU side independently of the liquid crystal drive signal read. Therefore even when the display data RAM is asynchronously accessed during liquid crystal display, the access will not have any adverse effect on the display such as flickering.

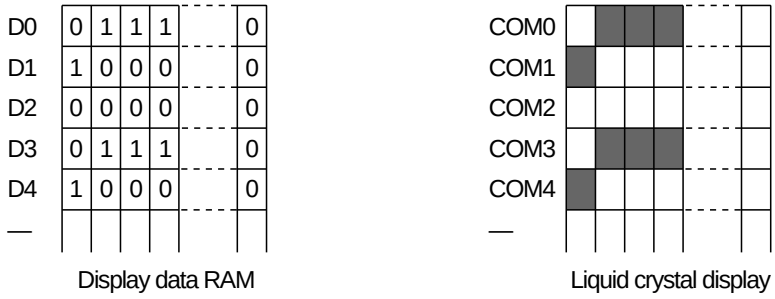


Fig. 3

Page address circuit

As shown in Fig. 4, the page address of the display data RAM is specified using the page address set command. To access the data using a new page, the page address is respecified.
The page address 1 (D0=1) is an indicator dedicated RAM area and only the display data D0 is valid.

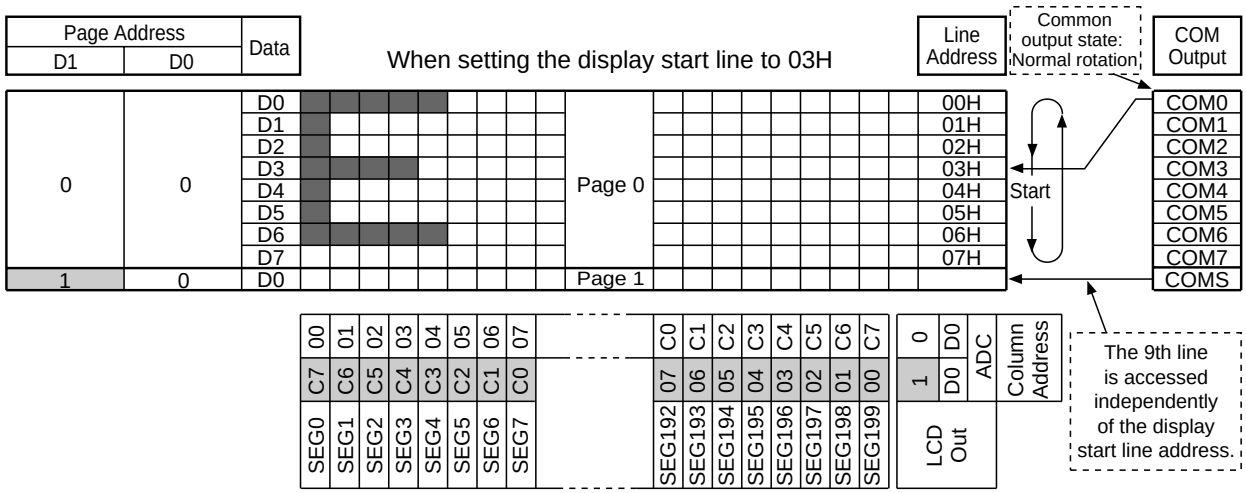


Fig. 4

Column address circuit

As shown in Fig. 5, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented by +1 at every input of display data read/write command. This allows the MPU to access the display data continuously.

After the last column address C7H is accessed, the column address returns to 00H. Since the page address is not automatically incremented, for example, the page address and the column address needs to be re-specified respectively to shift from the column C7H of page 0 to the column 00H of page 1.

Furthermore, as shown in Table 4, the AD command (segment driver direction select command) can used to reverse the correspondence between the display data RAM column address and segment output. This allows constraints on IC layout to be minimized at the time of LCD module assembling.

Table 4

SEG output		SEG0 SEG199
ADC	"0"	0 (H)→ Column Address→ C7 (H)
(D0)	"1"	C7 (H)←Column Address ← 0 (H)

Line address circuit

When displaying contents of the display data RAM, the line address circuit is used for specifying the corresponding addresses. See Figure 4. Using the display start line address set command, the top line is normally selected (when the common output state is normal, COM0 is output. And, when reversed outputs COM7). For the display area of 9 lines is secured starting from the specified display start line address in the address incrementing direction.

Dynamically changing the line address using the display start line address set command enables screen scrolling and page change.

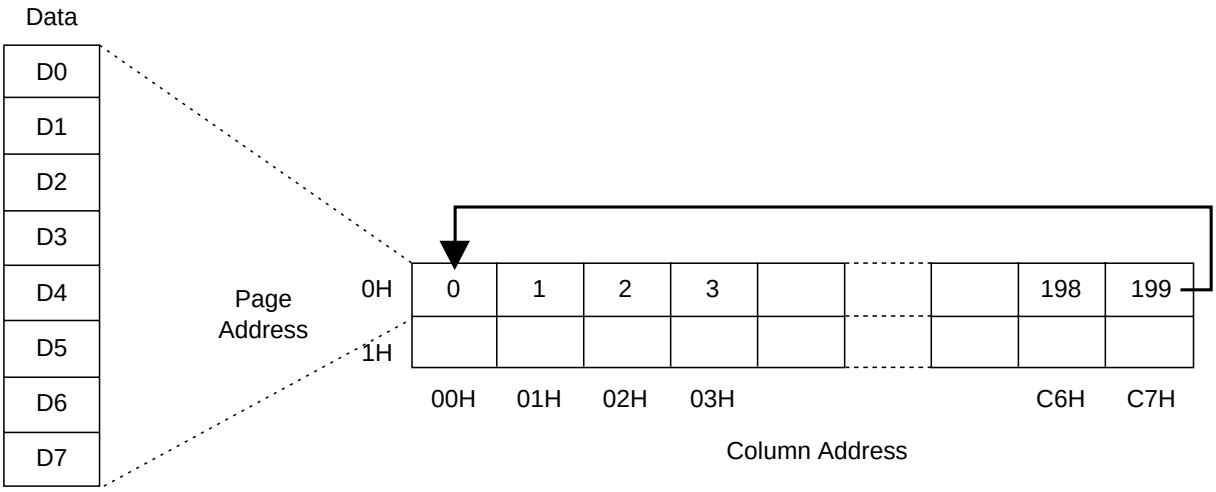


Fig. 5

Display data latch circuit

The display data latch circuit is a latch that temporarily stores the display data output from the display data RAM to the liquid crystal drive circuit.
Since the Display Normal Rotation/Reversal, Display ON/OFF, and Display All Lighting ON/OFF commands control the data in this latch, the data within the display data RAM is not changed.

Oscillator Circuit

This oscillator circuit is a CR type oscillator and generates display clocks. The oscillator circuit is valid only when M/S=HIGH and CL=HIGH.
When CL=LOW, the oscillation is stopped and the display clocks can entered from the CL pin.

Display Timing Generator Circuit

This display timing generator circuit generates timing signals from the display clocks to the line address circuit and the display latch circuit. It latches the display data to the display data latch circuit and outputs it to the segment drive output pin by synchronizing to the display clocks. The read operation of display data to the liquid crystal drive circuit is completely independent of the access to the display data RAM from the MPU. Therefore even when the display data RAM is asynchronously accessed during liquid crystal display, the access will not have any adverse effect on the display such as flickering.
The circuit also generates the internal common timing, liquid crystal alternating current signal (FR) from the display clocks.
As shown in Fig. 6, the FR normally generates the drive waveforms in the 2-frame alternating current drive system to the liquid crystal drive circuit.
When the S1D15711 Series is used for the multiple chip configuration, the slave side needs to supply the display timing signals (FR, CLO, and $\overline{DOF}$) from the master side.
Table 5 shows the state of FR, CLO, or $\overline{DOF}$.

Table 5

Operation mode		FR	CLO	$\overline{DOF}$
Master (M/S=HIGH)	Built-in oscillator circuit valid (CL=HIGH)	Output	Output	Output
	Built-in oscillator circuit invalid (Input an external clock from the CL pin.)	Output	Output	Output
Slave (M/S=LOW)	(Fix the CL pin to LOW.)	Input	Input	Input

2-frame alternating current drive waveforms

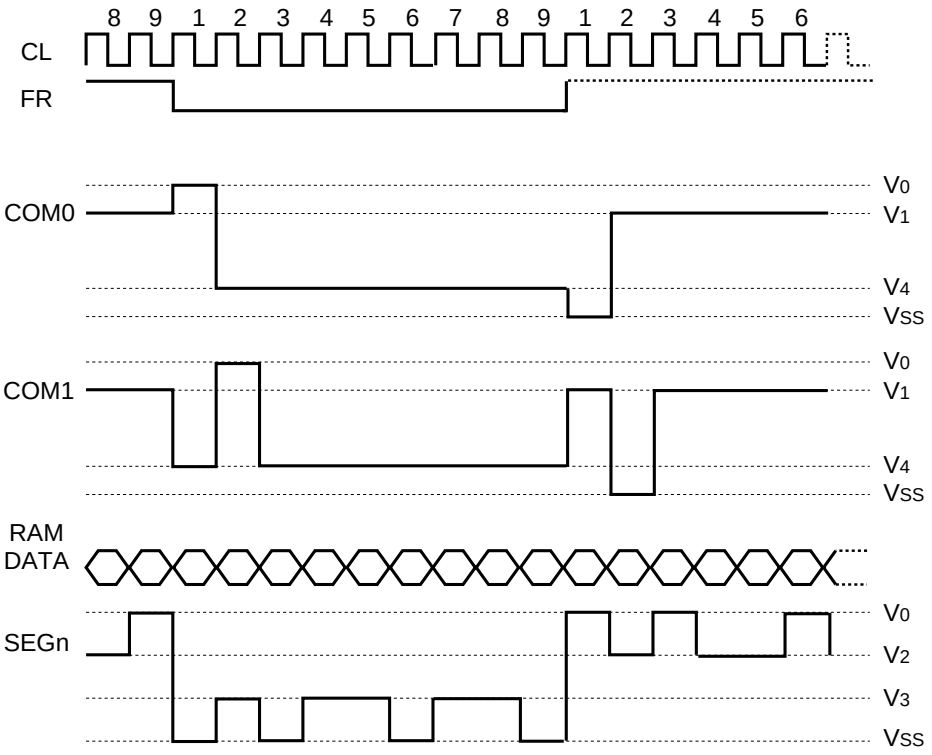


Fig. 6

Common Output State Selection Circuit

The S1D15711 Series can set the scanning direction of the COM output using the common output state selection command (see Fig. 6). Therefore the IC assignment restrictions at LCD module assembly are reduced.

Table 6

State	COM scanning direction
Normal rotation	COM 0 → COM 7
Reversal	COM 7 → COM 0

Liquid Crystal Drive Circuit

This liquid crystal drive circuit is 209 sets of mutiplexers that generate quadruple levels for liquid crystal drive. It outputs the liquid crystal drive voltage that corresponds to the combinations of the display data, COM scanning signal, and FR signal.
Fig. 6 shows examples of the SEG and COM output waveforms.

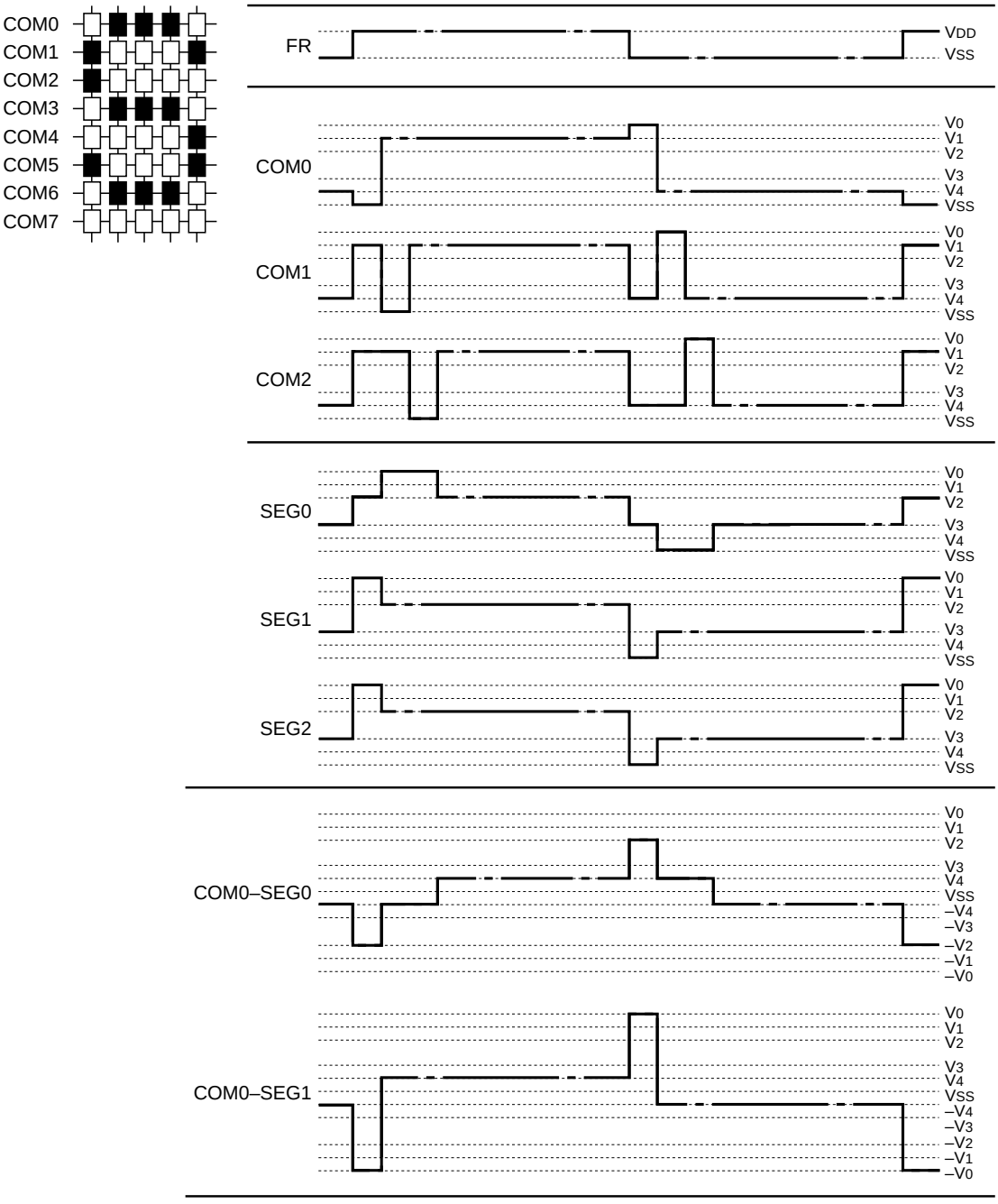


Fig. 7

Power Supply Circuit

This power supply circuit is a low power supply consumption one that generates the voltage required for the liquid crystal drive and consists of a boosting circuit, voltage adjusting circuit, and voltage follower circuit. It is valid only at master operation.
The power supply circuit ON/OFF controls the boosting circuit, voltage adjusting circuit, and voltage follower circuit using the power supply control set command, respectively.
Therefore, it can also use the partial functions of the external power supply and built-in power supply together. Table 7 lists the functions that control 3-bit data using the power control set command and Table 8 lists the reference combinations.

Table 7 Description of controlling bits using the power control set command

Item		State "1"	State "0"
D2	Boosting circuit control bit	ON	OFF
D1	Voltage adjusting circuit (V adjusting circuit) control bit	ON	OFF
D0	Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 8 Reference combinations

Status of use	D2	D1	D0	Boosting circuit	V adjusting circuit	V/F circuit	External voltage input	Boosting system pin
① Built-in power supply used	1	1	1	O	O	O	V_{DD2}	Used
② V adjusting circuit and V/F circuit only	0	1	1	X	O	O	V_{OUT}, V_{DD2}	OPEN
③ V/F circuit only	0	0	1	X	X	O	V_0, V_{DD2}	OPEN
④ External power supply only	0	0	0	X	X	X	V_1 to V_4	OPEN

- The boosting system pin indicates the CAP1+, CAP1–, CAP2+, CAP2–, or CAP3– pin.
- Although the combinations other than those listed in the above table are also possible, they cannot be recommended because they are not actual use methods.

Boosting circuit

The boosting circuit incorporated in the S1D15711 Series enables the quadruple boosting, triple boosting, and double boosting of the $V_{DD2} \leftrightarrow V_{SS}$ potential.
For the quadruple boosting, the $V_{DD2} \leftrightarrow V_{SS}$ potential is quadruple-boosted to the positive side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3+, and between V_{DD2} and V_{OUT}.
For the triple boosting, the $V_{DD2} \leftrightarrow V_{SS}$ potential is triple-boosted to the positive side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, and between V_{DD2} and V_{OUT} and strapping both CAP3– and V_{OUT} pins.
For the double boosting, the $V_{DD2} \leftrightarrow V_{SS}$ potential is doubly boosted to the positive side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+ and CAP1–, and between V_{DD2} and V_{OUT}, setting CAP2+ to OPEN, and V_{OUT} and strapping CAP2–, CAP3+, and V_{OUT} pins.
Fig. 8 shows the relationships of boosting potential.

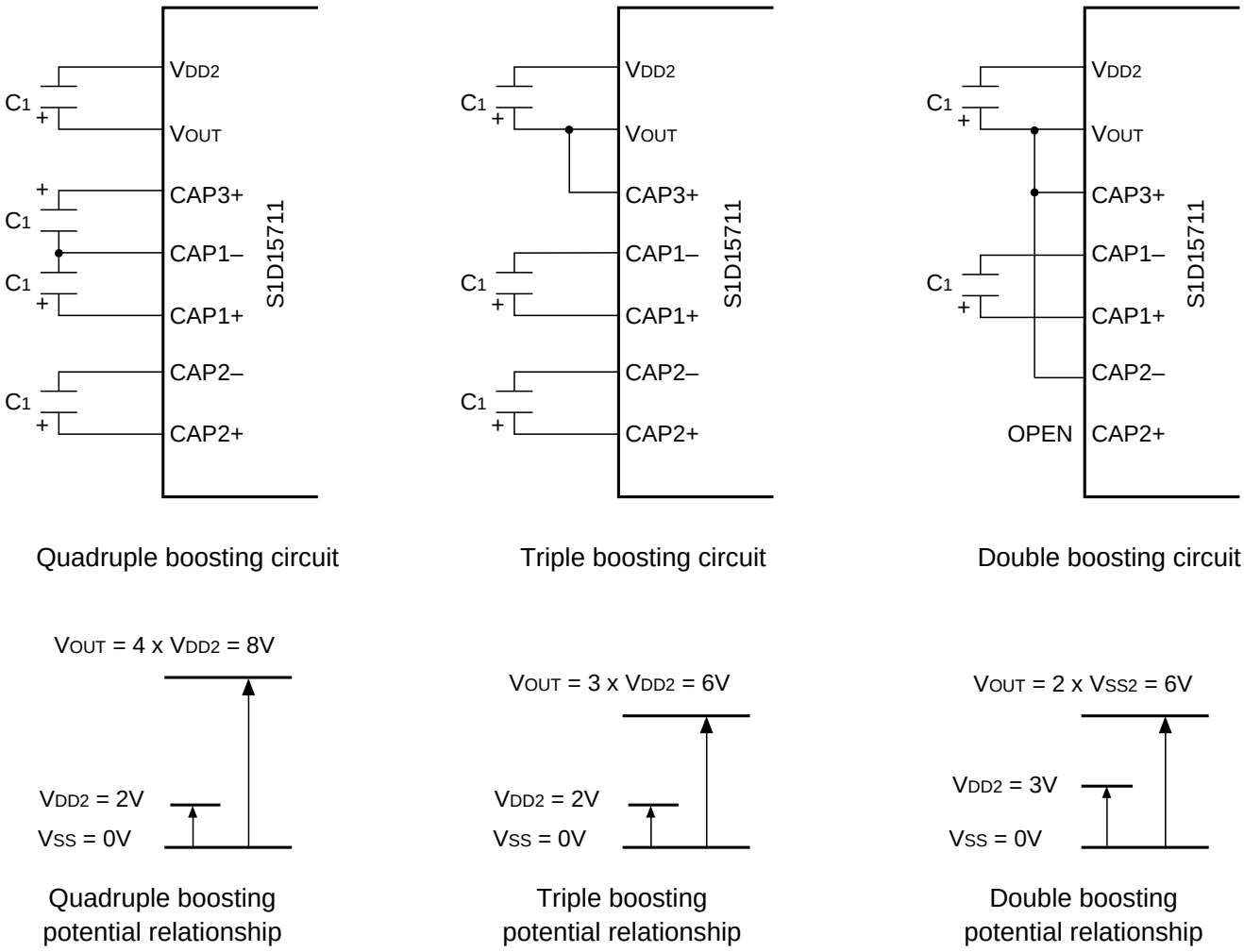


Fig. 8

- Set the V_{DD2} voltage range so that the voltage of the V_{OUT} pin cannot exceed the absolute maximum ratings.

Voltage adjusting circuit

The boosting voltage generated in V_{OUT} outputs the liquid crystal drive voltage V_0 through the voltage adjusting circuit.
Since the S1D15711 Series incorporates a high-accuracy constant power supply, 64-step electronic volume function, and V_0 voltage adjusting resistor, a high-accuracy voltage adjusting circuit can eliminate and save parts.

(A) When using the V_0 voltage adjusting internal resistor
The liquid crystal power supply voltage V_5 can be controlled and the depth of liquid crystal display can be adjusted only by the command with the use of V_0 voltage adjusting built-in resistor and the electronic volume function without any external resistor.
The V_0 voltage can be obtained according to Expression A-1 within the range of $|V_0|<|V_{OUT}|$.

$$V_0 = \left(1+\frac{Rb}{Ra}\right)\cdot V_{EV} = \left(1+\frac{Rb}{Ra}\right)\cdot\left(1-\frac{\alpha}{200}\right)\cdot V_{REG} \quad \left[\because V_{EV} = \left(1-\alpha/200\right)\cdot V_{REG}\right] \qquad \text{(Expression A-1)}$$

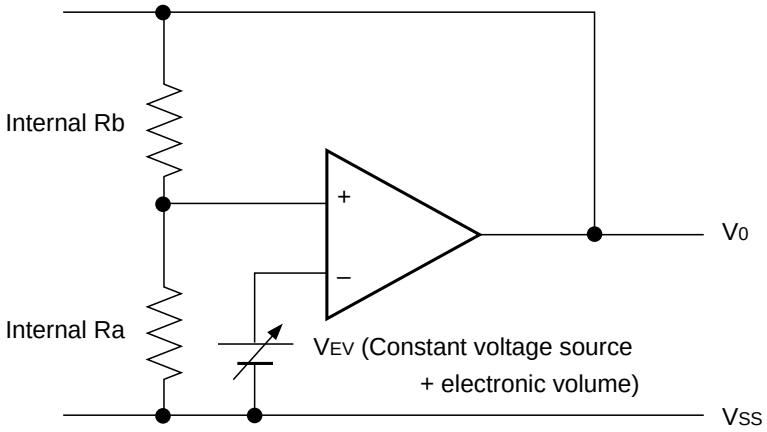


Fig. 9

V_{REG} is a constant voltage source within an IC, and the value at Ta=25°C is constant as listed in Table 9.

Table 9

Device	Temperature gradient	Unit	V_{REG}	Unit
Internal power supply	–0.1	[%/°C]	1.2	[V]

α indicates an electronic volume command value. Setting data in a 5-bit electronic volume register enters one state among 32 states. Table 10 lists the values of α based on the setup of the electronic volume register.

Table 10

D4	D3	D2	D1	D0	α
0	0	0	0	0	31
0	0	0	0	1	30
0	0	0	1	0	29
		⋮			⋮
1	1	1	0	1	2
1	1	1	1	0	1
1	1	1	1	1	0

Rb/Ra indicates the V_0 voltage adjusting internal resistance ratio and can be adjusted into seven steps using the V_0 voltage adjusting internal resistance ratio set command. The reference values of the (1+Rb/Ra) ratio are obtained as listed in Table 11 by setting 3-bit data in the V_0 voltage adjusting internal resistance ratio register.

Table 11 (Reference values)

Register			Ratio of 1+ Rb/Ra
D2	D1	D0	
0	0	0	5.2
0	0	1	5.4
0	1	0	5.7
0	1	1	6.0
1	0	0	6.3
1	0	1	6.6
1	1	0	7.0
1	1	1	External resistor mode

For the internal resistance ratio, a manufacturing dispersion of up to ±3% should be taken into account. When not within the tolerance, adjust the V_0 voltage by externally mounting Ra and Rb.

Figs. 10 show the V_0 voltage reference values per temperature gradient device based on the values of the V_0 voltage adjusting internal resistance ratio register and electronic volume register at Ta=25°C.

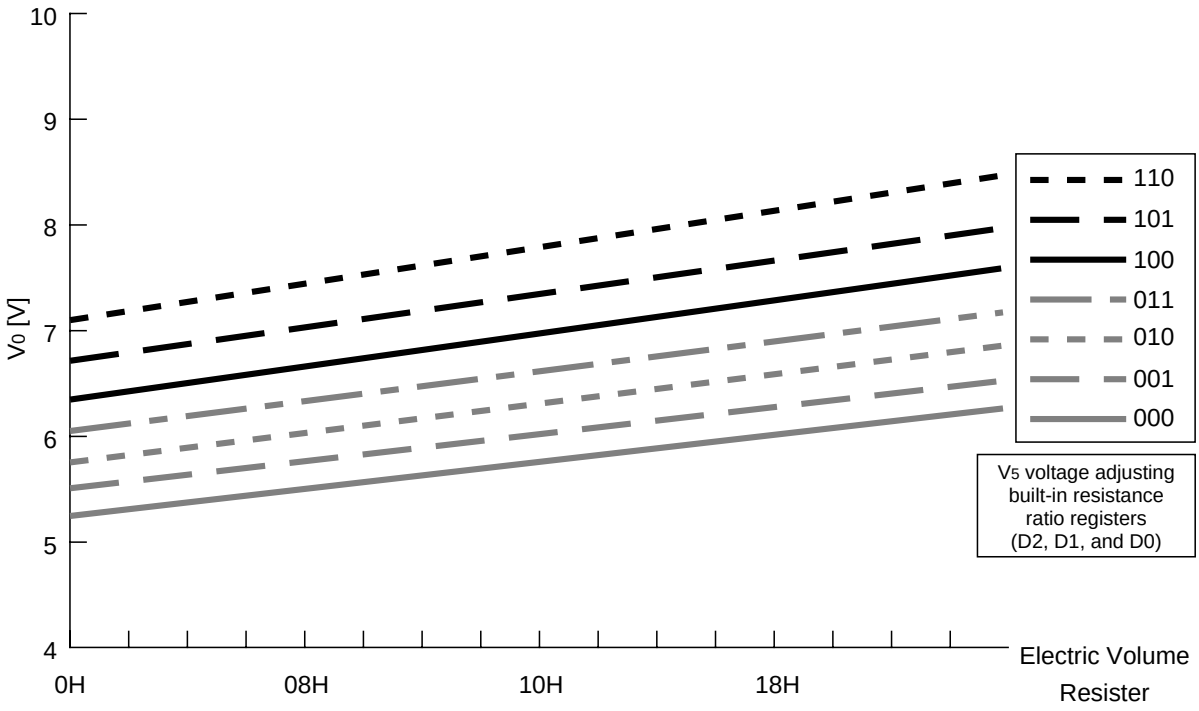


Fig. 10 S1D15711***

V_0 voltage based on the values of V_0 voltage adjusting internal resistance ratio register and electronic volume register

<Setting example: When setting V_0 = 6.0V at Ta=25°C>
From Fig. 8 and Expression A-1.

Table 12

	Register				
Description	**D4**	**D3**	**D2**	**D1**	**D0**
V_0 voltage adjusting	–	–	0	0	1
electronic control	1	0	0	0	0

In this case, Table 13 lists the V_0 voltage variable range and pitch width using the electronic volume function.

Table 13

V_0	**Min.**		**Typ.**		**Max.**	**Unit**
Variable range	5.5	to	6.0	to	6.5	[V]
Pitch width			about 31			[mV]

(B) When using the external resistor (not using the V0 voltage adjusting internal resistor) ①
The liquid crystal power supply voltage V0 can also be set by adding the resistors (Ra' and Rb') between VSS and VR and between VR and V0 without the V0 voltage adjusting built-in resistor (Internal resistance ratio set command for adjusting the V0 voltage [27H]). Also in this case, the liquid crystal power supply voltage V0 can be controlled using the command and the light and shade of liquid crystal display can be adjusted by using the electronic volume function.
The V0 voltage can be obtained from Expression B-1 by setting the external resistors Ra' and Rb' within the range of |V0| < |VOUT|.

$$V_0 = \left(1 + \frac{Rb'}{Ra'}\right) \cdot V_{EV}$$
$$= \left(1 + \frac{Rb'}{Ra'}\right) \cdot \left(1 - \frac{\alpha}{200}\right) \cdot V_{REG} \quad \text{(Expression B-1)}$$
$$\left[\because V_{EV} = \left(1 - \alpha/200\right) \cdot V_{REG}\right]$$

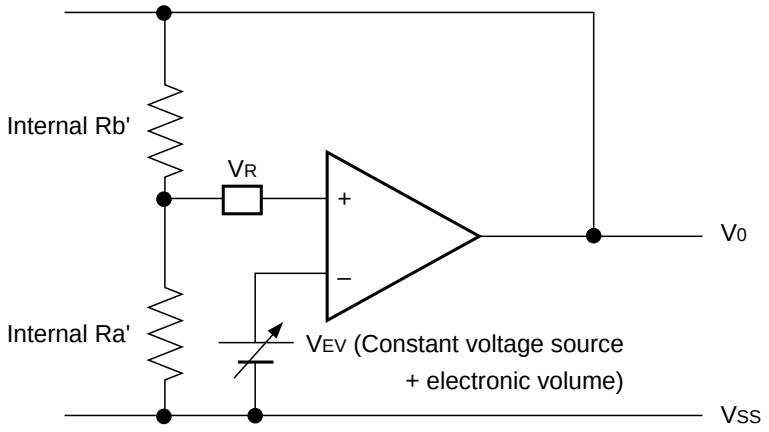


Fig. 11

<Setting example: When setting V0=6.0V at Ta=25°C>

Set the value of the electronic volume register as the intermediate value (D4, D3, D2, D1, D0) = (1,0,0,0,0). From the foregoing we can establish the expression:

$\alpha = 15$

$V_{REG} = 1.2V$

From Expression B-1, it follows that

$$V_0 = \left(1 + \frac{Rb'}{Ra'}\right) \cdot \left(1 - \frac{a}{200}\right) \cdot V_{REG} \quad \text{(Expression B-2)}$$
$$6.0V = \left(1 + \frac{Rb'}{Ra'}\right) \cdot \left(1 - \frac{15}{200}\right) \cdot 1.2$$

Also, suppose the current applied to Ra' and Rb' is 5µA.

$$Ra' + Rb' = 1.2M\Omega \quad \text{(Expression B-2)}$$

It follows that
Therefore from Expressions B-2 and B-3, we have

$$\frac{Rb'}{Ra'} = 4.4$$
$$Ra' = 272k\Omega$$
$$Rb' = 928k\Omega$$

In this case, Table 14 lists the V0 voltage variable range and pitch width using the electronic volume function.

Table 14

V5	Min.		Typ.		Max.	Unit
Variable range	5.5	to	6.0	to	6.5	[V]
Pitch width			about 31			[mV]

(C) When using the external resistor (not using the V0 voltage adjusting internal resistor) ②
In the use of the above-mentioned external resistor, the liquid crystal power supply voltage V0 can also be set by adding the resistors to finely adjust Ra' and Rb'. Also in this case, the liquid crystal power supply voltage V0 can be controlled using the command and the light and shade of liquid crystal display can be adjusted by using the electronic volume function.

The V0 voltage can be obtained from the following expression C-1 by setting the external resistors R1, R2 (variable resistors), and R3 within the range of |V0| < |VOUT| and finely adjusting R2 (ΔR2).

$$V_0 = \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot V_{EV}$$
$$= \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot \left(1 - \frac{\alpha}{200}\right) \cdot V_{REG}$$
$$\left[\because V_{EV} = \left(1 - \alpha/200\right) \cdot V_{REG}\right] \quad \text{(Expression C-1)}$$

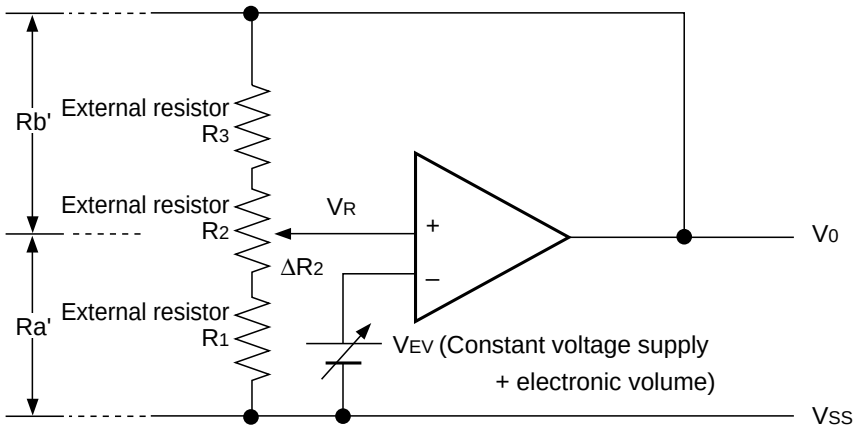


Fig. 12

<Setting example: When setting V_0= 5.0 to 8.0V at Ta=25°C>

Set the value of the electronic volume register as the intermediate value (D4, D3, D2, D1, D0) = (1,0,0,0,0). From the foregoing we can establish the expression:

$$\alpha = 15$$

$$V_{REG} = 1.2V$$

When ΔR_2=0Ω, to obtain V_0= (TBD) V from Expression C-1, it follows that

$$8.0V = \left(1 + \frac{R_3 + R_2}{R_1}\right) \cdot \left(1 - \frac{15}{200}\right) \cdot 1.2$$

(Expression C-2)

When ΔR_2=R_2, to obtain V_0= (TBD) V, it follows that

$$5.0V = \left(1 + \frac{R_3}{R_1 + R_2}\right) \cdot \left(1 - \frac{15}{200}\right) \cdot 1.2$$

(Expression C-3)

Also, suppose the current applied between V_{SS} and V_0 is 5µA.

$$R_1 + R_2 + R_3 = 1.3M\Omega$$

(Expression C-4)

It follows that

Therefore from Expressions C-2, C-3, and C-4, we have

$$R_1 = 180k\Omega$$

$$R_2 = 109k\Omega$$

$$R_3 = 1011k\Omega$$

At this time, the V_0 voltage variable range and notch width based on electronic volume function are given in the following Table when V_0= 6.5V by R_2 is assumed:

Table 15

V_0	Min.		Typ.		Max.	Unit
Variable range	5.9	to	6.5	to	7.0	[V]
Pitch width			about 35			[mV]

- When using the V_0 voltage adjusting internal resistor or electronic volume function, the state where at least the V_0 voltage adjusting circuit and voltage follower circuit are operated together needs to be set using the power control set command. Also when the boosting circuit is OFF, the voltage needs to be applied from V_{OUT}.
- The V_R pin is valid only when the V_0 voltage adjusting internal resistor. Set the V_R pin to OPEN when using the V_0 voltage adjusting internal resistor.
- Since the V_R pin has high input impedance, noise must be taken into consideration such as for short and shielded lines.

Liquid crystal voltage generator circuit

The V_0 voltage is resistor-split within an IC and generates the V_1, V_2, V_3, and V_4 potentials required for the liquid crystal drive.

Further, the V_1, V_2, V_3, and V_4 potentials are impedance-converted by the voltage follower and supplied to the liquid crystal drive circuit.

Using the bias set command allows you to select a desired bias ratio from 1/5 or 1/6.

Command sequence when the built-in power supply is turned off

To turn off the built-in power supply, set it in the power save state and then turn off the power supply according to the command sequence shown in Fig. 13 (procedure).

Procedure	Description (Command, state)	Command address D7	D6	D5	D4	D3	D2	D1	D0
Step1	Power save	1	0	1	0	1	1	1	0
	⬇	1	0	1	0	0	1	0	1
Step2	Turning off the built -in power supply								

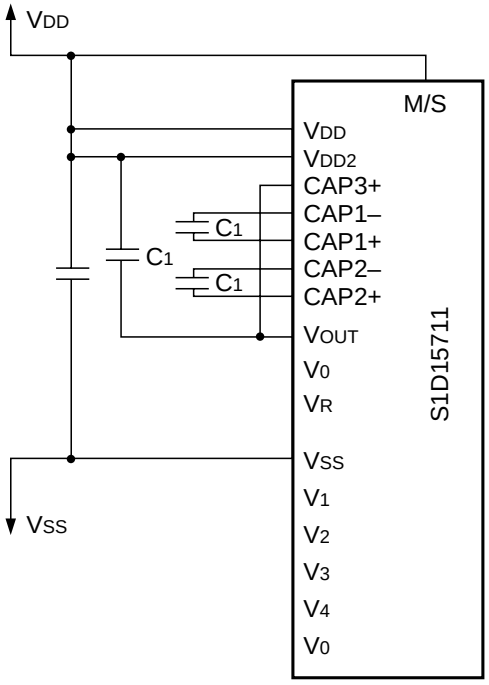
Power save command
(Composite command of display OFF and display full lighting ON)

Fig. 13

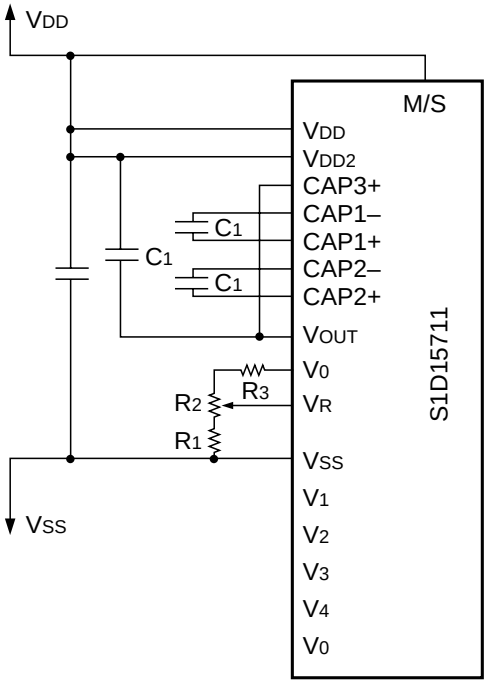
Reference circuit examples

① All the built-in power supply used

(1) When using the V_0 voltage adjusting built-in resistor (Example of V_{DD2}=V_{DD}, quadruple boosting)

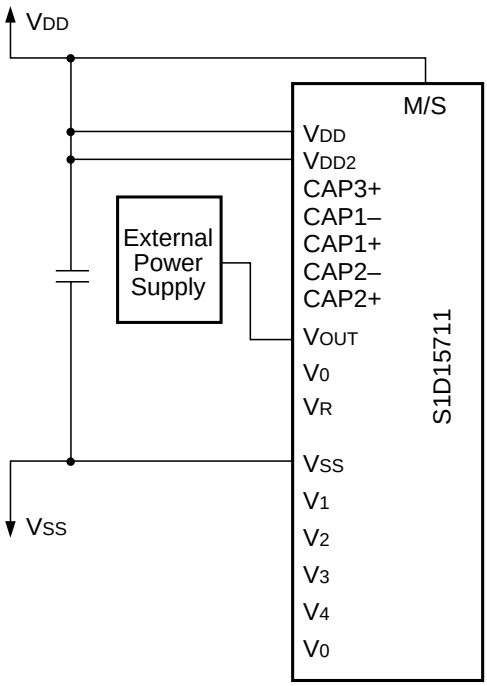


(2) When not using the V_0 voltage adjusting built-in resistor (Example of V_{DD2}=V_{DD}, quadruple boosting)

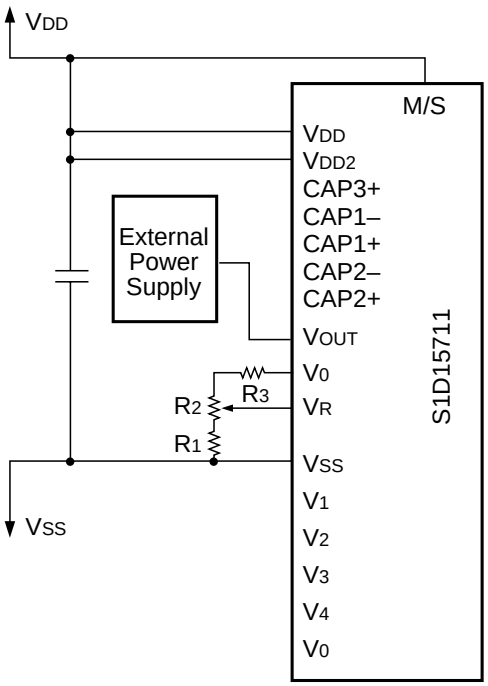


② Only the voltage adjusting circuit and V/F circuit used

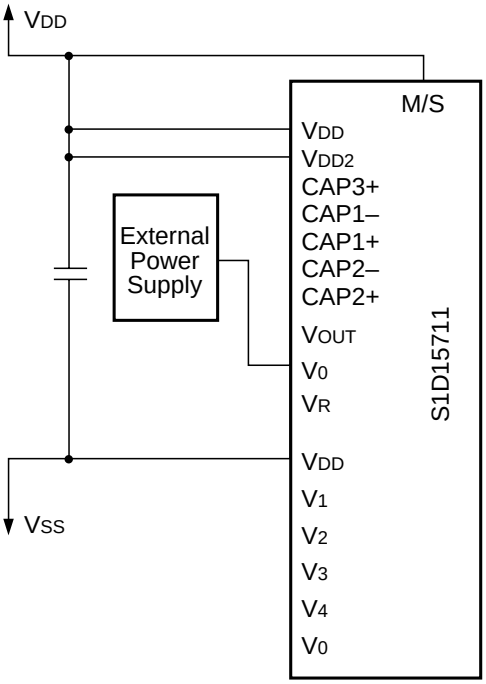
(1) When using the V_0 voltage adjusting built-in resistor



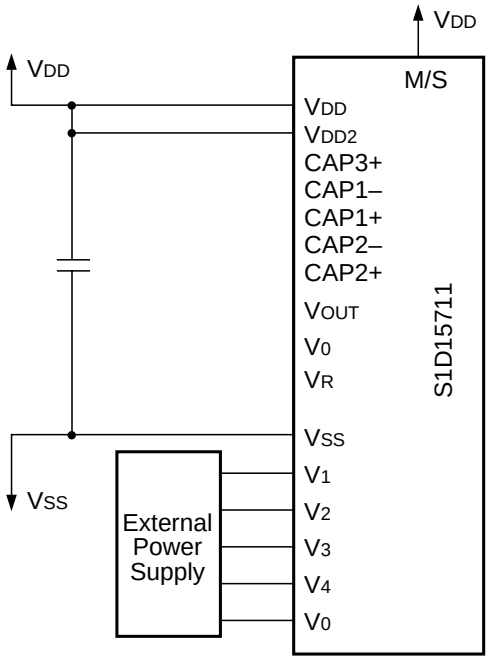
(2) When not using the V_0 voltage adjusting built-in resistor



③ Only the V/F circuit used



④ Only the external power supply used
Depending on all external power supplies



Common reference setting example
At V_0 ≒ 4.5 to 8.0V variable

Item	Setting value	Unit
C_1	1.0 to 4.7	µF

Fig. 14

*1 Since the V_R terminal input impedance is high, use short leads and shielded lines. When the V_R terminal is not used, means should be taken to prevent capacitance of the line or others from being applied.
*2 C_1 is determined according to the size of the LCD panel. Set a value so that the liquid crystal drive voltage can be stable.
[Setting example] • Turn on the V_0 adjusting circuit and the V/F circuit and apply external voltage.
• Then turn on all built-in power supplies and determine C_1.
*3 Capacity is connected in order to stabilize voltage between V_{DD} and V_{SS} power supplies.
*4 In case a large load panel is being driven by a built-in power supply and when the voltage level of V_0 to V_4 are not stable, it is possible to connect a capacitor between the V_0 to V_4 and the Vss for the purpose of stabilizing the voltage. Regarding the capacity, determine the capacity after confirming the indication quality targeting to a similar level of the capacity of C_1.
*5 Do not use the built-in power supply circuit if the display panel's load is large or if its possible that sufficient display quality will not be achieved by using only the built-in power supply circuit. Alternatively, use the external liquid crystal drive voltage.

Precautions when installing COG

When installing the COG, consider that there is a resistance on the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). This resistance may cause the indications on the LCD not to conform or it may cause IC malfunctions. Therefore, when installing the COG, design the module paying sufficient attention to the following three points and make sufficient evaluations under actual conditions.

1. As much as possible, suppress the resistance that is occurring between the driver chip pin and the externally connected parts.
   The boosting capacitors (the capacitors connecting to respective CAP pins and capacitor being inserted between V_{OUT} and V_{DD2}) of this IC are being switched over by the transistor with an ON-resistance of about 10Ω. However, when installing the COG, the resistance of the ITO wiring is being inserted in unison with the switching transistor, thus dominating the boosting ability. Take considerable care when wiring each boosting capacitor, and take measures such as using thicker ITO wiring.
   As much as possible, suppress the resistance in the driver chip's power supply pin.
   The power supply voltage may drop immediately due to an instantaneous current in areas like the switching part of the display clock. If the power supply pin's ITO wiring resistance is too high, then the voltage drop on the driver IC may increase significantly, causing malfunctions. Take considerable care when wiring the power supply line so that continuous power is supplied to the driver IC.
   The IC also employs the power supply pin V_{DD2} for the power supply circuit, which is separate from the logic system's power supply pin V_{DD}. If the noise from the power supply circuit affects the logic circuit, then supply separate power to the V_{DD} and the V_{DD2} or use external liquid crystal drive voltage instead of the built-in power supply.
2. Create the COG module sample with different sheet resistance.
   Evaluate sufficiently and, as much as possible, use ones with an operational margin sheet resistance.
3. Make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

Reset Circuit

When the $\overline{RES}$ input is set to the LOW level or the reset command is input, LSI enters initial setting states. The initial setting states are listed below.

1 Serial Interface Register Data Clear
2 Power Save Mode ON
(Built-in oscillator circuit OFF, built-in power supply circuit OFF, display full lighting ON)
3 Display Normal rotation
4 Page Address Set to page 0.
5 Column Address Set to address 0.
6 Display Start Line Set to first line.
7 Segment Driver Direction Normal rotation
8 Common Driver Direction Normal direction
9 Remote Modify Line OFF
10 Power Control Register: (D2, D1, D0) = (0, 0, 0)
11 V_0 Voltage Adjusting Built-in Resistance Ratio Register: (D2, D1, D0) = (0, 0, 0)
12 Electronic Control Register: (D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0)
13 LCD Power Supply Bias Ratio Set to 1/5 bias.
14 Test Mode Reset

When the power is turned on, the initialization using the $\overline{RES}$ pin is required. After the initialization using the $\overline{RES}$ pin, each input pin needs to be controlled normally. Besides, when the MPU control signal has high impedance, overcurrent may be applied to an IC. After turning on the power, take action so that the input pin cannot have high impedance.
The S1D15711 Series discharge electric charges of V_0 to V_{SS} and V_{OUT} to V_{DD2} at $\overline{RES}$ pin is set to the LOW level. If external power supplies for driving LCD are used, do not input external power while the $\overline{RES}$ pin is set to the LOW level to prevent short-circuiting between the external power supplies, V_{SS} and V_{DD2}.

7. COMMAND DESCRIPTION

The S1D15711 Series identifies data bus signals according to the combinations of A0, $\overline{RD}$(E), and $\overline{WR}$(R/$\overline{W}$). Since the interpretation and execution of commands are performed only by the internal timing independently of external clocks. The 80 series MPU interface starts commands by inputting low pulses to the $\overline{RD}$ pin at read and to the $\overline{WR}$ pin at write operation. The 68 series MPU interface enters the read state when HIGH is input to the R/$\overline{W}$ pin. It enters the write state when LOW is input to the same pin. It starts commands by inputting high pulses to the E pin (for the timing, see the Timing Characteristics of Chapter 10). Therefore the 68 series MPU interface differs from the 80 series MPU interface in that $\overline{RD}$(E) is set to "1 (H)" at display data read in the Command Description and Command Table. The command description is given below by taking the 80 series MPU interface as an example.
When selecting the serial interface, enter sequential data from D7.

Command description

(1) Display ON/OFF

This command specifies display ON/OFF.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

For display OFF, the segment and common drivers output the VSS level.
Further, for display OFF, when the display full lighting ON command is executed (otherwise, for display full lighting ON, when the display OFF command is executed, processing enters the power save mode.

(2) Display Start Line Set

This command specifies the display start line address of the display data RAM shown in Fig. 4. The display area is displayed for 9 lines from the specified line address to the line address increment direction. When this command is used to dynamically change the line address, the vertical smooth scroll and page change are enabled. For details, see the Line address circuit of "Function Description".

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
							↓				↓
							0	1	0	0	6
							0	1	1	1	7

(3) Page Address Set

This command specifies the page address that corresponds to the low address when accessing the display data RAM shown in Fig. 4 from the MPU side. The display data RAM can access desired bits when the page address and column address are specified. Even when the page address is changed, the display state will not be changed. For details, see the Page address circuit of "Function Description".

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
										1	1

(4) Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (higher 4-bits and lower 4-bits) when it is set (set continuously in principle). Each time the display data RAM is accessed, the column address automatically increments (+), making it possible for the MPU to continuously read and write the display data. The page address is not changed continuously. For details, see "Column Address Circuit" in Function Description.

	A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
High-order bit →	0	1	0	0	0	0	1	A7	A6	A5	A4
Low-order bit →							0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
				↓				↓
1	1	0	0	0	1	1	0	198
1	1	0	0	0	1	1	1	199

(5) Display Data Write

This command writes 8-bit data to the specified address of the display data RAM. Since the column address is automatically incremented by 1 after the data is written, the MPU can successively write the display data.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

(6) Display Data Read

This command reads the 8-bit data in the specified address of the display data RAM. Since the column address is automatically incremented by 1 after the data is written, the MPU can successively read the data consisting of multiple words.
Besides, immediately after the column address is set, dummy read is required one time. For details, see the description of the Display data RAM and internal register access of "Function Description".
When using the serial interface, the display cannot be read.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

(7) ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence relationship between the column address of the display RAM data shown in Fig. 4 and the segment driver output. Therefore the order of the segment driver output pin can be reversed using the command. After the display data is written and read, the column address is incremented by 1 according to the column address of Fig. 4. For details, see the Column address circuit of "Function Description".

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Clockwise (normal rotation)
										1	Counterclockwise (reversal)

(8) Display Normal Rotation/Reversal

This command can reversal display lighting and non-lighting without overwriting the contents of display data RAM. In this case, the contents of display data RAM are held.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	LCD on potential (normal rotation) RAM data HIGH
										1	LCD on potential (reversal) RAM data LOW

(9) Display All Points ON/OFF

This command can forcedly make all display set in the lighting state irrespective of the contents of display data RAM. In this case, the contents of display data RAM are held.
This command has priority over the display normal rotation/reversal command.
Also, when the display is OFF, execute the Display All Points ON Command (or when the display is ON, execute the Display OFF Command), and the power save mode will be selected.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display state
										1	Display all lighting

(10) LCD Bias Set

This command selects the bias ratio of the voltage required for liquid crystal drive. The command is valid when the V/F circuit of the power supply circuit is operated.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Selected state
0	1	0	1	0	1	0	0	0	1	1	1/5 bias
										0	1/6 bias

(11) Read Modify Write

This command is used together with the end command. Once this command is entered, the column address can be incremented by 1 only using the display data write command instead of being changed using the display read command. This state is held until the end command is entered. When the end command is entered, the column address returns to the address when the read modify write command is entered. This function can reduce the load of the MPU when repeatedly changing data for a specific display area such as a blinking cursor.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* The commands other than Display Data Read/Write can be used even in Read Modify Write mode. However, the column address set command cannot be used.

- Sequence for cursor display

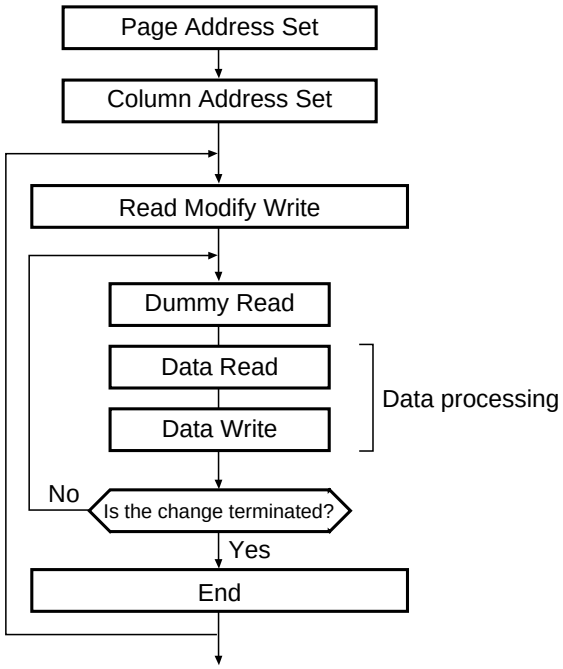


Fig. 15

(12) End

This command resets the Read Modify Write mode and returns the column address to the mode initial address.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

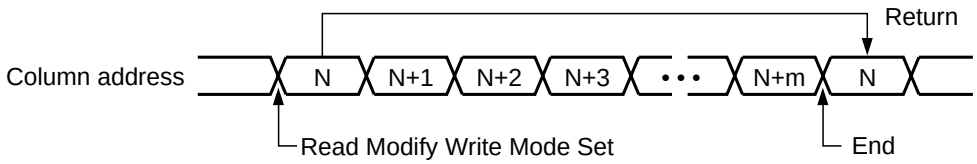


Fig. 16

(13) Reset

When this command is entered, this LSI is initialized. The execution of the reset command will not have any effect on the display data RAM. Further, the reset command cannot be used to perform strapping (discharging of an electric charge) between $V_{OUT} – V_{DD2}$ and between $V_0 – V_{SS}$. For details, see the Reset of “Function Description”.
Reset operation is performed after the reset command is entered.
For the detail, see "Reset" of Function Description. The reset operation is performed in the reset command input line.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power is applied is performed using the reset signal to the $\overline{RES}$ pin. The reset command cannot be substituted for the signal.

(14) Common Output State Selection

This command can select the scanning direction of the COM output pin. For details, see the Common Output State Selection Circuit of "Function Description".

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Selected state	
0	1	0	1	1	0	0	0	*	*	*	Normal rotation	COM0 → COM7
							1				Reversal	COM7 → COM0

*: Invalid bit

(15) Power Control Set

This command sets the function of the power supply circuit. For details, see the Power Supply Circuit of "Function Description".

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Selected state
0	1	0	0	0	1	0	1	0			Boosting circuit: OFF
								1			Boosting circuit: ON
									0		V adjusting circuit: OFF
									1		V adjusting circuit: ON
										0	V/F circuit: OFF
										1	V/F circuit: ON

(V/F circuit: Voltage follower circuit, V adjusting circuit: voltage adjusting circuit)

(16) V_0 Voltage Adjusting Internal Resistance Ratio Set

This command sets the V_0 voltage adjusting internal resistance ratio. For details, see the Power Supply Circuit of "Function Description".

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Rb to Ra ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	0	Large
								1	1	1	External Rb/Ra resistor mode

(17) Electronic Volume Set

This command controls the liquid crystal drive voltage V_0 output from the voltage adjusting circuit of the built-in liquid crystal power supply and can adjust the light and shade of liquid crystal display.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	| V5 |
0	1	0	1	0	0	0	0	0	0	0	Small
0	1	0				0	0	0	0	1	
0	1	0				0	0	0	1	0	↓
							↓				
0	1	0				1	1	1	1	0	
0	1	0				1	1	1	1	1	Large

*: Invalid bit

When not using the electronic volume function, set (1,0,0,0,0).

• Sequence of the electronic volume register set

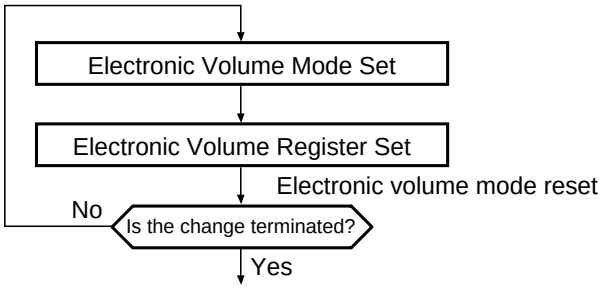


Fig. 17

(18) Power save

When display full lighting ON is set in the display OFF state, the power save state occurs and power consumption can greatly be reduced.
In the power save state, the operating state before the display data and power save activation is held, and the display data RAM can also be accessed from the MPU.
The power save state is reset using the procedure shown in Fig. 18.

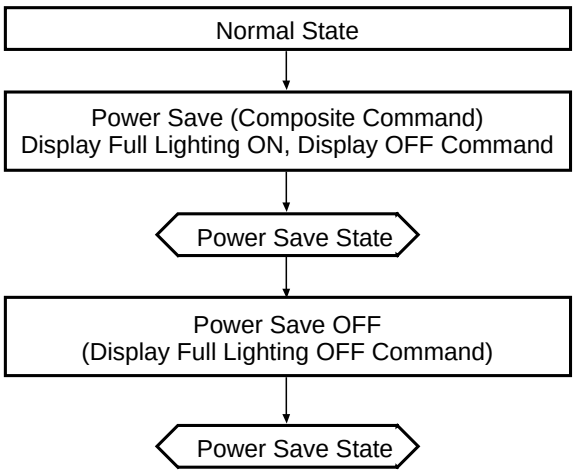


Fig. 18

In the power save mode, all the operations of LCD display systems are stopped, and the power consumption approximate to the static current when they are not accessed from the MPU can be reduced. The internal state in this state is as follows:
(1) The oscillator circuit and the LCD power supply circuit are stopped.
(2) All liquid crystal drive circuits are stopped and the segment and common drivers output the VSS level.

* When using an external power supply, it is recommended that the function of the external power supply circuit should be stopped at power save activation. For example, when assigning each level of the crystal liquid drive voltage via an external (standalone) resistance splitting circuit, it is recommended that a circuit which cuts off the current flowing into the resistance splitting circuit should be added at power save activation. The S1D15711 Series is provided with a liquid crystal display blanking control pin $\overline{DOF}$, and the pin is set to LOW at power save activation. The function of the external power supply circuit can be stopped using the $\overline{DOF}$ output.

(19) NOP

Non-OPeration

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

(20) Test

IC chip test command. Do not use this command. If the test command is used incorrectly, it can be reset by setting the RES input to LOW or by using the reset command or display ON/OFF.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	*	1	*	*	*	*

*: Invalid bit

(Note) Although the S1D15711 Series maintains the operation status as per the command, in case excessive external noise enters or when abrupt power voltage variation in excess of the specified value as per the “9. DC Characteristic Items” occurs, there is a possibility of changing the internal status or causing a malfunctioning. Such action that suppresses the generation of noise and prevents the effect of noise needs to be taken on installation and systems. Besides, to prevent sudden noise, it is recommended that the operating state should periodically be refreshed.

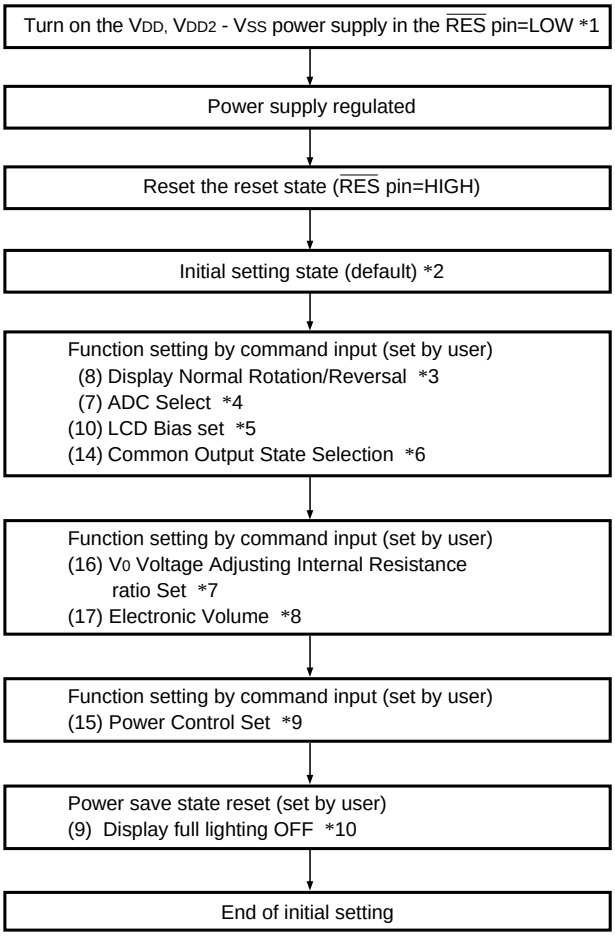
Table 16 S1D15711 Series Commands

Command	Command code											Function
	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display Start Line Set	0	1	0	0	1	Display start address						Sets the display start line address of the display RAM.
(3) Page Address Set	0	1	0	1	0	1	1	1	1	1	0 1	Display RAM: 0 : 0 page 1 : 1 page
(4) Column Address Set High-Order Bit	0	1	0	0	0	0	1	High order Column address				Sets the high-order four bits of the column address of the display RAM.
Column Address Set Low-Order Bit	0	1	0	0	0	0	0	Low order Column address				Sets the low-order four bits of the column address of the display RAM.
(5) Display Data Read	1	1	0	Write data								Writes data on the display RAM.
(6) Display Data Write	1	0	1	Read data								Reads data from the display RAM.
(7) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Supports the SEG output of the display RAM address. 0: normal rotation, 1: Reversal
(8) Display Normal Rotation/Reversal	0	1	0	1	0	1	0	0	1	1	0 1	LCD display normal rotation/ reversal 0: normal rotation, 1: Reversal
(9) Display All Points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all lighting 0: normal display, 1: All ON
(10) LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio. 0: 1/6, 1: 1/5
(11) Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address. At write operation: By 1, at read: 0
(12) End	0	1	0	1	1	1	0	1	1	1	0	Resets Read Modify Write.
(13) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal resetting
(14) Common Output State Selection	0	1	0	1	1	0	0	0 1	*	*	*	Selects the scanning direction of the COM output. 0: Normal rotation, 1: Reversal
(15) Power Control Set	0	1	0	0	0	1	0	1	Operating state			Selects the state of the built-in power supply
(16) V_0 Voltage Adjusting Internal Resistance Ratio Set	0	1	0	0	0	1	0	0	Resistance ratio setting			Selects the state of the internal resistance ratio (Rb/Ra).
(17) Electronic Volume Set	0	1	0	1	0	0	Electronic control value					Sets the V_0 output voltage in the electronic register.
(18) Power Save	–	–	–	–	–	–	–	–	–	–	–	Moves to the power save state. Display OFF and display all points ON compound command
(19) NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation command
(20) Test	0	1	0	1	1	*	1	*	*	*	*	Do not use the IC chip test command.

*: Invalid bit

Instruction Setup: Reference

(1) Initial Setting



Notes: Reference items

*1: If external power supplies for driving LCD are used, do not supply voltage on VOUT or V0 pin during the period when RES = LOW. Instead, input voltage after releasing the reset state.
6. Function Description "Reset Circuit"

*2: The contents of DDRAM are not defined even in the initial setting state after resetting.
6. Function Description Section "Reset Circuit"

*3: 7. Command Description Item (8) Display Normal Rotation/Reversal

*4: 7. Command Description Item (7) ADC Select

*5: 7. Command Description Item (10) LCD Bias Set

*6: 7. Command Description Item (14) Common output state selection

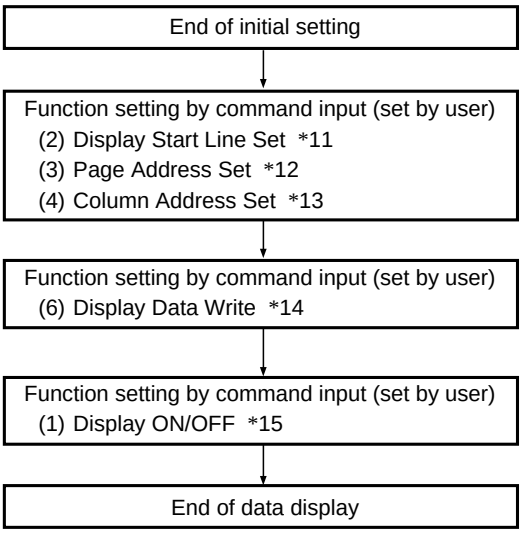
*7: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (16) V0 Voltage Adjusting Internal Resistance ratio Set

*8: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (17) Electronic Volume

*9: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (15) Power Control Set

*10 7. Command Description Item (9) Display All points ON/OFF and (18) Power Save

(2) Data Display



Notes: Reference items

*11: 7. Command Description Item (2) Display Start Line Set

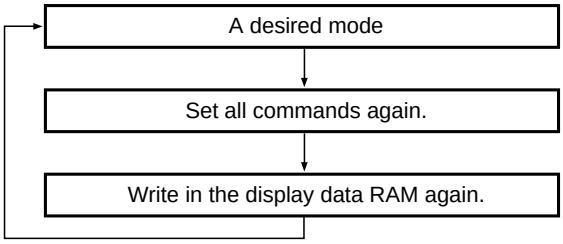
*12: 7. Command Description Item (3) Page Address Set

*13: 7. Command Description Item (4) Column Address Set

*14: The contents of DDRAM is not defined after completing initial setting. Enter data in each DDRAM to be used for display.
7. Command Description Item (5) Display Data Write

*15: Avoid activating the display function with entering space characters as the data if possible.
7. Command Description Item (1) Display ON/OFF

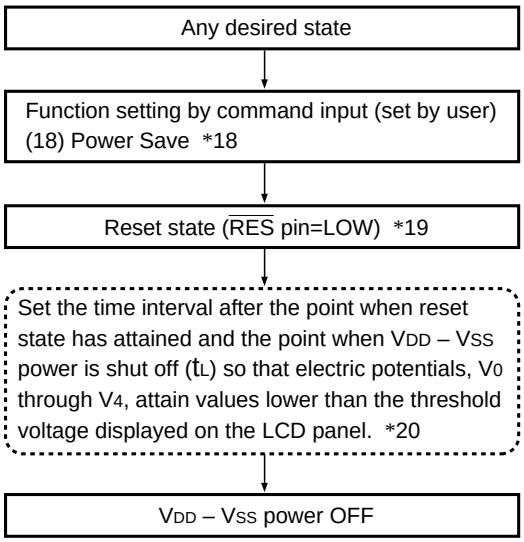
(3) Refresh *16



Notes: Reference items

*16: It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.

(4) Power *17



Notes: Reference items

*17: This IC is a V_{DD} – V_{SS} power system circuit controlling the LCD driving circuit for the V_0 – V_{SS} power system. Shutting of power with voltage remaining in the V_0 – V_{SS} power system may cause uncontrolling voltage to be output from the SEG and COM pins. Follow the Power OFF sequence.

*18: 7. Command Description Item (18) Power Saving

*19: When external power supplies for driving LCD are used, turn all external power supplies off before entering reset state.
6. Function Description Item Reset Circuit

*20: The threshold voltage of the LCD panel is about 1 [V].
Set up t_L so that the relationship, $t_L > t_H$, is maintained. A state of $t_L < t_H$ may cause faulty display.

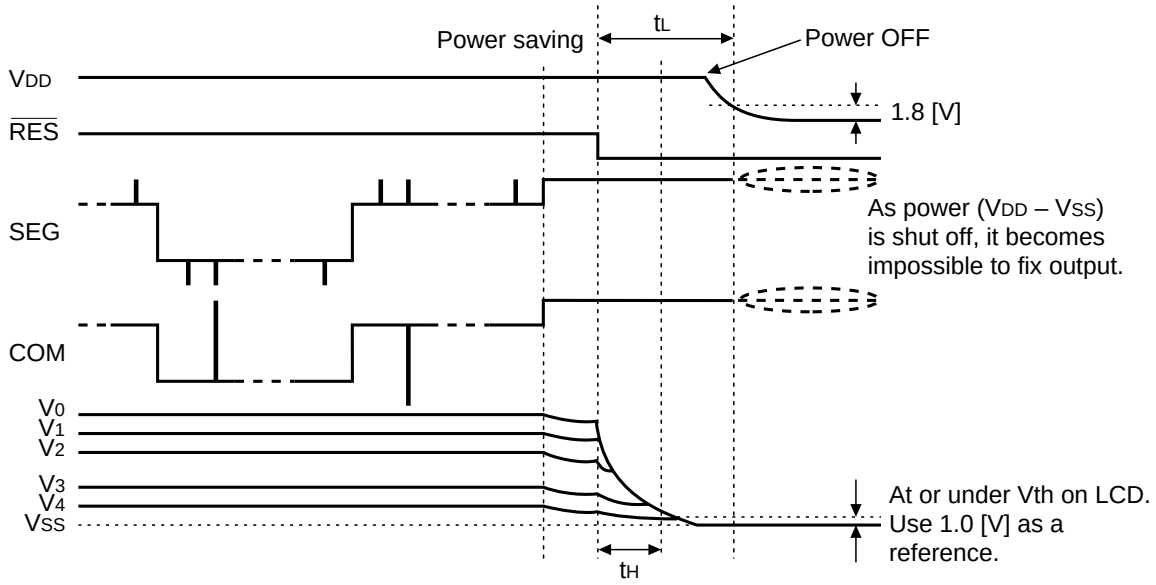
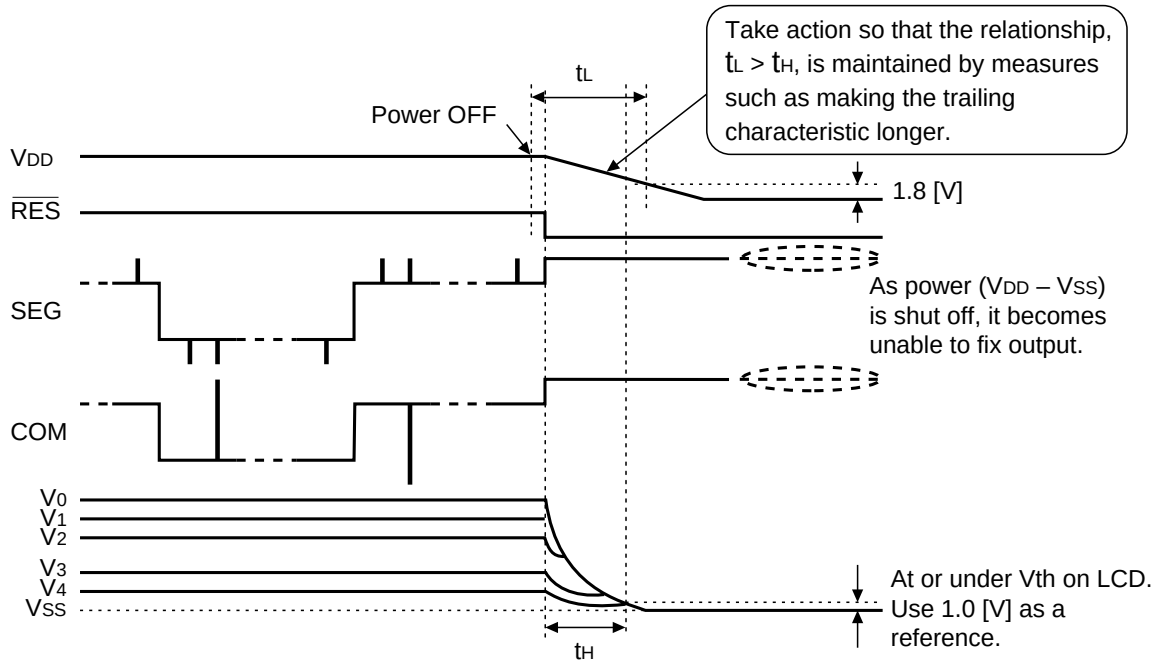


Fig. 19



If command control is disabled when power is OFF, take action so that the relationship, $t_L > t_H$, is maintained by measures such as making the trailing characteristic of power ($V_{DD} – V_{SS}$) longer.

Fig. 20

8. ABSOLUTE MAXIMUM RATINGS

Table 17

V_{SS}=0 V unless specified otherwise

Item		Symbol	Specification value			Unit
Power supply voltage		V_{DD}	–0.3	to	6.0	V
Power supply voltage (2) (Based on V_{DD})		V_{DD2}	–0.3	to	5.0	
	At triple boosting		–0.3	to	3.3	
	At quadruple boosting		–0.3	to	2.5	
Power supply voltage (3) (Based on V_{DD})		V_0, V_{OUT}	–0.3	to	10.0	
Power supply voltage (4) (Based on V_{DD})		V_1, V_2, V_3, V_4	–0.3	to	V_0	
Input voltage		V_{IN}	–0.3	to	V_{DD}+0.3	
Output voltage		V_O	–0.3	to	V_{DD}+0.3	
Operating temperature		T_{OPR}	–40	to	85	°C
Storage temperature	TCP	T_{STR}	–55	to	100	
	Bare chip		–55	to	125	

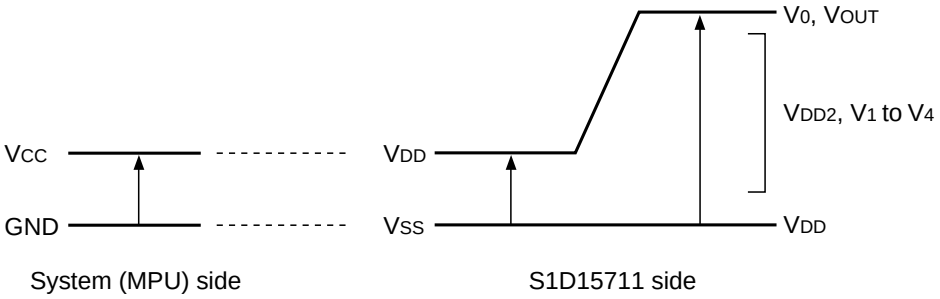


Fig. 21

(Notes) 1. The values of the V_{DD2}, V_0 to V_4, and V_{OUT} voltages are based on V_{SS}=0 V.
2. The V_1, V_2, V_3, and V_4 voltages must always satisfy the condition of $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$.
3. Insure that voltage levels V_{DD2} and V_{OUT} are always such that the relationship of $V_{OUT} \geq V_{DD2} \geq V_{DD} \geq V_{SS}$ is maintained.
4. When LSI is used exceeding the absolute maximum ratings, the LSI may be damaged permanently. Besides, it is desirable that the LSI should be used in the electrical characteristics condition for normal operation. If this condition is exceeded, the LSI may malfunction and have an adverse effect on the reliability of the LSI.

9. DC CHARACTERISTICS

Table 18

V_{SS}=0 V, V_{DD}=3.0 V ± 10%, and Ta=–40 to +85°C

Item		Symbol	Condition	Specification value			Unit	Applicable pin
				Min.	Typ.	Max.		
Operating voltage (1)		V_{DD}	(Based on V_{SS})	1.8	—	5.5	V	V_{DD} *1
Operating voltage (2)		V_{SS2}	(Based on V_{SS})	1.8	—	5.0		V_{SS2}
Operating voltage (3)		V_0 V_1, V_2 V_3, V_4	(Based on V_{SS}) (Based on V_{SS}) (Based on V_{SS})	4.5 0.6×V_0 V_0	— — —	9.0 V_0 0.4×V_0		V_0 *2 V_1, V_2 V_3, V_4
High level input voltage Low level input voltage		V_{IHC} V_{ILC}		0.8×V_{DD} V_{SS}	— —	V_{DD} 0.2×V_{DD}		*3 *3
High level output voltage Low level output voltage		V_{OHC} V_{OLC}	I_{OH}=–0.5mA I_{OL}=0.5mA	0.8×V_{DD} V_{SS}	— —	V_{DD} 0.2×V_{DD}		*4 *4
Input leak current Output leak current		I_{LI} I_{LO}	V_{IN}=V_{DD} or V_{SS}	–1.0 –3.0	— —	+1.0 +3.0	µA	*5 *6
Liquid crystal driver On resistance		R_{ON}	Ta=25°C, V_0 =5V V_0 =7V	—	4.2 3.0	8.0 5.0	kΩ	SEGn COMn *7
Static current consumption Output leak current		I_{SSQ} I_{0Q}	Ta=25°C V_0=9V (Based on V_{DD})	— —	0.01 0.01	5.0 15.0	µA	V_{SS}, V_{SS2} V_0
Input pin capacity		C_{IN}	Ta=25°C, f=1MHz	—	25	40	pF	
Oscillating frequency	Built-in oscillation	f_{OSC}	Ta=25°C	42.47	46.08	50.69	kHz	*8
	External input	f_{CL}		4.8	5.8	6.8		CL *8

Table 19

Item		Symbol	Condition		Specification value			Unit	Applicable pin
					Min.	Typ.	Max.		
Built-in power supply circuit	Input voltage	V_{SS2} V_{SS2} V_{SS2}	At double boosting (Based on V_{SS}) At triple boosting (Based on V_{SS}) At quadruple boosting (Based on V_{SS})		1.8 1.8 1.8	— — —	5.0 3.3 2.5	V	V_{SS2} V_{DD2} V_{DD2}
	Boosting output voltage	V_{OUT}	(Based on V_{SS})		—	—	10.0		V_{OUT}
	Voltage adjusting circuit operating voltage	V_{OUT}	(Based on V_{SS})		5.0	—	10.0		V_{OUT}
	V/F circuit operating voltage	V_0	(Based on V_{SS})		4.5	—	9.0		V_0 *9
	Reference voltage	V_{REG0}	Ta=25°C,	–0.1%/°C	1.16	1.2	1.24		*10

[*: see page 45.]

Dynamic current consumption value (1) During display operation and built-in power supply OFF
Current values dissipated by the whole IC when the external power supply is used

Table 20 Display All White

Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15711D00B000	I_{DD} (1)	$V_{DD}=V_{DD2}=3.0V, V_0=7.2V$	—	15	30	µA	*11
		$V_{DD}=V_{DD2}=3.0V, V_0=9.0V$	—	15	30		

Table 21 Display Checker Pattern

Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15711D00B000	I_{DD} (1)	$V_{DD}=V_{DD2}=3.0V, V_0=7.2V$	—	17	34	µA	*11
		$V_{DD}=V_{DD2}=3.0V, V_0=9.0V$	—	18	36		

Dynamic current consumption value (2) During display operation and built-in power supply ON
Current values dissipated by the whole IC containing the built-in power supply circuit

Table 22 Display All White

Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15711D00B000	I_{DD} (2)	$V_{DD}=V_{DD2}=3.3V$ Triple boosting, $V_0=7.0V$	—	59	118	µA	*12

Table 23 Display Checker Pattern

Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15711D00B000	I_{DD} (2)	$V_{DD}=V_{DD2}=3.3V$ Triple boosting, $V_0=7.0V$	—	63	126	µA	*12

Current consumption at power save $V_{SS}=0$ V and $V_{DD}=3.0$ V ±10%

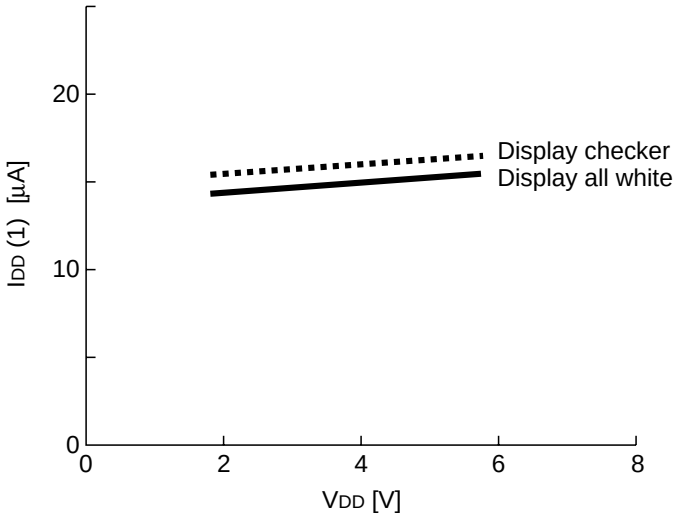
Table 24

Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15711D00B000	I_{DDS}		—	0.01	1.0	µA	

[*: see page 45.]

[Reference data 1]
• Dynamic current consumption (1) External power supply used and LCD being displayed

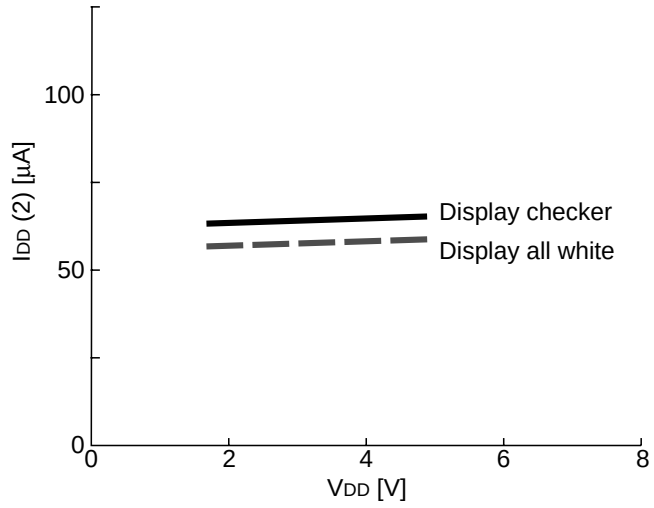


Condition: Built-in power supply OFF
External power supply used
V_0 = 7.2 V
Display pattern: All white/
checker
Ta = 25°C

Remarks: *11

Fig. 22

[Reference data 2]
• Dynamic current consumption (2) Built-in power supply used and LCD being displayed



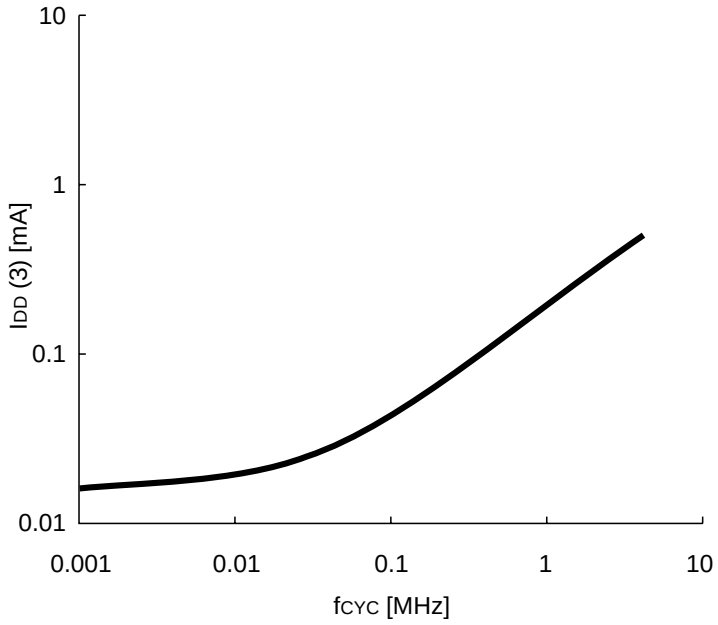
Condition: Built-in power supply ON
Quadruple boosting
V_{DD2} = 3.3 V
V_0 = 7.0 V
Display pattern: All white/
checker
Ta = 25°C

Remarks: *12

[*: see page 45.]

Fig. 23

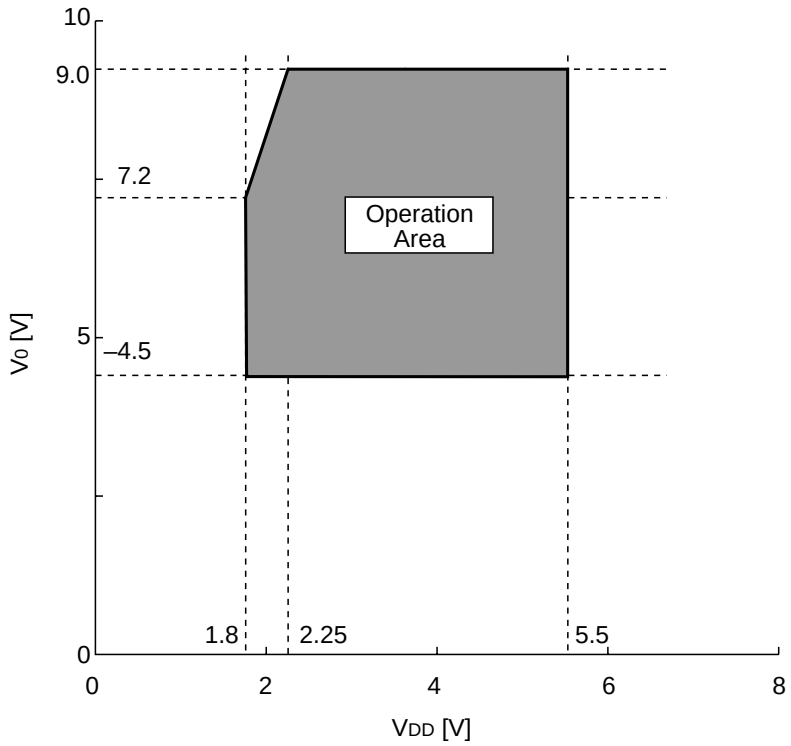
[Reference data 3]
• Dynamic current consumption (3) During access



Indicates the current consumption when the checker pattern is always written at f_{CYC}.
Only I_{DD} (1) when not accessed
Condition: Built-in power supply OFF and external power supply used
V_{DD} = 3.0 V,
V_0 = 6.0 V
Ta = 25°C

Fig. 24

[Reference data 4]



V_{DD} and V_0 system operating voltage ranges

Remarks: *2

[*: see page 45.]

Fig. 25

Relationships between the oscillating frequency f_{OSC}, display clock frequency f_{CL}, and liquid crystal frame frequency f_{FR}

Table 25

Item	f_{CL}	f_{FR}
When built-in oscillator circuit used	$\frac{f_{OSC}}{64}$	$\frac{f_{OSC}}{64 \times 9}$
When built-in oscillator circuit not used	External input (f_{CL})	$\frac{f_{CL}}{16 \times 9}$

(f_{FR} indicates the alternating current cycle of the liquid crystal and does not indicate that of the FR signal.)

[Reference items marked by *]

*1 The wide operating voltage range is not warranted. However, when there is a sudden voltage change it cannot be warranted.

*2 For the V_{DD} and V_0 operating voltage ranges, see Fig. 27. These ranges are applied when using the external power supply.

*3 A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CL, FR, M/S, C86, P/S, $\overline{DOF}$, and $\overline{RES}$ pins

*4 D0 to D7, FR, FRS, $\overline{DOF}$ and CL pins

*5 A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, M/S, C86, P/S and $\overline{RES}$ pins

*6 Applied when D0 to D5, D6 (SCL), D7 (SI), CL, FR, and $\overline{DOF}$ pins are in the high impedance state

*7 Resistance value when the 0.1 V voltage is applied between the output pin SEGn or COMn and power supply pins (V_1, V_2, V_3, and V_4). Specified within the range of operating voltage (3)
R_{ON} = 0.1 V/ΔI (ΔI indicates the current applied when 0.1 V is applied between the power ON.)

*8 For the relationship between the oscillating frequency and frame frequency. The specification value of the external input item is a recommended value.

*9 The V_0 voltage adjusting circuit is adjusted within the voltage follower operating voltage range.

*10 This is the internal voltage reference supply for the V_0 voltage regulator circuit. The thermal slope V_{REG} of the S1D15711 Series is about –0.1%/°C.

*11 and *12 Indicate the current dissipated by a single IC at built-in oscillator circuit used, 1/5 bias, and display ON.
Does not include the current due to the LCD panel capacity and wireing capacity.
Applicable only when there is no access from the MPU.

*12 When the V_0 voltage adjusting built-in resistor is used

10. TIMING CHARACTERISTICS

(1) System bus read/write characteristics 1 (80 series MPU)

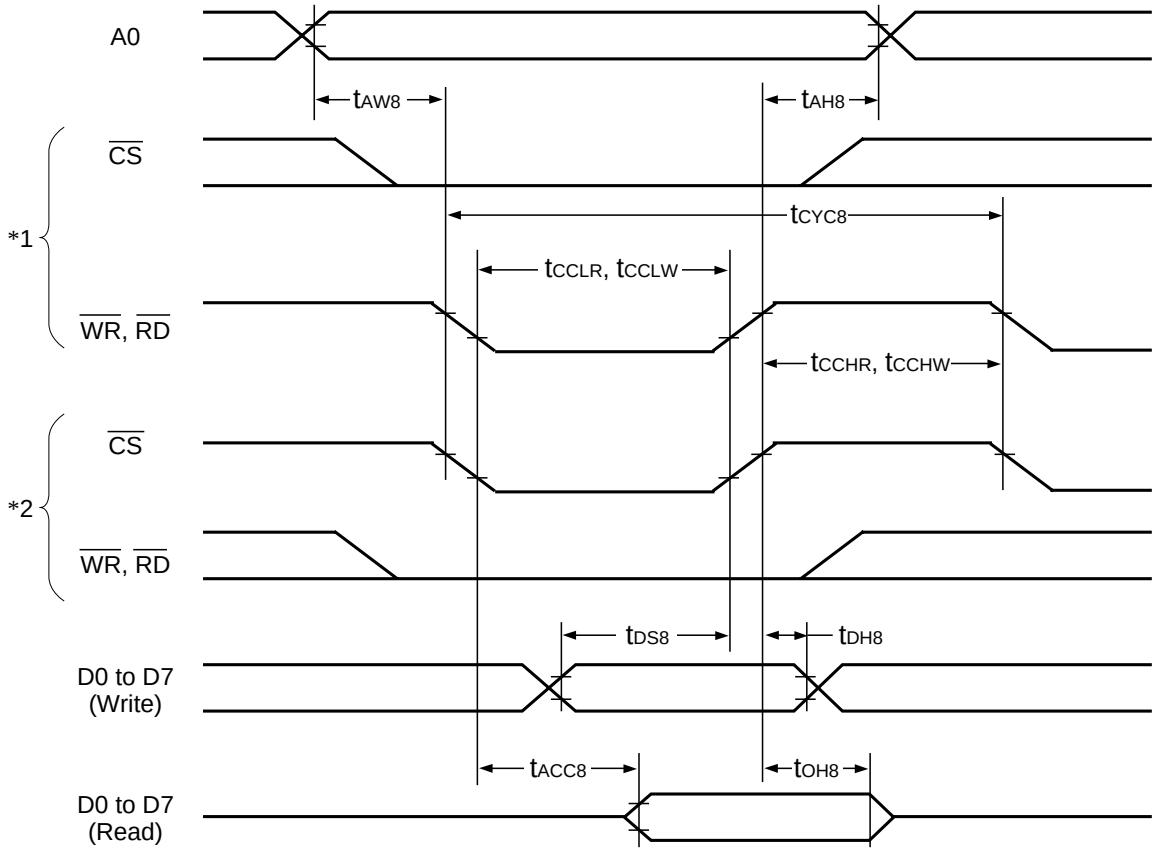


Fig. 26

Table 26

[V_{DD}=4.5V to 5.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		300	—	
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		50	—	
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		100	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		50	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		50	—	
Data setup time	D0 to D7	t_{DS8}		40	—	
Data hold time		t_{DH8}		0	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	90	
Output disable time		t_{OH8}		5	70	

Table 27

[V_{DD}=2.7V to 4.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		500	—	
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		100	—	
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		200	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		100	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		100	—	
Data setup time	D0 to D7	t_{DS8}		70	—	
Data hold time		t_{DH8}		0	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	180	
Output disable time		t_{OH8}		5	100	

Table 28

[V_{DD}=1.8V to 2.7V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time	A0	t_{CYC8}		1000	—	
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		150	—	
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		300	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		150	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		150	—	
Data setup time	D0 to D7	t_{DS8}		120	—	
Data hold time		t_{DH8}		0	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	260	
Output disable time		t_{OH8}		10	200	

*1. This is the case of accessing by $\overline{WR}$ and $\overline{RD}$ when $\overline{CS}$ = LOW.
*2. This is the case of accessing by $\overline{CS}$ when $\overline{WR}$ and $\overline{RD}$ = LOW.
*3 The rise and fall times (t_r and t_f) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for (t_r+t_f) ≤ (t_{CYC8}–t_{CCLW}–t_{CCHW}) or (t_r+t_f) ≤ (t_{CYC8}–t_{CCLR}–t_{CCHR}).
*4 All timings are specified based on the 20 and 80% of V_{DD}.
*5 t_{CCLW} and t_{CCLR} are specified for the overlap period when $\overline{CS}$ is at LOW level and $\overline{WR}$, $\overline{RD}$ are at the LOW level.

(2) System bus read/write characteristics 2 (68 series MPU)

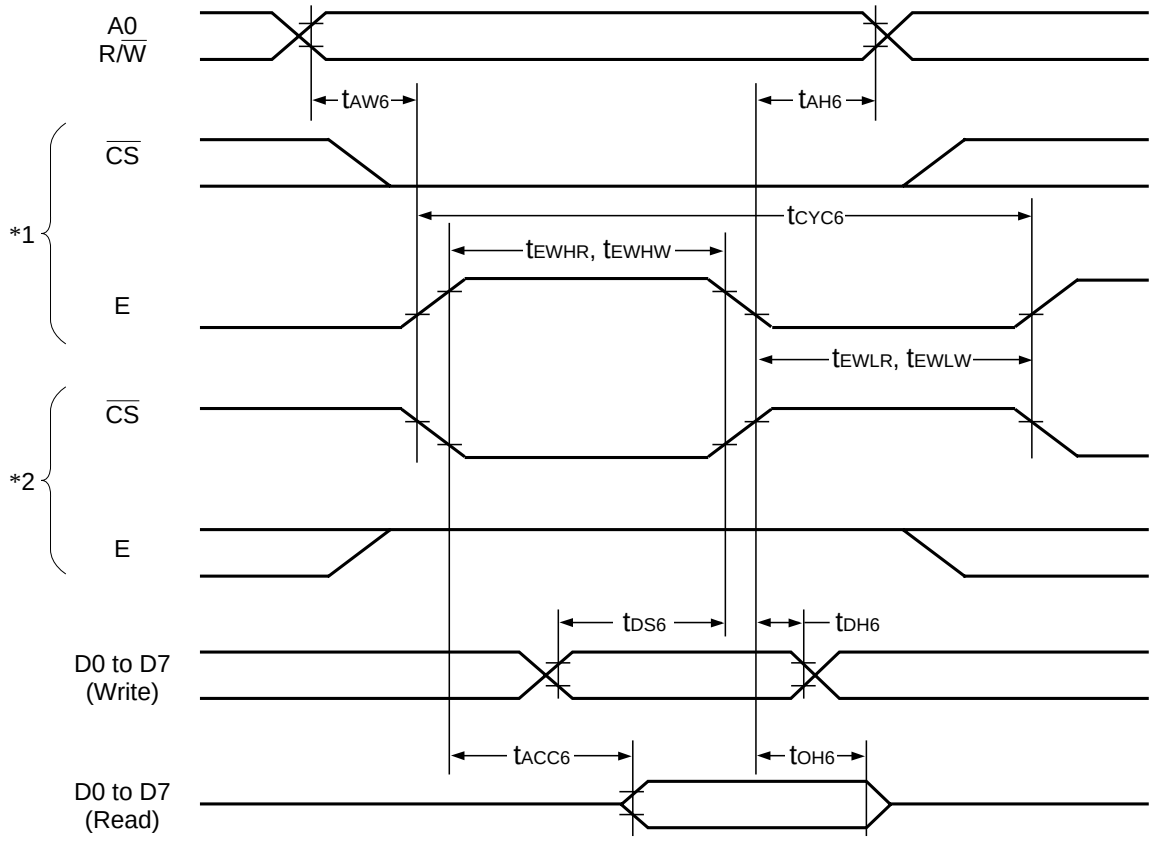


Fig. 27

Table 29

[V_{DD}=4.5V to 5.5V, Ta=–40 to +85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		10	—	ns
Address setup time			t_{AW6}		10	—	
System cycle time			t_{CYC6}		300	—	
Data setup time		D0 to D7	t_{DS6}		40	—	
Data hold time			t_{DH6}		0	—	
Access time			t_{ACC6}	C_L=100pF	—	90	
Output disable time			t_{OH6}		5	70	
Enable HIGH pulse width	Read	E	t_{EWHR}		100	—	
	Write		t_{EWHW}		50	—	
Enable LOW pulse width	Read	E	t_{EWLR}		50	—	
	Write		t_{EWLW}		50	—	

Table 30

[V_{DD}=2.7V to 4.5V, Ta=–40 to +85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		15	—	ns
Address setup time			t_{AW6}		15	—	
System cycle time			t_{CYC6}		500	—	
Data setup time		D0 to D7	t_{DS6}		70	—	
Data hold time			t_{DH6}		0	—	
Access time			t_{ACC6}	C_L=100pF	—	180	
Output disable time			t_{OH6}		5	100	
Enable HIGH pulse width	Read	E	t_{EWHR}		200	—	
	Write		t_{EWHW}		100	—	
Enable LOW pulse width	Read	E	t_{EWLR}		100	—	
	Write		t_{EWLW}		100	—	

Table 31

[V_{DD}=1.8V to 2.7V, Ta=–40 to +85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		20	—	ns
Address setup time			t_{AW6}		20	—	
System cycle time			t_{CYC6}		1000	—	
Data setup time		D0 to D7	t_{DS6}		120	—	
Data hold time			t_{DH6}		0	—	
Access time			t_{ACC6}	C_L=100pF	—	260	
Output disable time			t_{OH6}		10	200	
Enable HIGH pulse width	Read	E	t_{EWHR}		300	—	
	Write		t_{EWHW}		150	—	
Enable LOW pulse width	Read	E	t_{EWLR}		150	—	
	Write		t_{EWLW}		150	—	

*1 This is the case of accessing by E when $\overline{CS}$ = LOW.
*2 This is the case of accessing by $\overline{CS}$ when E = HIGH.
*3 The rise and fall times (t_r and t_f) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for (t_r+t_f) ≤ (t_{CYC6}–t_{EWLW}–t_{EWHW}) or (t_r+t_f) ≤ (t_{CYC6}–t_{EWLR}–t_{EWHR}).
*4 All timings are specified based on the 20 and 80% of V_{DD}.
*5 t_{EWLW} and t_{EWLR} are specified for the overlap period when $\overline{CS}$ is at LOW level and E is at the HIGH level.

(3) Serial interface

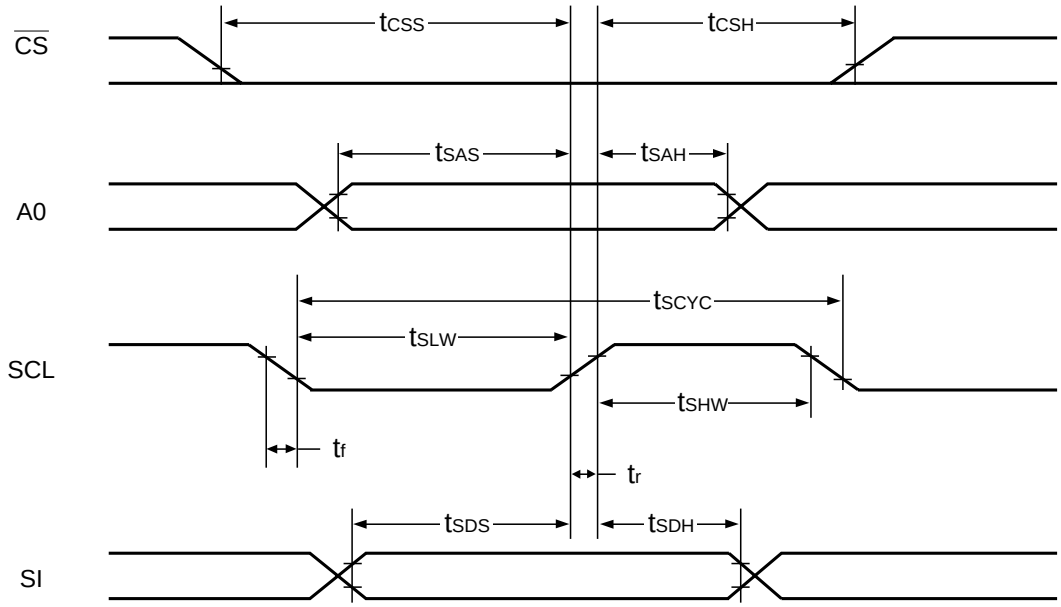


Fig. 28

Table 32

[V_{DD}=4.5V to 5.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		120	—	ns
SCL HIGH pulse width		t_{SHW}		40	—	
SCL LOW pulse width		t_{SLW}		40	—	
Address setup time	A0	t_{SAS}		50	—	
Address hold time		t_{SAH}		50	—	
Data setup time	SI	t_{SDS}		25	—	
Data hold time		t_{SDH}		25	—	
CS-SCL time	CS	t_{CSS}		50	—	
		t_{CSH}		50	—	

Table 33

[V_{DD}=2.7V to 4.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		150	—	ns
SCL HIGH pulse width		t_{SHW}		50	—	
SCL LOW pulse width		t_{SLW}		50	—	
Address setup time	A0	t_{SAS}		75	—	
Address hold time		t_{SAH}		75	—	
Data setup time	SI	t_{SDS}		50	—	
Data hold time		t_{SDH}		50	—	
CS-SCL time	CS	t_{CSS}		75	—	
		t_{CSH}		75	—	

Table 34

[V_{DD}=1.8V to 2.7V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		200	—	ns
SCL HIGH pulse width		t_{SHW}		75	—	
SCL LOW pulse width		t_{SLW}		75	—	
Address setup time	A0	t_{SAS}		75	—	
Address hold time		t_{SAH}		75	—	
Data setup time	SI	t_{SDS}		50	—	
Data hold time		t_{SDH}		50	—	
CS-SCL time	CS	t_{CSS}		100	—	
		t_{CSH}		100	—	

*1 The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns.
*2 All timings are specified based on the 20 and 80% of V_{DD}.

(4) Display control output timing

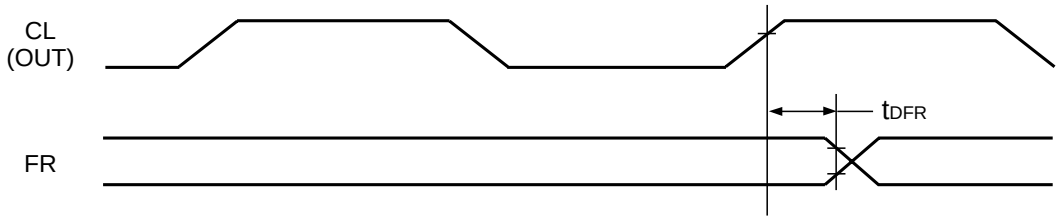


Fig. 29

Table 35

[V_{DD}=4.5V to 5.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L=50pF	—	10	40	ns

Table 36

[V_{DD}=2.7V to 4.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L=50pF	—	20	80	ns

Table 37

[V_{DD}=1.8V to 2.7V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L=50pF	—	50	200	ns

*1 Valid only when the master mode is selected.
*2 All timings are specified based on the 20 and 80% of V_{DD}.
*3 Pay attention not to cause delays of the timing signals CL and FR to the salve side by wiring resistance, etc., while master/slave operations are in progress. If these delays occur, indication failures such as flickering may occur.

(5) Reset input timing

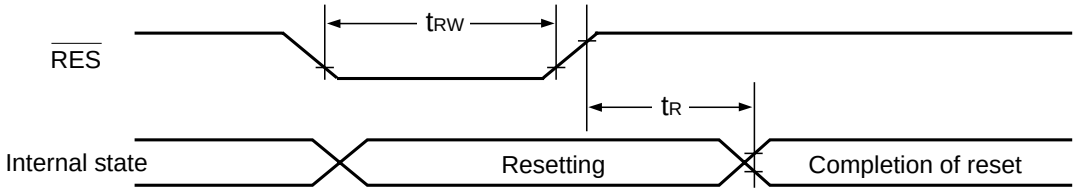


Fig. 30

Table 38

[V_{DD}=4.5V to 5.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	500	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		500	—	—	

Table 39

[V_{DD}=2.7V to 4.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1000	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1000	—	—	

Table 40

[V_{DD}=1.8V to 2.7V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1500	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1500	—	—	

*1 All timings are specified based on the 20 and 80% of V_{DD}.

11. MICROPROCESSOR (MPU) INTERFACE: REFERENCE

The S1D15711 Series can directly be connected to the 80 system MPU and 68 series MUP. It can also be operated with a fewer signal lines by using the serial interface.
The S1D15711 Series is used for the multiple chip configuration to expand the display area. In this case, it can select the ICs that are accessed individually using the Chip Select signal.
After the initialization using the $\overline{RES}$ pin, the respective input pins of the S1D15711 Series need to be controlled normally.

(1) 80 series MPU

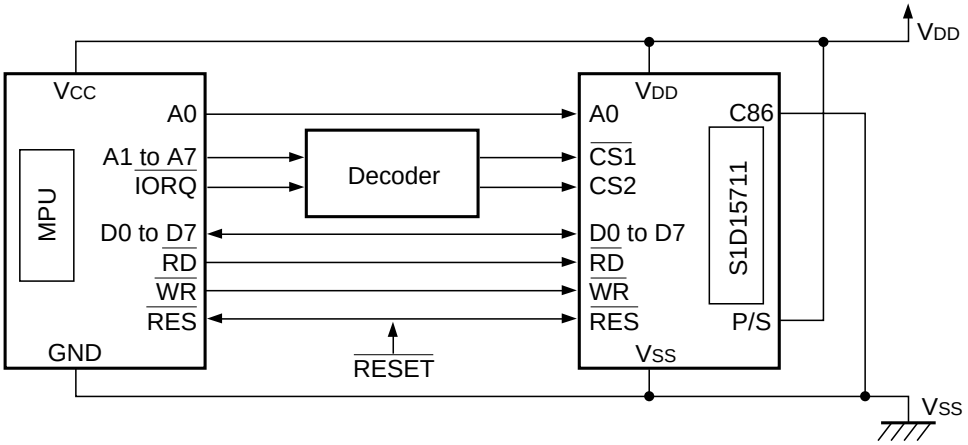


Fig. 31-1

(2) 68 series MPU

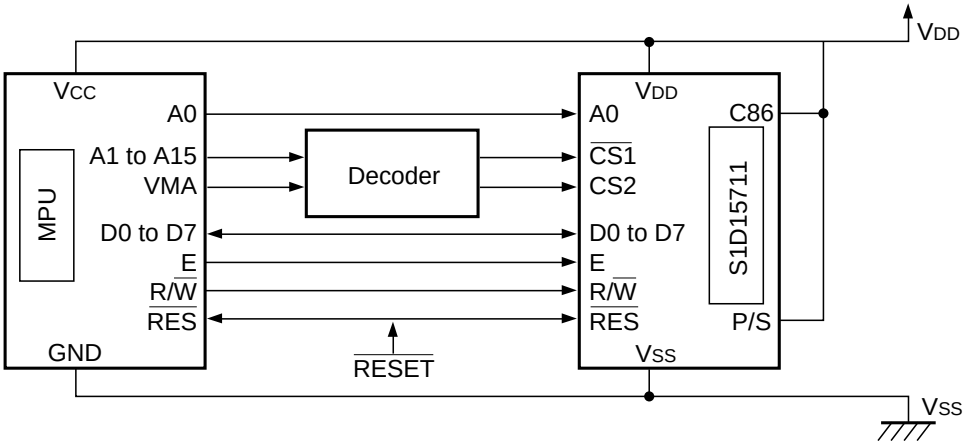


Fig. 31-2

(3) Serial interface

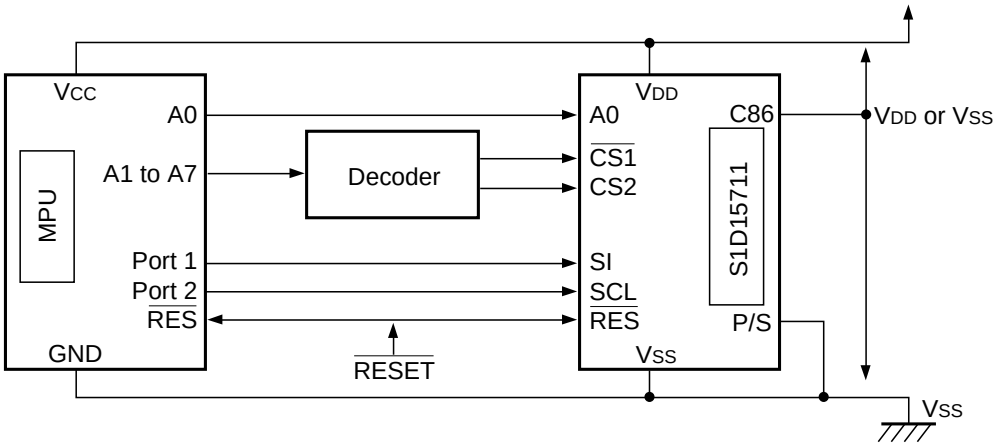


Fig. 31-3

12. CONNECTION BETWEEN LCD DRIVERS: REFERENCE

The S1D15711 Series is used for the multiple chip configuration to easily expand the liquid crystal display area. Use the same device (S1D15711✱✱✱✱✱/S1D15711✱✱✱✱✱) for the master/slave.

S1D15711(master) ↔ S1D15711(slave)

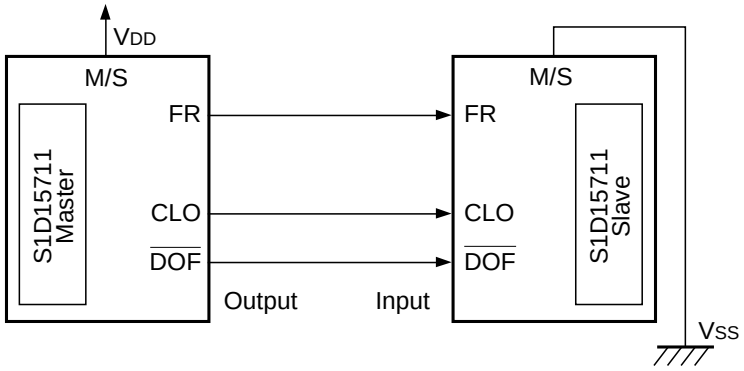


Fig. 32

13. LCD PANEL WIRING: REFERENCE

The S1D15711 Series is used for the multiple chip configuration to easily expand the liquid crystal display area. Use the same device (S1D15711*****/S1D15711*****) for the multiple chip configuration.

(1) 1-chip configuration

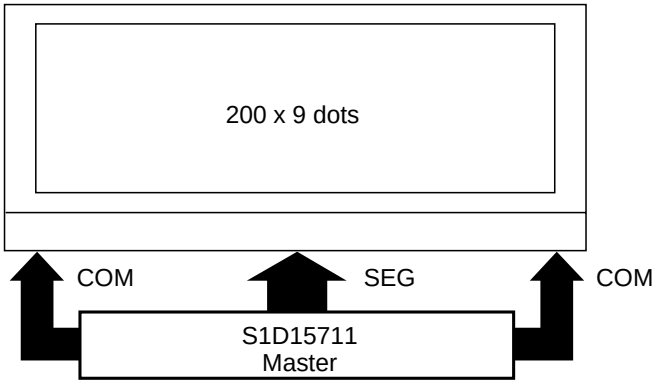


Fig. 33-1

(2) 2-chip configuration

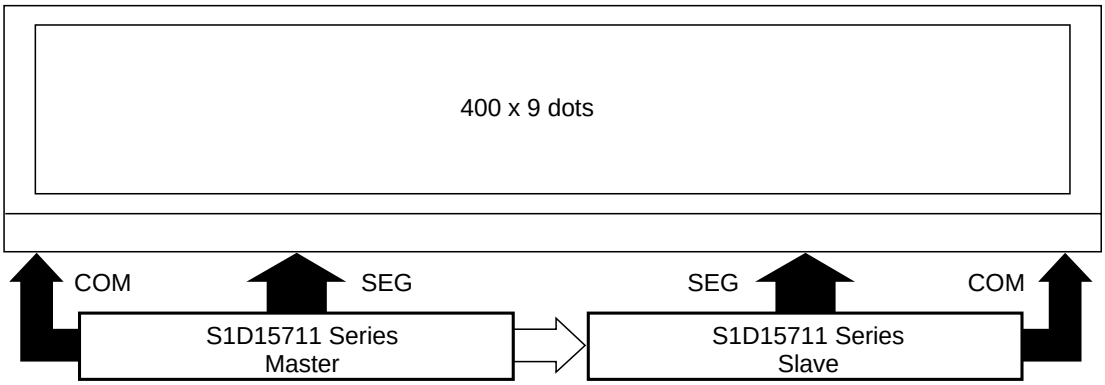


Fig. 33-2

14. CAUTIONS

Cautions must be exercised on the following points when using this Development Specification:

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2. This Development Specification does not guarantee execution of the industrial proprietary rights or other rights, or grant a license. Examples of applications described in This Development Specification are intended for your understanding of the Product. We are not responsible for any circuit problem or the like arising from the use of them.
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For the use of the semi-conductor,cautions must be exercised on the following points:

[Cautions against Light]

The semiconductor will be subject to changes in characteristics when light is applied. If this IC is exposed to light, operation error may occur. To protect the IC against light, the following points should be noted regarding the substrate or product where this IC is mounted:

(1) Designing and mounting must be provided to get a structure which ensures a sufficient resistance of the IC to light in practical use.
(2) In the inspection process, environmental configuration must be provided to ensure a sufficient resistance of the IC to light.
(3) Means must be taken to ensure resistance to light on all the surfaces, backs and sides of the IC

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