

Crystal oscillator

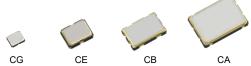
CRYSTAL OSCILLATOR (Programmable) SPREAD SPECTRUM OUTPUT: CMOS

SG-9101 series

- Frequency range: 0.67 MHz to 170 MHz (1 ppm Step)
- Supply voltage : 1.62 V to 3.63 V : Output enable (OE) or Standby (ST)
- Function
- Configurable spread spectrum settings:
 - 2 kinds of spread type, 6 kinds of spread width
 - 4 kinds of modulation frequency, 3 kinds of spread profile
- PLL technology to enable short lead time
- Available field oscillator programmer "SG-Writer II"



Product Number SG-9101CA: X1G005301xxxx00 SG-9101CB: X1G005311xxxx00 SG-9101CE: X1G005321xxxx00 SG-9101CG: X1G005291xxxx00



2.5 × 2.0 mm 3.2 × 2.5 mm

5.0 × 3.2 mm 7.0 × 5.0 mm

Specificat	ions (cha	racteristi	cs)						
Item		Symbol	Specifications			Conditions/Remarks			
Supply voltage		Vcc	1.80 V Typ. 2.50 V Typ. 3.30 V Typ.			_	-		
			1.62 V to 1.98 V		2.20 V to 2.80 V	2.70 V to 3.63 V			
Output frequency range		f _O			to 170 MHz				
Storage temperature		T_stg	-40 °C to +125 °C				Storage as single product.		
Operating temperature		T_use	-40 °C to +85 °C						
			-40 °C to +105 °C						
Frequency tolerance ^{*1}		f_tol	±50 × 10 ⁻⁶		Average frequency of 1s gate time.				
Current consumption		lcc	3.4 mA Max.	3.5 mA Max.	3.6 mA Max.	3.7 mA Max.	T_use = +105 °C	No load, fo = 20 MHz	
			2.9 mA Typ.		3.0 mA Typ.	3.2 mA Typ.	T_use = +25 °C		
ourion concur	iption	100	5.7 mA Max.	6.0 mA Max.	6.9 mA Max.	8.3 mA Max.	T_use = +105 °C	No load, f _o = 170 MHz	
				А Тур.	5.9 mA Typ.	7.0 mA Typ.	T_use = +25 °C		,10 110 1112
Output disable of	current	I_dis	3.4 mA Max.	3.4 mA Max.	3.5 mA Max.	3.7 mA Max.	OE = GND, f _o = 170 M	lHz	
Standby current	ł	I_std	0.9 µA Max.	1.0 µA Max.	1.5 µA Max.	2.5 µA Max.	T_use = +105 °C	ST = GND	
			0.3 µА Тур.	0.4 µA Typ.	0.5 µA Typ.	1.1 µA Typ.	T_use = +25 °C	01 - 010	
Symmetry Output voltage (DC characteristics)		SYM		45 % t	to 55 %		50 % V _{CC} Level		
		Vон		90 %	V _{cc} Min.	I_{OH}/I_{OL} Conditions Rise/Fall time Default (f _O > 40 MHz Fast	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		
		Vol	10 % V _{cc} Max.				$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$		
Output load condition		L_CMOS	15 pF Max.					-	
		VIH	70 % V _{CC} Min.				ar at		
Input voltage		VIL		30 % \	/ _{cc} Max.	OE or ST			
			3.0 ns Max.			f ₀ > 40 MHz			
Rise time	Default	tr/tf	6.0 ns Max.			f ₀ ≤ 40 MHz	-		
/Fall time	Fast		3.0 ns Max.						f ₀ = 0.67 MHz to 170 M
	Slow		10.0 ns Max.						f ₀ = 0.67 MHz to 20 M
Output disable time (OE) Output disable time (ST)		tstp_oe tstp_st	1 µs Max.				Measured from the time OE or $\overline{\text{ST}}$ pin crosses 30 % V_{CC}		
Output enable time (OE)		tsta_oe	1 μs Max.				Measured from the time OE pin crosses 70 % V_{CC}		
Output enable time (ST)		tsta_st	3 ms Max.				Measured from the time \overline{ST} pin crosses 70 % V _{CC}		
Start-up time		t_str	3 ms Max.				Measured from the time V_{CC} reaches its rated minimum value, 1.62 V		
Frequency aging		f_age	This is included in frequency tolerance specification.			+25 °C, first year			

*1 Frequency tolerance includes initial frequency tolerance, frequency / temperature characteristics, frequency / voltage coefficient, frequency / load coefficient and frequency aging (+25 °C, 1 year).

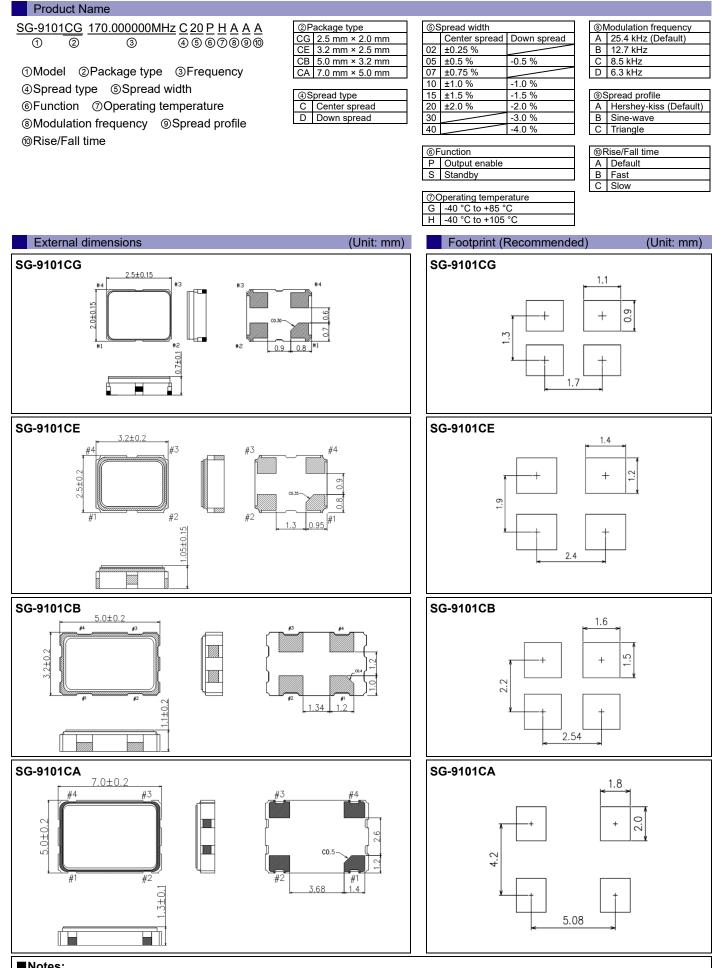
P	Pin description								
Pin	Name	I/O type		Function					
1	OE	Input	Output enable	High ^{*2} : Specified frequency output from OUT pin					
	UE			Low: Out pin is low (weak pull down), only output driver is disabled.					
		Input	Standby	High ^{*2} : Specified frequency output from OUT pin					
	ST			Low: Out pin is low (weak pull down),					
				Device goes to standby mode. Supply current reduces to the least as 1 std.					
2	GND	Power	Ground						
3	OUT	Output	Clock output						
4	V _{cc}	Power	Power supply						
*2 Please de not use the OF/ST terminal in the appendiate									

2 Please do not use the OE/ST terminal in the open state.

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Notes:

In order to achieve optimum jitter performance, the 0.1 µF capacitor between V_{CC} and GND should be placed. It is also recommended that the capacitors are placed on the device side of the PCB, as close to the device as possible and connected together with short wiring pattern.

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