ESP32-S3 Series

Datasheet

2.4 GHz Wi-Fi + Bluetooth® LE SoC

Supporting IEEE 802.11b/g/n (2.4 GHz Wi-Fi) and Bluetooth 5 (LE)

Including:

- ESP32-S3
- ESP32-S3FN8
- ESP32-S3R2
- ESP32-S3R8
- ESP32-S3R8V

Prerelease version 0.6.1 (for chip revision 1)
Espressif Systems

Product Overview

ESP32-S3 is a low-power MCU-based SoC that supports 2.4 GHz Wi-Fi and Bluetooth® Low Energy (Bluetooth LE). It consists of high-performance dual-core MCU (Xtensa® 32-bit LX7), a low power coprocessor, a Wi-Fi baseband, a Bluetooth LE baseband, RF module, and peripherals. The block diagram of the SoC is shown below.

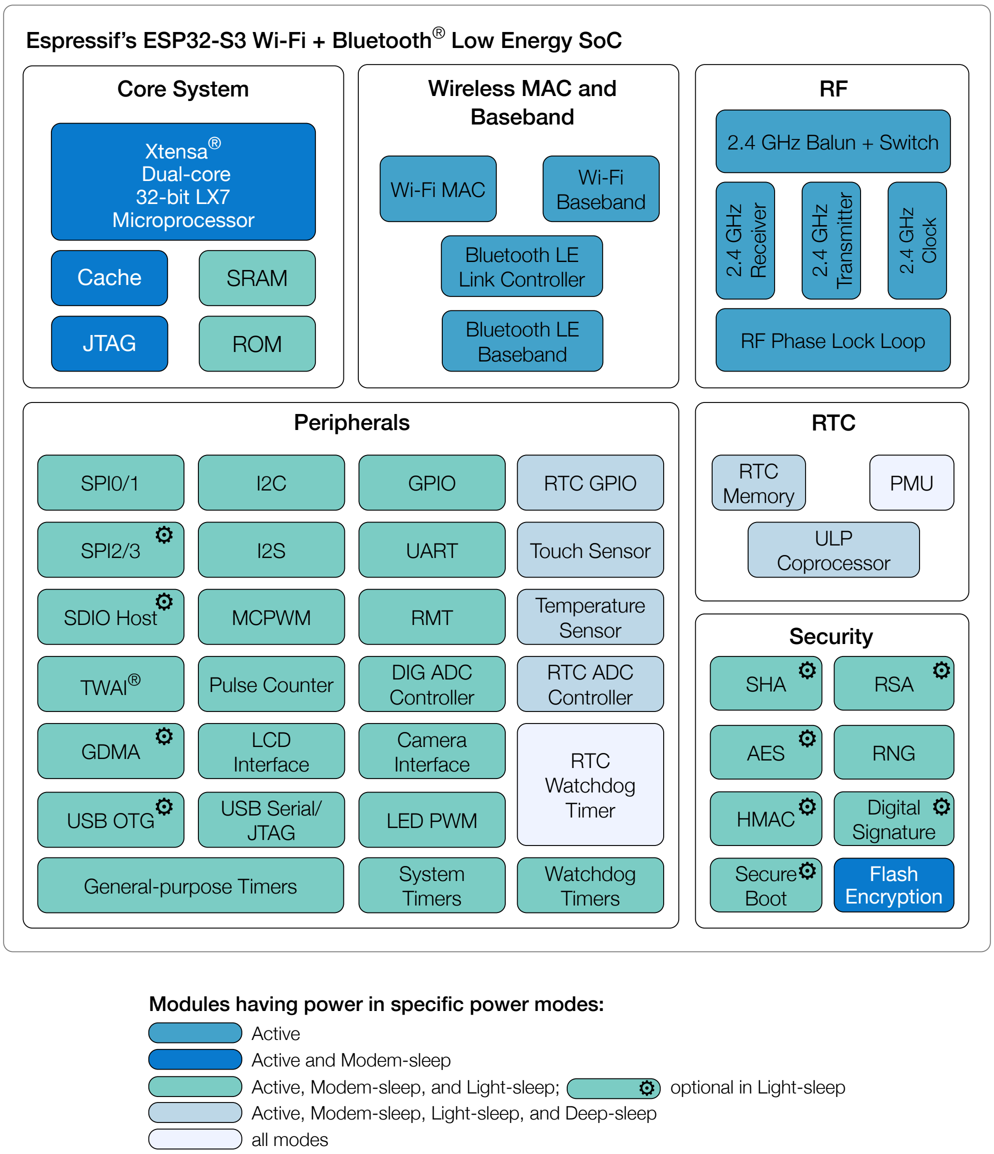

Figure 1: Block Diagram of ESP32-S3

Solution Highlights

- **A complete Wi-Fi subsystem** that complies with IEEE 802.11b/g/n protocol and supports Station, SoftAP, and SoftAP + Station modes
- **A Bluetooth LE subsystem** that supports features of Bluetooth 5 and Bluetooth mesh
- **Xtensa® 32-bit LX7 dual-core processor** with a five-stage pipeline that operates at up to 240 MHz

- A 128-bit data bus and dedicated SIMD instructions to provide high computing performance
  - Efficient L1 cache to improve execution of external memory
  - Single-precision floating-point unit (FPU) to accelerate computing
- **Highly-integrated RF module** that provides industry-leading power and RF performance
- **State-of-the-art power management** designed for a wide range of applications with its multiple low-power modes. The ULP coprocessor can operate in ultra-low-power mode.
- **Powerful storage capacities** ensured by 512 KB SRAM and 384 KB ROM on the chip, and SPI, Dual SPI, Quad SPI, Octal SPI, QPI, and OPI interfaces that allow connection to flash and external RAM
- **Reliable security features** ensured by
  - Cryptographic hardware accelerators that support AES-128/256, Hash, RSA, HMAC, digital signature, and secure boot
  - Random number generator
  - Permission control on accessing internal and external memory
  - External memory encryption and decryption
- **Rich set of peripheral interfaces and GPIOs,** ideal for various scenarios and complex applications

Features

Wi-Fi

- IEEE 802.11 b/g/n-compliant
- Supports 20 MHz, 40 MHz bandwidth in 2.4 GHz band
- 1T1R mode with data rate up to 150 Mbps
- Wi-Fi Multimedia (WMM)
- TX/RX A-MPDU, TX/RX A-MSDU
- Immediate Block ACK
- Fragmentation and defragmentation
- Automatic Beacon monitoring (hardware TSF)
- 4 × virtual Wi-Fi interfaces
- Simultaneous support for Infrastructure BSS in Station, SoftAP, or Station + SoftAP modes
  Note that when ESP32-S3 scans in Station mode, the SoftAP channel will change along with the Station channel
- Antenna diversity
- 802.11mc FTM
- External PA is supported

Bluetooth

- Bluetooth LE: Bluetooth 5, Bluetooth mesh
- High power mode (20 dBm, share the same PA with Wi-Fi)
- 2 Mbps PHY
- Long range mode
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2
- Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna

CPU and Memory

- Xtensa® dual-core 32-bit LX7 microprocessor, up to 240 MHz
- CoreMark® score:
  - 1 core at 240 MHz: 613.86 CoreMark; 2.56 CoreMark/MHz
  - 2 cores at 240 MHz: 1181.60 CoreMark; 4.92 CoreMark/MHz
- 128-bit data bus and SIMD commands

- 384 KB ROM
- 512 KB SRAM
- 16 KB SRAM in RTC
- SPI, Dual SPI, Quad SPI, Octal SPI, QPI and OPI interfaces that allow connection to multiple flash and external RAM
- Flash controller with cache is supported
- Flash in-Circuit Programming (ICP) is supported

Advanced Peripheral Interfaces

- 45 × programmable GPIOs
- Digital interfaces:
  - 4 × SPI
  - 1 × LCD interface (8-bit ~16-bit parallel RGB, I8080 and MOTO6800), supporting conversion between RGB565, YUV422, YUV420 and YUV411
  - 1 × DVP 8-bit ~16-bit camera interface
  - 3 × UART
  - 2 × I2C
  - 2 × I2S
  - 1 × RMT (TX/RX)
  - 1 × pulse counter
  - LED PWM controller, up to 8 channels
  - 1 × full-speed USB OTG
  - 1 × USB Serial/JTAG controller
  - 2 × MCPWM
  - 1 × SDIO host controller with 2 slots
  - DMA controller, with 5 transmit channels and 5 receive channels
  - 1 × TWAI® controller, compatible with ISO 11898-1 (CAN Specification 2.0)
- Analog interfaces:
  - 2 × 12-bit SAR ADCs, up to 20 channels
  - 1 × temperature sensor
  - 14 × touch sensing IOs
- Timers:
  - 4 × 54-bit general-purpose timers
  - 1 × 52-bit system timer
  - 3 × watchdog timers

Low Power Management

- Power Management Unit with five power modes
- Ultra-Low-Power (ULP) coprocessors:
  - ULP-RISC-V coprocessor
  - ULP-FSM coprocessor

Security

- Secure boot
- Flash encryption
- 4096-bit OTP, up to 1652 bits for users
- Cryptographic hardware acceleration:
  - AES-128/256 (FIPS PUB 197)
  - Hash (FIPS PUB 180-4)
  - RSA
  - Random Number Generator (RNG)
  - HMAC
  - Digital signature

Applications (A Non-exhaustive List)

With low power consumption, ESP32-S3 is an ideal choice for IoT devices in the following areas:

- Smart Home
  - Light control
  - Smart button
  - Smart plug
- Industrial Automation
  - Industrial robot

- Mesh network
- Human machine interface (HMI)
- Health Care
  - Health monitor
  - Baby monitor
- Consumer Electronics
  - Smart watch and bracelet
  - Over-the-top (OTT) devices
  - Wi-Fi and bluetooth speaker
  - Logger toys and proximity sensing toys
- Smart Agriculture
  - Smart greenhouse
  - Smart irrigation
  - Agriculture robot
- Retail and Catering
  - POS machines
  - Service robot
- Audio Device
  - Internet music players
  - Live streaming devices
  - Internet radio players
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- USB Devices
- Speech Recognition
- Image Recognition
- Wi-Fi + Bluetooth Networking Card
- Touch Sensing
  - Waterproof design
  - Distance sensing applications
  - Linear slider, wheel slider designs

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1.1 ESP32-S3 Series Nomenclature

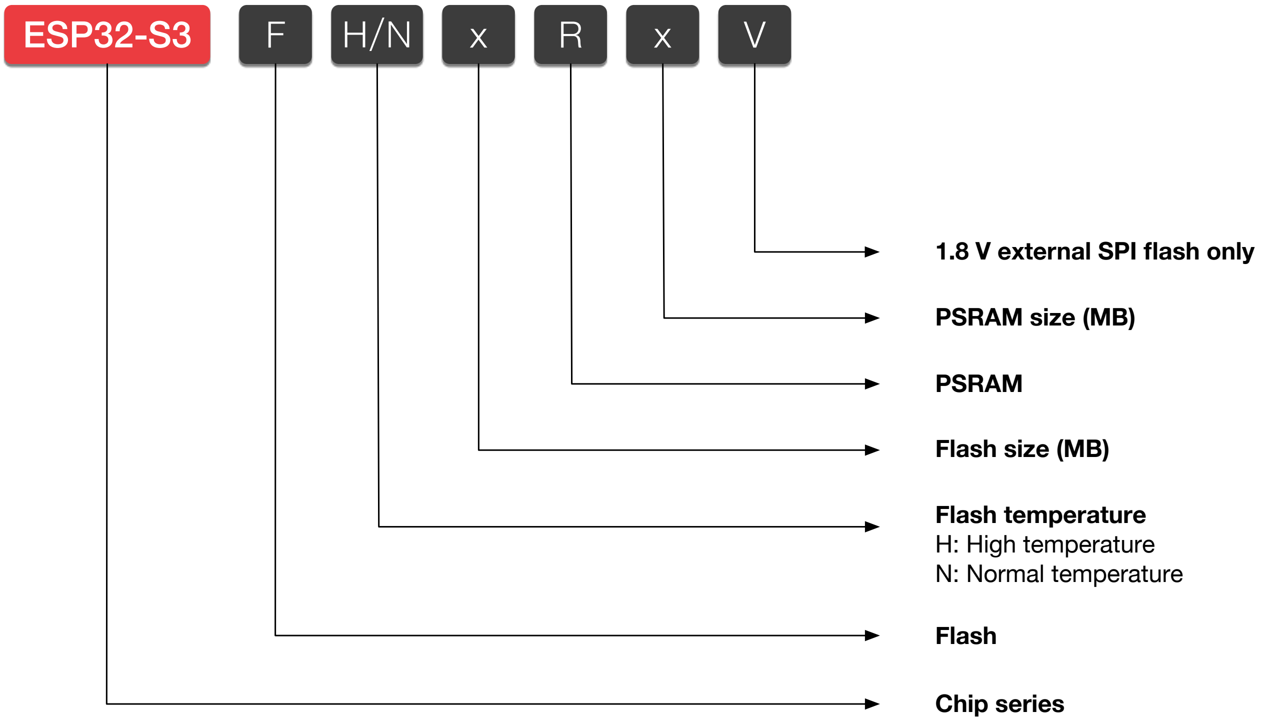

Figure 2: ESP32-S3 Series Nomenclature

1.2 Comparison

Table 1: ESP32-S3 Series Comparison

Ordering Code	SiP flash	SiP PSRAM	Ambient Temperature (°C)	SPI Voltage
ESP32-S3	—	—	–40 ∼ 105	3.3 V/1.8 V
ESP32-S3FN8	8 MB (Quad SPI)	—	–40 ∼ 85	3.3 V
ESP32-S3R2	—	2 MB (Quad SPI)	–40 ∼ 85	3.3 V
ESP32-S3R8	—	8 MB (Octal SPI)	–40 ∼ 85	3.3 V
ESP32-S3R8V	—	8 MB (Octal SPI)	–40 ∼ 85	1.8 V

SiP refers to flash/PSRAM integrated into the package.

Octal SPI occupies five more GPIOs (GPIO33 ∼ GPIO37) than Quad SPI.

2. Pin Definition

2.1 Pin Layout

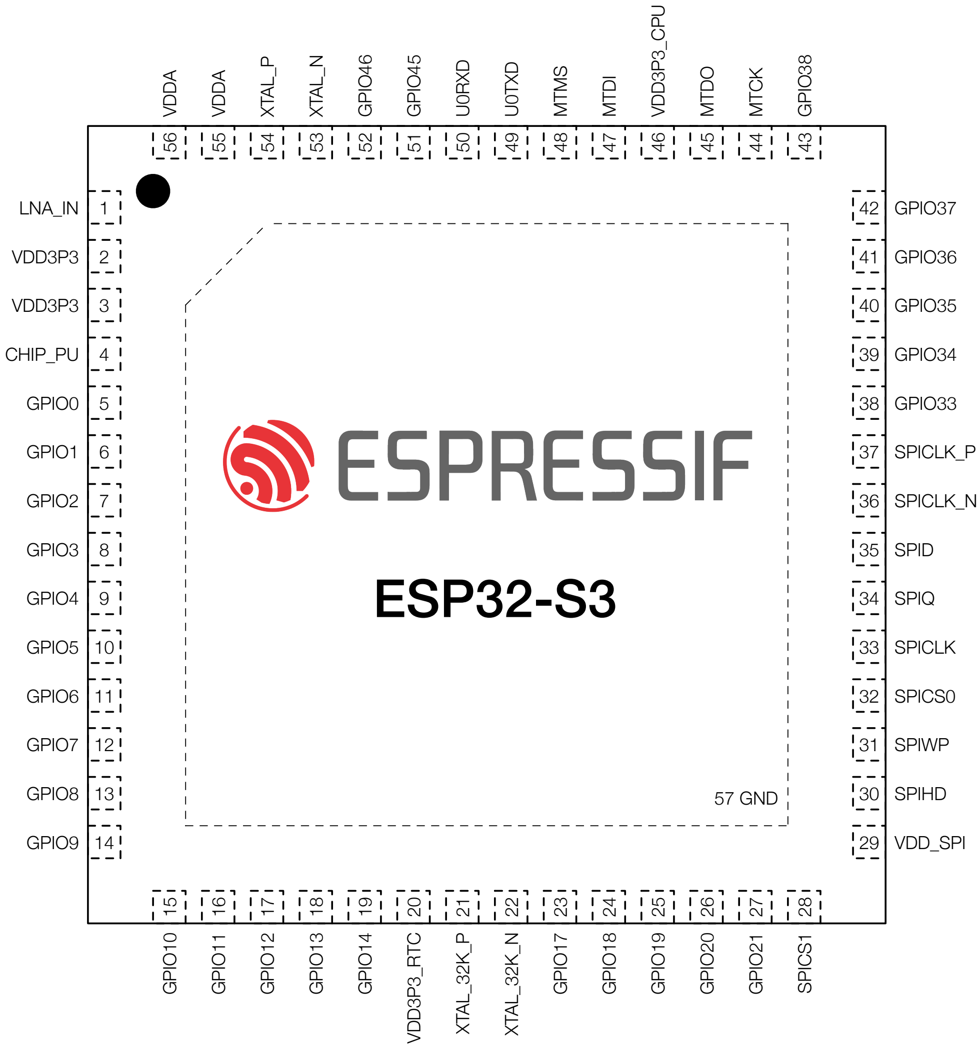

Figure 3: ESP32-S3 Pin Layout (Top View)

2.2 Pin Description

Table 2: Pin Description

Name	No.	Type	Power Domain	Function
LNA_IN	1	I/O	—	Low Noise Amplifier(RF LNA) input and output signal
VDD3P3	2	P_A	—	Analog power supply
VDD3P3	3	P_A	—	Analog power supply
CHIP_PU	4	I	VDD3P3_RTC	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the CHIP_PU pin floating.
GPIO0	5	I/O/T	VDD3P3_RTC	RTC_GPIO0, **GPIO0**
GPIO1	6	I/O/T	VDD3P3_RTC	RTC_GPIO1, **GPIO1**, TOUCH1, ADC1_CH0
GPIO2	7	I/O/T	VDD3P3_RTC	RTC_GPIO2, **GPIO2**, TOUCH2, ADC1_CH1
GPIO3	8	I/O/T	VDD3P3_RTC	RTC_GPIO3, **GPIO3**, TOUCH3, ADC1_CH2
GPIO4	9	I/O/T	VDD3P3_RTC	RTC_GPIO4, **GPIO4**, TOUCH4, ADC1_CH3
GPIO5	10	I/O/T	VDD3P3_RTC	RTC_GPIO5, **GPIO5**, TOUCH5, ADC1_CH4
GPIO6	11	I/O/T	VDD3P3_RTC	RTC_GPIO6, **GPIO6**, TOUCH6, ADC1_CH5
GPIO7	12	I/O/T	VDD3P3_RTC	RTC_GPIO7, **GPIO7**, TOUCH7, ADC1_CH6
GPIO8	13	I/O/T	VDD3P3_RTC	RTC_GPIO8, **GPIO8**, TOUCH8, ADC1_CH7, S
GPIO9	14	I/O/T	VDD3P3_RTC	RTC_GPIO9, **GPIO9**, TOUCH9, ADC1_CH8, S
GPIO10	15	I/O/T	VDD3P3_RTC	RTC_GPIO10, **GPIO10**, TOUCH10, ADC1_CH9, F
GPIO11	16	I/O/T	VDD3P3_RTC	RTC_GPIO11, **GPIO11**, TOUCH11, ADC2_CH0, F
GPIO12	17	I/O/T	VDD3P3_RTC	RTC_GPIO12, **GPIO12**, TOUCH12, ADC2_CH1, F
GPIO13	18	I/O/T	VDD3P3_RTC	RTC_GPIO13, **GPIO13**, TOUCH13, ADC2_CH2, F
GPIO14	19	I/O/T	VDD3P3_RTC	RTC_GPIO14, **GPIO14**, TOUCH14, ADC2_CH3, F
VDD3P3_RTC	20	P_A	—	Analog power supply
XTAL_32K_P	21	I/O/T	VDD3P3_RTC	RTC_GPIO15, **GPIO15**, U0RTS, ADC2_CH4, X
XTAL_32K_N	22	I/O/T	VDD3P3_RTC	RTC_GPIO16, **GPIO16**, U0CTS, ADC2_CH5, X
GPIO17	23	I/O/T	VDD3P3_RTC	RTC_GPIO17, **GPIO17**, U1TXD, ADC2_CH6
GPIO18	24	I/O/T	VDD3P3_RTC	RTC_GPIO18, **GPIO18**, U1RXD, ADC2_CH7, C

Name	No.	Type	Power Domain	Function
GPIO19	25	I/O/T	VDD3P3_RTC	RTC_GPIO19, **GPIO19**, U1RTS, ADC2_CH8,
GPIO20	26	I/O/T	VDD3P3_RTC	RTC_GPIO20, **GPIO20**, U1CTS, ADC2_CH9,
GPIO21	27	I/O/T	VDD3P3_RTC	RTC_GPIO21, **GPIO21**
SPICS1	28	I/O/T	VDD_SPI	SPICS1, **GPIO26**
VDD_SPI	29	P_D	—	Output power supply: 1.8 V or VDD3P3_RTC
SPIHD	30	I/O/T	VDD_SPI	SPIHD, **GPIO27**
SPIWP	31	I/O/T	VDD_SPI	SPIWP, **GPIO28**
SPICS0	32	I/O/T	VDD_SPI	SPICS0, **GPIO29**
SPICLK	33	I/O/T	VDD_SPI	SPICLK, **GPIO30**
SPIQ	34	I/O/T	VDD_SPI	SPIQ, **GPIO31**
SPID	35	I/O/T	VDD_SPI	SPID, **GPIO32**
SPICLK_N	36	I/O/T	VDD_SPI	SPICLK_N_DIFF, **GPIO48**, SUBSPICLK_N_DIFF
SPICLK_P	37	I/O/T	VDD_SPI	SPICLK_P_DIFF, **GPIO47**, SUBSPICLK_P_DIFF
GPIO33	38	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO4, **GPIO33**, FSPIHD, SUBSPIHD
GPIO34	39	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO5, **GPIO34**, FSPICS0, SUBSPICS0
GPIO35	40	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO6, **GPIO35**, FSPID, SUBSPID
GPIO36	41	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO7, **GPIO36**, FSPICLK, SUBSPICLK
GPIO37	42	I/O/T	VDD3P3_CPU / VDD_SPI	SPIDQS, **GPIO37**, FSPIQ, SUBSPIQ
GPIO38	43	I/O/T	VDD3P3_CPU	**GPIO38**, FSPIWP, SUBSPIWP
MTCK	44	I/O/T	VDD3P3_CPU	**MTCK**, GPIO39, CLK_OUT3, SUBSPICS1
MTDO	45	I/O/T	VDD3P3_CPU	**MTDO**, GPIO40, CLK_OUT2
VDD3P3_CPU	46	P_D	—	Input power supply for CPU IO
MTDI	47	I/O/T	VDD3P3_CPU	**MTDI**, GPIO41, CLK_OUT1
MTMS	48	I/O/T	VDD3P3_CPU	**MTMS**, GPIO42
U0TXD	49	I/O/T	VDD3P3_CPU	**U0TXD**, GPIO43, CLK_OUT1
U0RXD	50	I/O/T	VDD3P3_CPU	**U0RXD**, GPIO44, CLK_OUT2
GPIO45	51	I/O/T	VDD3P3_CPU	**GPIO45**
GPIO46	52	I/O/T	VDD3P3_CPU	**GPIO46**
XTAL_N	53	—	—	External crystal output

Name	No.	Type	Power Domain	Function
XTAL_P	54	—	—	External crystal input
VDDA	55	P_A	—	Analog power supply
VDDA	56	P_A	—	Analog power supply
GND	57	G	—	Ground

[1] P: power pin; P_A: analog power pin; P_D: digital power pin; I: input; O: output; T: high impedance.

[2] Pin functions in bold font are the default pin functions.

[3] Power supply for GPIO33, GPIO34, GPIO35, GPIO36 and GPIO37 is configurable to be either VDD3P3_CPU (default)

[4] The pin function in this table refers only to some fixed settings and do not cover all cases for signals that can be inpu
more information on the GPIO matrix, please refer to *ESP32-S3 Technical Reference Manual*.

2.3 Pin Name Description

The explanation of each pin name is briefly described below.

Table 3: Pin Name Description

Pin Name	Description
GPIOx	General-purpose input and output (x is GPIO number). GPIO pins can be assigned various functions, including digital and analog functions. For more information on digital functions, please refer to Table 5.
SPIx	SiP flash/PSRAM and external flash/RAM interface (x is CLK, CS0, CS1, D, Q, WP, HD, IO4~7 or DQS).
XTAL_32K_P/N	32 KHz external clock input/output (connecting to ESP32-S3's oscillator). P/N means differential clock positive/negative.
XTAL_P/N	External clock input/output (connecting to ESP32-S3's oscillator). P/N means differential clock positive/negative.
U0RXD/U0TXD	UART0 receive/transmit signals.
MTCK/MTDO/MTDI/MTMS	JTAG interface signals.
LNA_IN	Low-Noise Amplifier (RF LNA) input/output signals.
CHIP_PU	Chip power up pin.
GND	External ground connection.
VDDA	Power supply for analog domain.
VDD3P3_RTC	Power supply for RTC digital domain.
VDD3P3_CPU	Power supply for digital domain.
VDD_SPI	Power supply for SPI IOs.

2.4 Function Name Description

The explanation of each function name is briefly described below.

Table 4: Function Name Description

Function Name	Description
RTC_GPIOx	RTC domain GPIO function for low power management.
TOUCHx	Analog function for touch sensing.
ADCx_CHy	Analog to digital conversion channel (x is ADC number, y is channel number).
SUBSPIx	Sub-SPI0/1 bus, differing from SPIx bus (x is CLK, CS0, CS1, D, Q, WP or HD), used for different voltage level of flash and PSRAM
FSPIx	8-line Fast-SPI2 bus function (x is CLK, CS0, CS1, D, Q, WP, HD, IO4~7 or DQS)
SPIx	SPI0/1 bus function (x is CLK, CS0, CS1, D, Q, WP, HD, IO4~7 or DQS)
UxRTS/UxCTS	UARTx hardware flow control signals (x is UART number).
U1RXD/U1TXD	UART1 receive/transmit signals.
CLK_OUTx	Clock output for debug (x is clock number).
USB_D-/USB_D+	USB OTG and USB Serial/JTAG function. USB signal is a differential signal transmitted over a pair of D+ and D- wires.
SPICLK_N/P_DIFF	Serial peripheral interface differential clock negative/positive.

2.5 GPIO Functions

ESP32-S3 has 45 GPIO pins (numbering 22-25 is not used) which can be assigned various functions as listed in Table 5. T
(F0-F4). RTC functions and analog functions can be found in Table 2.

Table 5: GPIO Functions

GPIO	Pin Name	F0	Type	F1	Type	F2	Type	F3	Type	F4
0	GPIO0	GPIO0	I/O/T	GPIO0	I/O/T	-	-	-	-	-
1	GPIO1	GPIO1	I/O/T	GPIO1	I/O/T	-	-	-	-	-
2	GPIO2	GPIO2	I/O/T	GPIO2	I/O/T	-	-	-	-	-
3	GPIO3	GPIO3	I/O/T	GPIO3	I/O/T	-	-	-	-	-
4	GPIO4	GPIO4	I/O/T	GPIO4	I/O/T	-	-	-	-	-
5	GPIO5	GPIO5	I/O/T	GPIO5	I/O/T	-	-	-	-	-
6	GPIO6	GPIO6	I/O/T	GPIO6	I/O/T	-	-	-	-	-
7	GPIO7	GPIO7	I/O/T	GPIO7	I/O/T	-	-	-	-	-
8	GPIO8	GPIO8	I/O/T	GPIO8	I/O/T	-	-	SUBSPICS1	O/T	-
9	GPIO9	GPIO9	I/O/T	GPIO9	I/O/T	-	-	SUBSPIHD	I1/O/T	FSPIHD
10	GPIO10	GPIO10	I/O/T	GPIO10	I/O/T	FSPIIO4	I1/O/T	SUBSPICS0	O/T	FSPICS
11	GPIO11	GPIO11	I/O/T	GPIO11	I/O/T	FSPIIO5	I1/O/T	SUBSPID	I1/O/T	FSPID
12	GPIO12	GPIO12	I/O/T	GPIO12	I/O/T	FSPIIO6	I1/O/T	SUBSPICLK	O/T	FSPICL
13	GPIO13	GPIO13	I/O/T	GPIO13	I/O/T	FSPIIO7	I1/O/T	SUBSPIQ	I1/O/T	FSPIQ
14	GPIO14	GPIO14	I/O/T	GPIO14	I/O/T	FSPIDQS	O/T	SUBSPIWP	I1/O/T	FSPIWP
15	XTAL_32K_P	GPIO15	I/O/T	GPIO15	I/O/T	U0RTS	O	-	-	-
16	XTAL_32K_N	GPIO16	I/O/T	GPIO16	I/O/T	U0CTS	I1	-	-	-
17	GPIO17	GPIO17	I/O/T	GPIO17	I/O/T	U1TXD	O	-	-	-
18	GPIO18	GPIO18	I/O/T	GPIO18	I/O/T	U1RXD	I1	CLK_OUT3	O	-
19	GPIO19	GPIO19	I/O/T	GPIO19	I/O/T	U1RTS	O	CLK_OUT2	O	-
20	GPIO20	GPIO20	I/O/T	GPIO20	I/O/T	U1CTS	I1	CLK_OUT1	O	-
21	GPIO21	GPIO21	I/O/T	GPIO21	I/O/T	-	-	-	-	-
26	SPICS1	SPICS1	O/T	GPIO26	I/O/T	-	-	-	-	-
27	SPIHD	SPIHD	I1/O/T	GPIO27	I/O/T	-	-	-	-	-
28	SPIWP	SPIWP	I1/O/T	GPIO28	I/O/T	-	-	-	-	-
29	SPICS0	SPICS0	O/T	GPIO29	I/O/T	-	-	-	-	-

GPIO	Pin Name	F0	Type	F1	Type	F2	Type	F3	Type	F4
30	SPICLK	SPICLK	O/T	GPIO30	I/O/T	-	-	-	-	-
31	SPIQ	SPIQ	I1/O/T	GPIO31	I/O/T	-	-	-	-	-
32	SPID	SPID	I1/O/T	GPIO32	I/O/T	-	-	-	-	-
33	GPIO33	GPIO33	I/O/T	GPIO33	I/O/T	FSPIHD	I1/O/T	SUBSPIHD	I1/O/T	SPIIO4
34	GPIO34	GPIO34	I/O/T	GPIO34	I/O/T	FSPICS0	I1/O/T	SUBSPICS0	O/T	SPIIO5
35	GPIO35	GPIO35	I/O/T	GPIO35	I/O/T	FSPID	I1/O/T	SUBSPID	I1/O/T	SPIIO6
36	GPIO36	GPIO36	I/O/T	GPIO36	I/O/T	FSPICLK	I1/O/T	SUBSPICLK	O/T	SPIIO7
37	GPIO37	GPIO37	I/O/T	GPIO37	I/O/T	FSPIQ	I1/O/T	SUBSPIQ	I1/O/T	SPIDQS
38	GPIO38	GPIO38	I/O/T	GPIO38	I/O/T	FSPIWP	I1/O/T	SUBSPIWP	I1/O/T	-
39	MTCK	MTCK	I1	GPIO39	I/O/T	CLK_OUT3	O	SUBSPICS1	O/T	-
40	MTDO	MTDO	O/T	GPIO40	I/O/T	CLK_OUT2	O	-	-	-
41	MTDI	MTDI	I1	GPIO41	I/O/T	CLK_OUT1	O	-	-	-
42	MTMS	MTMS	I1	GPIO42	I/O/T	-	-	-	-	-
43	U0TXD	U0TXD	O	GPIO43	I/O/T	CLK_OUT1	O	-	-	-
44	U0RXD	U0RXD	I1	GPIO44	I/O/T	CLK_OUT2	O	-	-	-
45	GPIO45	GPIO45	I/O/T	GPIO45	I/O/T	-	-	-	-	-
46	GPIO46	GPIO46	I/O/T	GPIO46	I/O/T	-	-	-	-	-
47	SPICLK_P	SPICLK_P_DIFF	O/T	GPIO47	I/O/T	SUBSPI-CLK_P_DIFF	O/T	-	-	-
48	SPICLK_N	SPICLK_N_DIFF	O/T	GPIO48	I/O/T	SUBSPI-CLK_N_DIFF	O/T	-	-	-

Please refer to the next page for more information on GPIO functions.

Type

Each digital function (F*n*, *n*=0~4) is associated with a "Type". The description of "Type" is as follows:

- O: Output only.
- O/T: The signal can be output or high-impedance.
- I/O/T: The signal can be input, output, and high-impedance.
- I1: Input only. If the pin is assigned a function other than F*n*, the input signal of F*n* is always "1".
- I1/O/T: The signal can be input, output, and high-impedance. If F*n* is not selected, the input signal of F*n* is always "1".
- I0/O/T: The signal can be input, output, and high-impedance. If F*n* is not selected, the input signal of F*n* is always "0".

At Reset/After Reset

The default configuration of each pin at reset and after reset:

- **IE0** - input disabled
- **IE1** - input enabled
- **IE1, WPD1** - input enabled, internal weak pull-down resistor enabled
- **IE1, WPU1** - input enabled, internal weak pull-up resistor enabled
- **IE1, or IE1&WPU1** - When the value of eFuse bit EFUSE_DIS_PAD_JTAG is
  1, the MTCK pin floats after chip reset (IE1)
  0, the MTCK pin connects to internal weak pull-up resistor after chip reset (IE1&WPU1)

Notes

- **R** - These pins have RTC or analog functions.

Drive Strength

- The default drive strength of GPIO27~32 is 2'd3 (~40 mA).
- The default drive strength of other pins is 2'd2 (~20 mA).

2.6 Pin-to-Pin Mapping Between Chip and SiP Flash/PSRAM

Table 6 lists the pin-to-pin mapping between the chip and the SiP flash/PSRAM. The chip pins listed here are not recommended for other usage. For the data port connection between ESP32-S3 and external flash please refer to Section 3.4.2.

Table 6: Pin-to-Pin Mapping Between Chip and SiP Flash/PSRAM

ESP32-S3FN8	SiP flash (8 MB, Quad SPI)
SPICLK	CLK
SPICS0	CS#
SPID	DI
SPIQ	DO
SPIWP	WP#
SPIHD	HOLD#
ESP32-S3R2	**SiP PSRAM (2 MB, Quad SPI)**

SPICLK	CLK
SPICS1	CE#
SPID	SI/SIO0
SPIQ	SO/SIO1
SPIWP	SIO2
SPIHD	SIO3
ESP32-S3R8 / ESP32-S3R8V	**SiP PSRAM (8 MB, Octal SPI)**
SPICLK	CLK
SPICS1	CE#
SPID	DQ0
SPIQ	DQ1
SPIWP	DQ2
SPIHD	DQ3
GPIO33	DQ4
GPIO34	DQ5
GPIO35	DQ6
GPIO36	DQ7
GPIO37	DQS/DM

2.7 Power Scheme

ESP32-S3 has four input power pins:

- VDDA1
- VDDA2
- VDD3P3_RTC
- VDD3P3_CPU

And one input/output power pin:

- VDD_SPI

VDDA1 and VDDA2 are the input power supply for the analog domain.

VDD_SPI can be an input power supply or output power supply. It can be powered by Flash Voltage Regulator (nominal 1.8 V) or by VDD3P3_RTC via R_{SPI} (nominal 3.3 V). As the SiP flash/PSRAM in ESP32-S3FN8, ESP32-S3R2, and ESP32-S3R8 operates at 3.3 V, VDD_SPI must be powered by VDD3P3_RTC via R_{SPI}. Software can power off VDD_SPI to minimize current leakage of flash in Deep-sleep mode.

VDD3P3_RTC is the input power supply for Low Power Voltage Regulator that powers the RTC domain.

VDD3P3_CPU and VDD3P3_RTC power Digital System Voltage Regulator at the same time that further powers the Digital System domain.

VDD3P3_RTC is the input power supply for RTC IO.

VDD3P3_CPU is the input power supply for Digital IO.

VDD_SPI is the input power supply for SPI IO.

Either VDD_SPI or VDD3P3_CPU can be selected as the input power supply for SPI/Digital IO.

The power scheme diagram is shown in Figure 4.

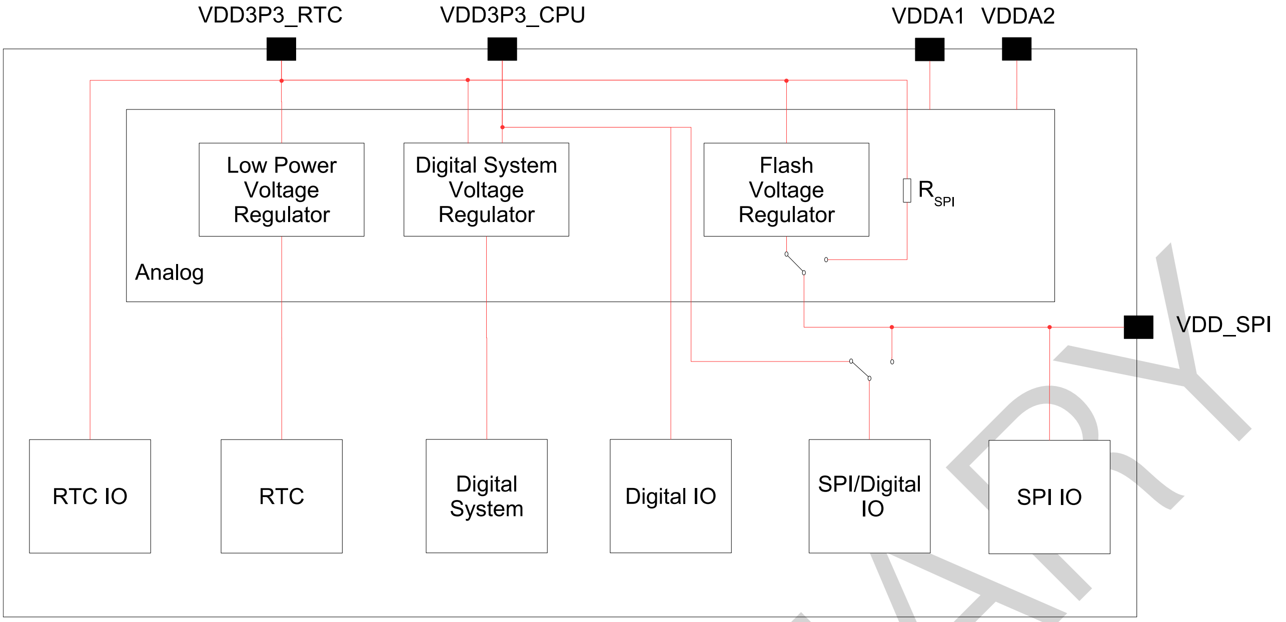

Figure 4: ESP32-S3 Power Scheme

Notes on CHIP_PU:

Figure 5 shows the power-up and reset timing of ESP32-S3 series. Details about the parameters are listed in Table 7.

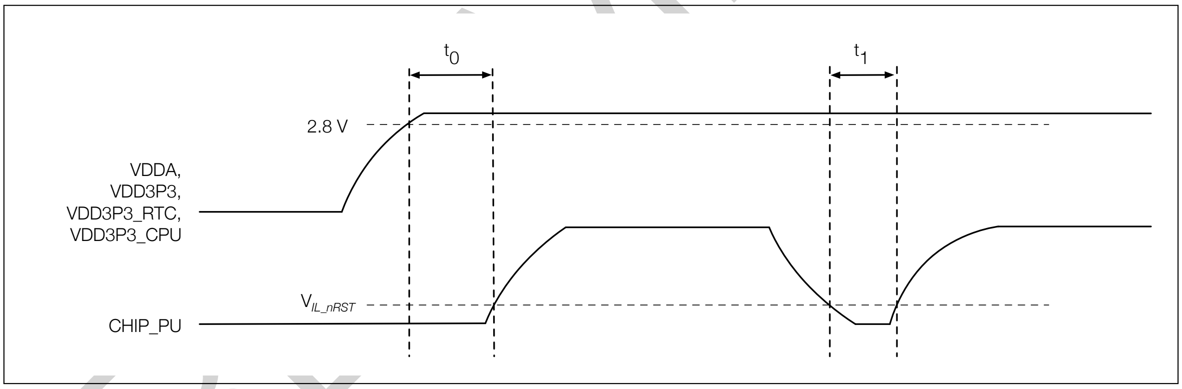

Figure 5: ESP32-S3 Power-up and Reset Timing

Table 7: Description of ESP32-S3 Power-up and Reset Timing Parameters

Parameter	Description	Min (μs)
t_0	Time between bringing up the VDDA, VDD3P3, VDD3P3_RTC, and VDD3P3_CPU rails, and activating CHIP_PU	50
t_1	Duration of CHIP_PU signal level < V_{IL_nRST} (refer to its value in Table 16) to reset the chip	50

2.8 Strapping Pins

ESP32-S3 has four strapping pins:

- GPIO0
- GPIO45
- GPIO46
- GPIO3

Software can read the values of corresponding bits from register "GPIO_STRAPPING".

During the chip's system reset (power-on-reset, RTC watchdog reset, brownout reset, analog super watchdog reset, and crystal clock glitch detection reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down.

GPIO0, GPIO45 and GPIO46 are connected to the chip's internal weak pull-up/pull-down during the chip reset. Consequently, if they are unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of these strapping pins.

GPIO3 is floating by default. Its strapping value can be configured to determine the source of the JTAG signal inside the CPU, as shown in Table 9. In this case, the strapping value is controlled by the external circuit that cannot be in a high impedance state. Table 8 shows more configuration combinations of EFUSE_DIS_USB_JTAG, EFUSE_DIS_PAD_JTAG, and EFUSE_STRAP_JTAG_SEL that determine the JTAG signal source.

Table 8: JTAG Signal Source Selection

EFUSE_STRAP_JTAG_SEL	EFUSE_DIS_USB_JTAG	EFUSE_DIS_PAD_JTAG	JTAG Signal Source
1	0	0	Refer to Table 9
0	0	0	USB Serial/JTAG controller
don't care	0	1	USB Serial/JTAG controller
don't care	1	0	On-chip JTAG pins
don't care	1	1	N/A

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32-S3.

After reset, the strapping pins work as normal-function pins.

Refer to Table 9 for a detailed configuration of the strapping pins.

Table 9: Strapping Pins

VDD_SPI Voltage [1]			
Pin	Default	3.3 V	1.8 V
GPIO45	Pull-down	0	1
Booting Mode [2]			
Pin	Default	SPI Boot	Download Boot
GPIO0	Pull-up	1	0
GPIO46	Pull-down	Don't care	0
Enabling/Disabling ROM Messages Print During Booting [3] [4]			
Pin	Default	Enabled	Disabled
GPIO46	Pull-down	See the fourth note	See the fourth note
JTAG Signal Selection			

Pin	Default	EFUSE_DIS_USB_JTAG = 0, EFUSE_DIS_PAD_JTAG = 0, EFUSE_STRAP_JTAG_SEL=1
GPIO3	N/A	0: JTAG signal from on-chip JTAG pins 1: JTAG signal from USB Serial/JTAG controller

Note:

1. VDD_SPI voltage is determined either by the strapping value of GPIO45 or by VDD_SPI_TIEH. When EFUSE_VDD_SPI_FORCE is 0, VDD_SPI voltage is determined by the strapping value of GPIO45; when EFUSE_VDD_SPI_FORCE is 1, VDD_SPI voltage is determined by VDD_SPI_TIEH.
2. The strapping combination of GPIO46 = 1 and GPIO0 = 0 is invalid and will trigger unexpected behavior.
3. ROM boot messages can be printed over U0TXD (by default) or GPIO17 (U1TXD), depending on the eFuse bit EFUSE_UART_PRINT_CHANNEL.
4. When both EFUSE_DIS_USB_SERIAL_JTAG and EFUSE_DIS_USB_OTG are 0, ROM boot messages will be printed to the USB Serial/JTAG controller. Otherwise, the messages will be printed to UART, controlled by GPIO46 and EFUSE_UART_PRINT_CONTROL. Specifically, when EFUSE_UART_PRINT_CONTROL value is:
   0, print is normal during boot and not controlled by GPIO46.
   1 and GPIO46 is 0, print is normal during boot; but if GPIO46 is 1, print is disabled.
   2 and GPIO46 is 0, print is disabled; but if GPIO46 is 1, print is normal.
   3, print is disabled and not controlled by GPIO46.

Figure 6 shows the setup and hold times for the strapping pin before and after the CHIP_PU signal goes high. Details about the parameters are listed in Table 10.

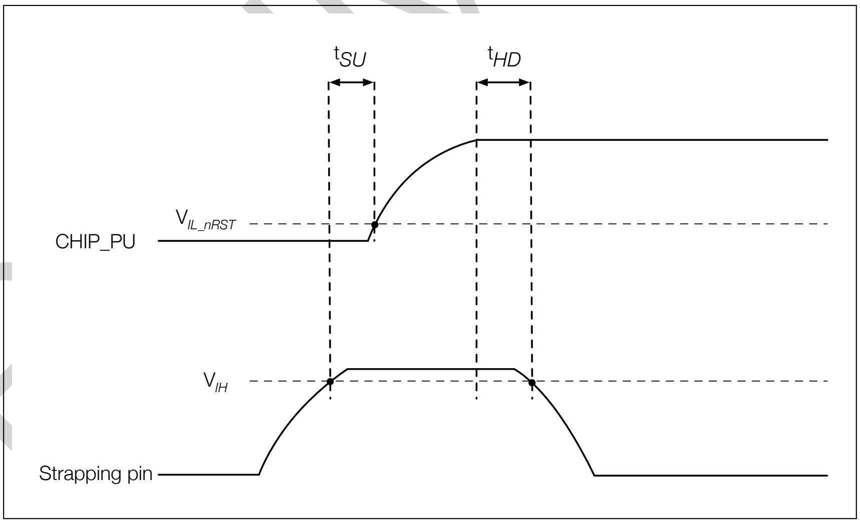

Figure 6: Setup and Hold Times for the Strapping Pin

Table 10: Parameter Descriptions of Setup and Hold Times for the Strapping Pin

Parameter	Description	Min (μs)
t_{SU}	Setup time before CHIP_PU goes from low to high	0
t_{HD}	Hold time after CHIP_PU goes high	3

3. Functional Description

3.1 CPU and Memory

3.1.1 CPU

ESP32-S3 has a low-power Xtensa® dual-core 32-bit LX7 microprocessor with the following features:

- Five-stage pipeline that supports the clock frequency of up to 240 MHz
- 16-bit/24-bit instruction set providing high code density
- 32-bit customized instruction set and 128-bit data bus that provide high computing performance
- Support for single-precision floating-point unit (FPU)
- 32-bit multiplier and 32-bit divider
- Unbuffered GPIO instructions
- 32 interrupts at six levels
- Windowed ABI with 64 physical general registers
- Trace function with TRAX compressor, up to 16 KB trace memory
- JTAG for debugging

3.1.2 Internal Memory

ESP32-S3's internal memory includes:

- **384 KB ROM**: for booting and core functions
- **512 KB on-chip SRAM**: for data and instructions, running at a configurable frequency of up to 240 MHz
- **RTC FAST memory**: 8 KB SRAM that supports read/write/instruction fetch by the main CPU (LX7 dual-core processor). It can retain data in Deep-sleep mode.
- **RTC SLOW Memory**: 8 KB SRAM that supports read/write/instruction fetch by the main CPU (LX7 dual-core processor) or coprocessors. It can retain data in Deep-sleep mode.
- **4 kbit eFuse**: 1652 bits are reserved for user data, such as encryption key and device ID.
- **SiP flash and PSRAM**: See details in Table 1 *Comparison*.

3.1.3 External Flash and RAM

ESP32-S3 supports SPI, Dual SPI, Quad SPI, Octal SPI, QPI and OPI interfaces that allow connection to multiple external flash and RAM.

The external flash and RAM can be mapped into the CPU instruction memory space and read-only data memory space. The external RAM can also be mapped into the CPU data memory space. ESP32-S3 supports up to 1 GB of external flash and RAM, and hardware encryption/decryption based on XTS-AES to protect users' programs and data in flash and external RAM.

Through high-speed caches, ESP32-S3 can support at a time up to:

- External flash or RAM mapped into 32 MB instruction space as individual blocks of 64 KB
- External RAM mapped into 32 MB data space as individual blocks of 64 KB. 8-bit, 16-bit, 32-bit, and 128-bit reads and writes are supported. External flash can also be mapped into 32 MB data space as individual blocks of 64 KB, but only supporting 8-bit, 16-bit, 32-bit and 128-bit reads.

Note:
After ESP32-S3 is initialized, firmware can customize the mapping of external RAM or flash into the CPU address space.

3.1.4 Address Mapping Structure

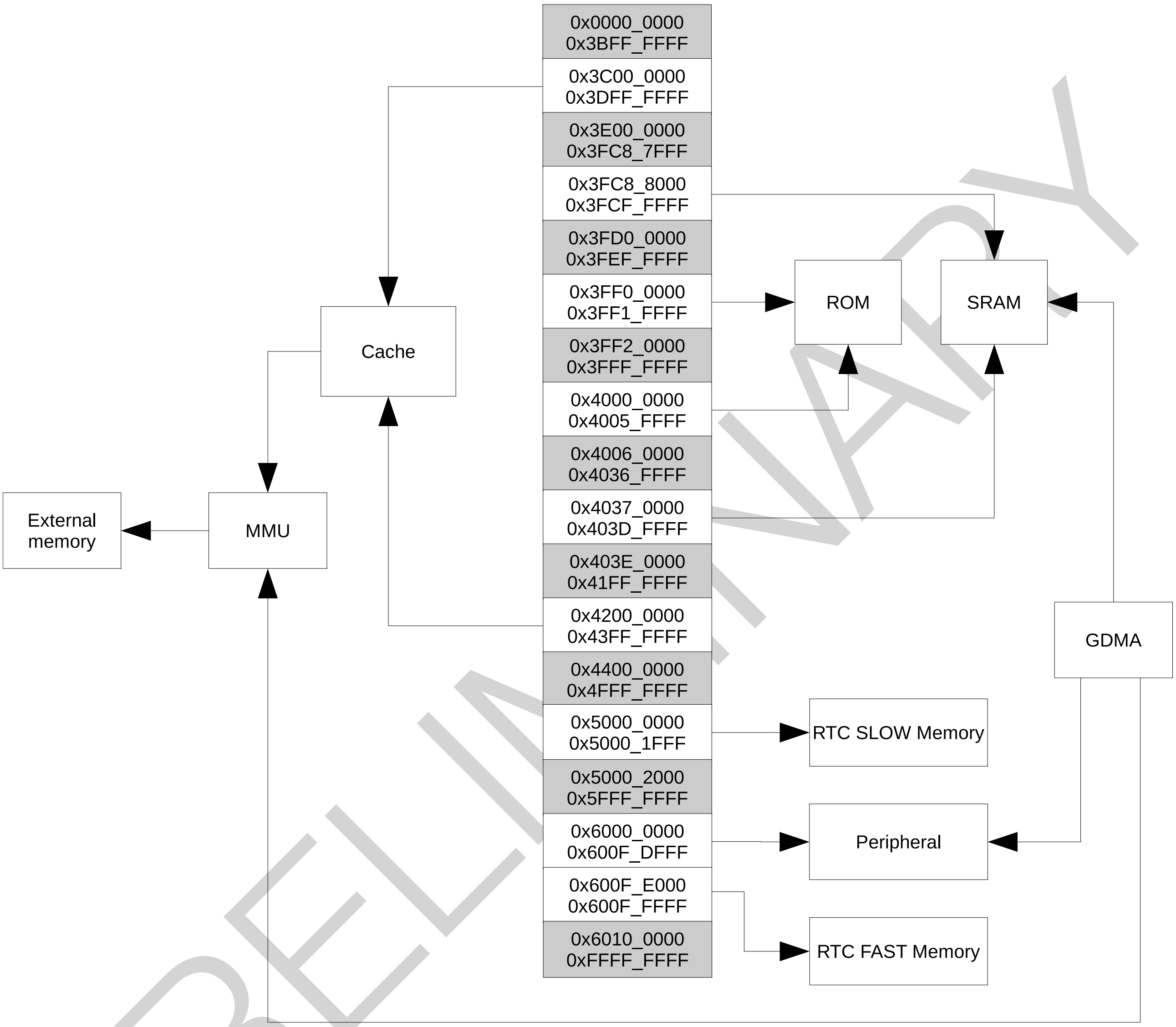

Figure 7: Address Mapping Structure

Note:
The memory space with gray background is not available to users.

3.1.5 Cache

ESP32-S3 has an instruction cache and a data cache shared by the two CPU cores. Each cache can be partitioned into multiple banks and has the following features:

- Instruction cache: 16 KB (one bank) or 32 KB (two banks)
  Data cache: 32 KB (one bank) or 64 KB (two banks)
- Instruction cache: four-way or eight-way set associative

Data cache: four-way set associative

- Block size of 16 bytes or 32 bytes for both instruction cache and data cache
- Pre-load function
- Lock function
- Critical word first and early restart

3.2 System Clocks

3.2.1 CPU Clock

The CPU clock has three possible sources:

- External main crystal clock
- Internal fast RC oscillator (typically about 17.5 MHz, and adjustable)
- PLL clock

The application can select the clock source from the three clocks above. The selected clock source drives the CPU clock directly, or after division, depending on the application. Once the CPU is reset, the default clock source would be the external main crystal clock divided by 2.

3.2.2 RTC Clock

The RTC slow clock is used for RTC counter, RTC watchdog and low-power controller. It has three possible sources:

- External low-speed (32 kHz) crystal clock
- Internal slow RC oscillator (typically about 136 kHz, and adjustable)
- Internal fast RC oscillator divided clock (derived from the internal fast RC oscillator divided by 256)

The RTC fast clock is used for RTC peripherals and sensor controllers. It has two possible sources:

- External main crystal clock divided by 2
- Internal fast RC oscillator (typically about 17.5 MHz, and adjustable)

3.3 Analog Peripherals

3.3.1 Analog-to-Digital Converter (ADC)

ESP32-S3 integrates two 12-bit SAR ADCs and supports measurements on 20 channels (analog-enabled pins). For power-saving purpose, the ULP coprocessors in ESP32-S3 can also be used to measure voltage in sleep modes. By using threshold settings or other methods, we can awaken the CPU from sleep modes.

3.3.2 Temperature Sensor

The temperature sensor generates a voltage that varies with temperature. The voltage is internally converted via an ADC into a digital value.

The temperature sensor has a range of –20 °C to 110 °C. It is designed primarily to sense the temperature changes inside the chip. The temperature value depends on factors such as microcontroller clock frequency or I/O load. Generally, the chip's internal temperature is higher than the ambient temperature.

3.3.3 Touch Sensor

ESP32-S3 has 14 capacitive-sensing GPIOs, which detect variations induced by touching or approaching the GPIOs with a finger or other objects. The low-noise nature of the design and the high sensitivity of the circuit allow relatively small pads to be used. Arrays of pads can also be used, so that a larger area or more points can be detected. The touch sensing performance can be further enhanced by the waterproof design and digital filtering feature.

3.4 Digital Peripherals

3.4.1 General Purpose Input / Output Interface (GPIO)

ESP32-S3 has 45 GPIO pins which can be assigned various functions by configuring corresponding registers. Besides digital signals, some GPIOs can be also used for analog functions, such as ADC, touch sensing, etc.

All GPIOs have selectable internal weak pull-up or pull-down, or can be set to high impedance. When these GPIOs are configured as an input, the input value can be read by software through the register. Input GPIOs can also be set to generate edge-triggered or level-triggered CPU interrupts. All digital IO pins are bi-directional, non-inverting, and tristate, including input and output buffers with tristate control. These pins can be multiplexed with other functions, such as UART, SPI, etc. For low-power operations, the GPIOs can be set to holding state.

The IO MUX and the GPIO matrix are used to route signals from peripherals to GPIO pads. Together they provide highly configurable I/O. Using GPIO Matrix, peripheral input signals can be configured from any IO pads while peripheral output signals can be configured to any IO pad. For more information about IO MUX and GPIO matrix, please refer to *ESP32-S3 Technical Reference Manual*.

3.4.2 Serial Peripheral Interface (SPI)

ESP32-S3 features four SPI interfaces (SPI0, SPI1, SPI2 and SPI3). SPI0 and SPI1 can be configured to operate in SPI memory mode; SPI2 and SPI3 can be configured to operate in general-purpose SPI mode.

- **SPI Memory mode**

  In SPI memory mode, SPI0 and SPI1 interface with external SPI memory. Data transmission is in multiples of bytes. Up to 8-line SDR/DDR (Single Data Rate/Double Data Rate) reads and writes are supported. The clock frequency is configurable to a maximum of 120 MHz for OPI SDR/DDR mode.

- **SPI2 General-purpose SPI (GP-SPI) mode**

  SPI2 can operate in master and slave modes. The master mode supports two-line full-duplex communication and single-/two-/four-/eight-line half-duplex communication. The slave mode supports two-line full-duplex communication and single-/two-/four-line half-duplex communication. The host's clock frequency is configurable. Data transmission is in multiples of bytes. The clock polarity (CPOL) and phase (CPHA) are also configurable. The SPI2 interface supports DMA.

  - In two-line full-duplex communication mode, the host's clock frequency is configurable to 80 MHz at most, and the slave's clock frequency to 60 MHz at most. Four modes of SPI transfer format are supported. Only SDR reads and writes are supported.

  - In single-/two-/four-/eight-line half-duplex communication mode, the host's clock frequency is configurable to 80 MHz at most for SDR reads/writes and 40 MHz for DDR reads/writes. Four modes of SPI transfer format are supported.

  - In single-/two-/four-line half-duplex communication mode, the slave's clock frequency is configurable to 60 MHz at most. Only SDR reads and writes are supported. Four modes of SPI transfer format are supported.

- **SPI3 General-purpose SPI (GP-SPI) mode**

  SPI3 can operate in master and slave modes, in two-line full-duplex and single-line, two-line and four-line half-duplex communication modes. Only SDR reads and writes are supported. The host's clock frequency is configurable. Data transmission is in multiples of bytes. The clock polarity (CPOL) and phase (CPHA) are also configurable. The SPI3 interface supports DMA.

  - In two-line full-duplex communication mode, the host's clock frequency is configurable to a maximum of 80 MHz, and the slave's clock frequency to a maximum of 60 MHz. Four modes of SPI transfer format are supported.
  - In single-line, two-line and four-line half-duplex communication mode, the host's clock frequency is configurable to a maximum of 80 MHz, and the slave's clock frequency to 60 MHz at most. Four modes of SPI transfer format are supported.

In most cases, the data port connection between ESP32-S3 and external flash is as follows:

Table 11: Connection Between ESP32-S3 and External Flash

	External Flash Data Port			
Chip Pin	**SPI Single-Line Mode**	**SPI Two-Line Mode**	**SPI Four-Line Mode**	**SPI Eight-Line Mode**
SPID (SPID)	DI	IO0	IO0	IO0
SPIQ (SPIQ)	DO	IO1	IO1	IO1
SPIWP (SPIWP)	WP#	—	IO2	IO2
SPIHD (SPIHD)	HOLD#	—	IO3	IO3
GPIO33	—	—	—	IO4
GPIO34	—	—	—	IO5
GPIO35	—	—	—	IO6
GPIO36	—	—	—	IO7
GPIO37	—	—	—	DQS

3.4.3 LCD Interface

ESP32-S3 supports 8-bit ~16-bit parallel RGB, I8080, and MOTO6800 interfaces. These interfaces operate at 40 MHz or lower, and support conversion among RGB565, YUV422, YUV420, and YUV411.

3.4.4 Camera Interface

ESP32-S3 supports an 8-bit ~16-bit DVP image sensor, with clock frequency of up to 40 MHz. The camera interface supports conversion among RGB565, YUV422, YUV420, and YUV411.

3.4.5 Universal Asynchronous Receiver Transmitter (UART)

ESP32-S3 has three UART interfaces, i.e., UART0, UART1, and UART2, which support IrDA and asynchronous communication (RS232 and RS485) at a speed of up to 5 Mbps. The UART controller provides hardware management of the CTS and RTS signals and software flow control (XON and XOFF). All of the interfaces can be accessed by the DMA controller or directly by the CPU.

3.4.6 I2C Interface

ESP32-S3 has two I2C bus interfaces which are used for I2C master mode or slave mode, depending on the user's configuration. The I2C interfaces support:

- Standard mode (100 kbit/s)
- Fast mode (400 kbit/s)
- Up to 800 kbit/s (constrained by SCL and SDA pull-up strength)
- 7-bit and 10-bit addressing mode
- Double addressing mode (slave addressing and slave register addressing)

The hardware provides a command abstraction layer to simplify the usage of the I2C peripheral.

3.4.7 I2S Interface

ESP32-S3 includes two standard I2S interfaces. They can operate in master mode or slave mode, in full-duplex mode or half-duplex communication mode, and can be configured to operate with an 8-bit, 16-bit, 24-bit, or 32-bit resolution as an input or output channel. BCK clock frequency, from 10 kHz up to 40 MHz, is supported.

The I2S interface has a dedicated DMA controller. It supports TDM PCM, TDM MSB alignment, TDM LSB alignment, TDM Phillips, and PDM interface.

3.4.8 Remote Control Peripheral

The Remote Control Peripheral (RMT) supports four channels of infrared remote transmission and four channels of infrared remote reception. By controlling pulse waveform through software, it supports various infrared and other single wire protocols. All eight channels share a 384 × 32-bit memory block to store transmit or receive waveforms.

3.4.9 Pulse Counter

The pulse counter captures pulse and counts pulse edges through multiple modes. It has four channels, each of which captures four signals at a time. The four input signals include two pulse signals and two control signals.

3.4.10 LED PWM Controller

The LED PWM controller can generate independent digital waveforms on eight channels. The LED PWM controller:

- Can generate a digital waveform with configurable periods and duty cycle. The duty cycle resolution can be up to 14 bits within a 1 ms period.
- Has multiple clock sources, including APB clock and external main crystal clock.
- Can operate when the CPU is in Light-sleep mode.
- Supports gradual increase or decrease of duty cycle, which is useful for the LED RGB color-fading generator.

3.4.11 USB 1.1 OTG

ESP32-S3 features a full-speed USB OTG interface along with an integrated transceiver. The USB OTG interface complies with the USB 1.1 specification. It has the following features:

- Software-configurable endpoint settings and suspend/resume
- Dynamic FIFO size
- Session request protocol (SRP) and host negotiation protocol (HNP)
- Supports the full-speed USB PHY integrated in the chip or external USB PHY (but cannot use the same USB PHY together with the USB Serial/JTAG controller)

3.4.12 USB Serial/JTAG Controller

ESP32-S3 integrates a USB Serial/JTAG controller that:

- Complies with the full-speed USB 2.0 specification, with data rate up to 12 Mbit/s (Note that high-speed mode at 480 Mbit/s is not supported)
- Contains CDC-ACM virtual serial port and JTAG adapter functionality
- Supports programming SiP flash and external flash
- Supports CPU debugging with compact JTAG instructions
- Supports the full-speed USB PHY integrated in the chip or external USB PHY (but cannot use the same USB PHY together with USB 1.1 OTG)

3.4.13 Motor Control PWM (MCPWM)

ESP32-S3 integrates two MCPWM that can be used to drive digital motors and smart light. This controller includes PWM timers, PWM operators, and a dedicated capture submodule. PWM timers can be synchronized or work independently. Each PWM operator generates a waveform for one PWM channel. The dedicated capture submodule can accurately capture external timing events.

3.4.14 SD/MMC Host Controller

ESP32-S3 has an SD/MMC Host Controller with the following features:

- Secure Digital (SD) memory version 3.0 and version 3.01
- Secure Digital I/O (SDIO) version 3.0
- Consumer Electronics Advanced Transport Architecture (CE-ATA) version 1.1
- Multimedia Cards (MMC version 4.41, eMMC version 4.5 and version 4.51)

The controller allows up to 80 MHz clock output in 1-bit, 4-bit or 8-bit data bus mode. In 4-bit mode, ESP32-S3 supports two SD/SDIO/MMC 4.41 cards, and one SD card operating at 1.8 V.

3.4.15 GDMA Controller

ESP32-S3 has a general-purpose DMA controller (GDMA) with five independent channels for transmitting and another five independent channels for receiving. These ten channels are shared by peripherals that have DMA feature, and support dynamic priority.

The DMA controller controls data transfer using linked lists. It allows peripheral-to-memory and memory-to-memory data transfer at a high speed. All channels can access internal and external RAM.

The ten peripherals on ESP32-S3 with DMA feature are SPI2, SPI3, UHCI0, I2S0, I2S1, LCD/CAM, AES, SHA, ADC, and RMT.

3.4.16 TWAI® Controller

ESP32-S3 has a TWAI® controller with the following features:

- Compatible with ISO 11898-1 protocol (CAN Specification 2.0)
- Standard frame format (11-bit ID) and extended frame format (29-bit ID)
- Bit rates from 1 Kbit/s to 1 Mbit/s
- Multiple modes of operation: Normal, Listen Only, and Self-Test (no acknowledgment required)
- 64-byte receive FIFO
- Acceptance filter (single and dual filter modes)
- Error detection and handling: error counters, configurable error interrupt threshold, error code capture, arbitration lost capture

3.5 Radio and Wi-Fi

The ESP32-S3 radio consists of the following blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- Bias and regulators
- Balun and transmit-receive switch
- Clock generator

3.5.1 2.4 GHz Receiver

The 2.4 GHz receiver demodulates the 2.4 GHz RF signal to quadrature baseband signals and converts them to the digital domain with two high-resolution, high-speed ADCs. To adapt to varying signal channel conditions, ESP32-S3 integrates RF filters, Automatic Gain Control (AGC), DC offset cancelation circuits, and baseband filters.

3.5.2 2.4 GHz Transmitter

The 2.4 GHz transmitter modulates the quadrature baseband signals to the 2.4 GHz RF signal, and drives the antenna with a high-powered CMOS power amplifier. The use of digital calibration further improves the linearity of the power amplifier.

To compensate for receiver imperfections, additional calibration methods are built into the chip, including:

- Carrier leakage compensation
- I/Q amplitude/phase matching
- Baseband nonlinearities suppression
- RF nonlinearities suppression
- Antenna matching

These built-in calibration routines reduce the cost and time to the market for your product, and eliminate the need for specialized testing equipment.

3.5.3 Clock Generator

The clock generator produces quadrature clock signals of 2.4 GHz for both the receiver and the transmitter. All components of the clock generator are integrated into the chip, including inductors, varactors, filters, regulators, and dividers.

The clock generator has built-in calibration and self-test circuits. Quadrature clock phases and phase noise are optimized on chip with patented calibration algorithms which ensure the best performance of the receiver and the transmitter.

3.5.4 Wi-Fi Radio and Baseband

The ESP32-S3 Wi-Fi radio and baseband support the following features:

- 802.11b/g/n
- 802.11n MCS0-7 that supports 20 MHz and 40 MHz bandwidth
- 802.11n MCS32
- 802.11n 0.4 μs guard-interval
- Data rate up to 150 Mbps
- RX STBC (single spatial stream)
- Adjustable transmitting power
- Antenna diversity;
  ESP32-S3 supports antenna diversity with an external RF switch. This switch is controlled by one or more GPIOs, and used to select the best antenna to minimize the effects of channel imperfections.

3.5.5 Wi-Fi MAC

ESP32-S3 implements the full 802.11 b/g/n Wi-Fi MAC protocol. It supports the Basic Service Set (BSS) STA and SoftAP operations under the Distributed Control Function (DCF). Power management is handled automatically with minimal host interaction to minimize the active duty period.

The ESP32-S3 Wi-Fi MAC applies the following low-level protocol functions automatically:

- 4 × virtual Wi-Fi interfaces
- Simultaneous Infrastructure BSS Station mode, SoftAP mode, and Station + SoftAP mode
- RTS protection, CTS protection, Immediate Block ACK
- Fragmentation and defragmentation
- TX/RX A-MPDU, TX/RX A-MSDU
- TXOP
- WMM
- GCMP, CCMP, TKIP, WAPI, WEP, and BIP
- Automatic beacon monitoring (hardware TSF)
- 802.11mc FTM

3.5.6 Networking Features

Users are provided with libraries for TCP/IP networking, ESP-WIFI-MESH networking, and other networking protocols over Wi-Fi. TLS 1.2 support is also provided.

3.6 Bluetooth LE

ESP32-S3 includes a Bluetooth Low Energy subsystem that integrates a hardware link layer controller, an RF/modem block and a feature-rich software protocol stack. It supports the core features of Bluetooth 5 and Bluetooth mesh.

3.6.1 Bluetooth LE Radio and PHY

Bluetooth Low Energy radio and PHY in ESP32-S3 support:

- 1 Mbps PHY
- 2 Mbps PHY for high transmission speed and high data throughput
- Coded PHY for high RX sensitivity and long range (125 Kbps and 500 Kbps)
- Class 1 transmit power without external PA
- Listen before talk (LBT), implemented in hardware
- Antenna diversity with an external RF switch. This switch is controlled by one or more GPIOs, and used to select the best antenna to minimize the effects of channel imperfections.

3.6.2 Bluetooth LE Link Layer Controller

Bluetooth Low Energy Link Layer Controller in ESP32-S3 supports:

- LE advertising extensions, to enhance broadcasting capacity and broadcast more intelligent data
- Multiple advertisement sets
- Simultaneous advertising and scanning
- Multiple connections in simultaneous central and peripheral roles
- Adaptive frequency hopping and channel assessment
- LE channel selection algorithm #2
- Connection parameter update
- High duty cycle non-connectable advertising
- LE privacy 1.2
- LE data packet length extension
- Link layer extended scanner filter policies
- Low duty cycle directed advertising
- Link layer encryption
- LE Ping

3.7 RTC and Low-Power Management

3.7.1 Power Management Unit (PMU)

With the use of advanced power-management technologies, ESP32-S3 can switch between different power modes.

- **Active mode**: CPU and chip radio are powered on. The chip can receive, transmit, or listen.
- **Modem-sleep mode**: The CPU is operational and the clock speed can be reduced. The wireless baseband and radio are disabled, but wireless connection can remain active.
- **Light-sleep mode**: The CPU is paused. The RTC peripherals, as well as the ULP coprocessor can be woken up periodically by the timer. Any wake-up events (MAC, host, RTC timer, or external interrupts) will wake up the chip. Wireless connection can remain active. Users can optionally decide what peripherals to shut down/keep on (refer to Figure 1), for power-saving purpose.
- **Deep-sleep mode**: CPU and most peripherals are powered down. Only the RTC memory and RTC peripherals are powered on. Wi-Fi connection data are stored in the RTC memory. The ULP coprocessor is functional.
- **Hibernation mode**: The internal fast RC oscillator and ULP co-processor are disabled. Only one RTC timer on the slow clock is active. The RTC GPIO function is disabled and can only wake up the chip from the Hibernation mode. The RTC timer is also responsible for waking up the chip.

For power consumption in different power modes, please refer to Table 19.

3.7.2 Ultra-Low-Power Coprocessor

The ULP coprocessor is designed as a simplified, low-power replacement of CPU in sleep modes. It can be also used to supplement the functions of the CPU in normal working mode. The ULP coprocessor and RTC memory remain powered on during the Deep-sleep mode. Hence, the developer can store a program for the ULP coprocessor in the RTC slow memory to access RTC GPIO, RTC peripheral devices, RTC timers and internal sensors in Deep-sleep mode.

ESP32-S3 has two ULP coprocessors, one based on RISC-V instruction set architecture (ULP-RISC-V) and the other on finite state machine (ULP-FSM). The clock of the coprocessors is the internal fast RC oscillator.

ULP-RISC-V has the following features:

- Support for RV32IMC instruction set
- Thirty-two 32-bit general-purpose registers
- 32-bit multiplier and divider
- Support for interrupts
- Booted by the CPU, its dedicated timer, or RTC GPIO

ULP-FSM has the following features:

- Support for common instructions including arithmetic, jump, and program control instructions
- Support for on-board sensor measurement instructions
- Booted by the CPU, its dedicated timer, or RTC GPIO

Note that these two coprocessors cannot work simultaneously.

3.8 Timers and Watchdogs

3.8.1 General Purpose Timers

ESP32-S3 is embedded with four 54-bit general-purpose timers, which are based on 16-bit prescalers and 54-bit auto-reload-capable up/down-timers.

The timers' features are summarized as follows:

- A 16-bit clock prescaler, from 2 to 65536
- A 54-bit time-base counter programmable to be incrementing or decrementing
- Able to read real-time value of the time-base counter
- Halting and resuming the time-base counter
- Programmable alarm generation
- Timer value reload (Auto-reload at alarm or software-controlled instant reload)
- Level interrupt generation

3.8.2 System Timer

ESP32-S3 integrates a 52-bit system timer, which has two 52-bit counters and three comparators. The system timer has the following features:

- Counters with a clock frequency of 16 MHz
- Three types of independent interrupts generated according to alarm value
- Two alarm modes: target mode and period mode
- 52-bit target alarm value and 26-bit periodic alarm value
- Read sleep time from RTC timer when the chip is awaken from Deep-sleep or Light-sleep mode
- Counters can be stalled if the CPU is stalled or in OCD mode

3.8.3 Watchdog Timers

The ESP32-S3 contains three watchdog timers: one in each of the two timer groups (called Main System Watchdog Timers, or MWDT) and one in the RTC Module (called the RTC Watchdog Timer, or RWDT).

During the flash boot process, RWDT and the first MWDT are enabled automatically in order to detect and recover from booting errors.

Watchdog timers have the following features:

- Four stages, each with a programmable timeout value. Each stage can be configured, enabled and disabled separately
- Interrupt, CPU reset, or core reset for MWDT upon expiry of each stage; interrupt, CPU reset, core reset, or system reset for RWDT upon expiry of each stage
- 32-bit expiry counter
- Write protection, to prevent RWDT and MWDT configuration from being altered inadvertently
- Flash boot protection
  If the boot process from an SPI flash does not complete within a predetermined period of time, the watchdog will reboot the entire main system.

3.9 Cryptographic Hardware Accelerators

ESP32-S3 is equipped with hardware accelerators of general algorithms, such as AES (FIPS PUB 197), ECB/CBC/OFB/CFB/CTR (NIST SP 800-38A), SHA (FIPS PUB 180-4), RSA, and ECC. The chip also supports independent arithmetic, such as Big Integer Multiplication and Big Integer Modular Multiplication. The maximum operation length for RSA and Big Integer Modular Multiplication is 4096 bits. The maximum factor length for Big Integer Multiplication is 2048 bits.

3.10 Physical Security Features

- Transparent external flash and RAM encryption (AES-XTS) with software inaccessible key prevents unauthorized readout of user application code or data.
- Secure Boot feature uses a hardware root of trust to ensure only signed firmware (with RSA-PSS signature) can be booted.
- HMAC module uses a software inaccessible MAC key to generate MAC signatures for identity verification, as well as other uses.
- Digital Signature module uses a software inaccessible secure key to generate RSA signatures for identity verification.
- World controller provides two running environment for software. All hardware and software resources are sorted to two groups, and placed in either secure or general world. The secure world cannot be accessed by hardware in the general world, thus establishing a security boundary.

3.11 Peripheral Pin Configurations

Table 12: Peripheral Pin Configurations

Interface	Signal	Pin	Function
ADC	ADC1_CH0	GPIO1	Two 12-bit SAR ADCs
	ADC1_CH1	GPIO2	
	ADC1_CH2	GPIO3	
	ADC1_CH3	GPIO4	
	ADC1_CH4	GPIO5	
	ADC1_CH5	GPIO6	
	ADC1_CH6	GPIO7	
	ADC1_CH7	GPIO8	
	ADC1_CH8	GPIO9	
	ADC1_CH9	GPIO10	
	ADC2_CH0	GPIO11	
	ADC2_CH1	GPIO12	
	ADC2_CH2	GPIO13	
	ADC2_CH3	GPIO14	
	ADC2_CH4	XTAL_32K_P	
	ADC2_CH5	XTAL_32K_N	
	ADC2_CH6	GPIO17	
	ADC2_CH7	GPIO18	
	ADC2_CH8	GPIO19	

Interface	Signal	Pin	Function
	ADC2_CH9	GPIO20	
Touch sensor	TOUCH1	GPIO1	Capacitive touch sensors
	TOUCH2	GPIO2	
	TOUCH3	GPIO3	
	TOUCH4	GPIO4	
	TOUCH5	GPIO5	
	TOUCH6	GPIO6	
	TOUCH7	GPIO7	
	TOUCH8	GPIO8	
	TOUCH9	GPIO9	
	TOUCH10	GPIO10	
	TOUCH11	GPIO11	
	TOUCH12	GPIO12	
	TOUCH13	GPIO13	
	TOUCH14	GPIO14	
JTAG	MTDI	MTDI	JTAG for software debugging
	MTCK	MTCK	
	MTMS	MTMS	
	MTDO	MTDO	
UART	U0RXD_in	Any GPIO pins	Three UART devices with hardware flow-control and DMA
	U0CTS_in		
	U0DSR_in		
	U0TXD_out		
	U0RTS_out		
	U0DTR_out		
	U1RXD_in		
	U1CTS_in		
	U1DSR_in		
	U1TXD_out		
	U1RTS_out		
	U1DTR_out		
	U2RXD_in		
	U2CTS_in		
	U2DSR_in		
	U2TXD_out		
	U2RTS_out		
	U2DTR_out		
I2C	I2CEXT0_SCL_in/_out	Any GPIO pins	Two I2C devices in slave or master mode
	I2CEXT0_SDA_in/_out		
	I2CEXT1_SCL_in/_out		
	I2CEXT1_SDA_in/_out		
LED PWM	LEDC_LS_SIG_out0~7	Any GPIO pins	Eight independent channels.

Interface	Signal	Pin	Function
I2S	I2S0O_BCK_in I2S0_MCLK_in I2S0O_WS_in I2S0I_SD_in I2S0I_SD1_in I2S0I_SD2_in I2S0I_SD3_in I2S0I_BCK_in I2S0I_WS_in I2S1O_BCK_in I2S1_MCLK_in I2S1O_WS_in I2S1I_SD_in I2S1I_BCK_in I2S1I_WS_in I2S0O_BCK_out I2S0_MCLK_out I2S0O_WS_out I2S0O_SD_out I2S0O_SD1_out I2S0I_BCK_out I2S0I_WS_out I2S1O_BCK_out I2S1_MCLK_out I2S1O_WS_out I2S1O_SD_out I2S1I_BCK_out I2S1I_WS_out	Any GPIO pins	Stereo input and output from/to the audio codec
LCD_CAMERA	LCD_PCLK LCD_DC LCD_V_SYNC LCD_H_SYNC LCD_H_ENABLE LCD_DATA_out0~15 LCD_CS CAM_CLK CAM_V_SYNC CAM_H_SYNC CAM_H_ENABLE CAM_PCLK CAM_DATA_in0~15	Any GPIO pins	8 ~16 data transmission to LCD interface and 8 ~16 data reception by camera interface
Remote Control Peripheral	RMT_SIG_in0~3 RMT_SIG_out0~3	Any GPIO pins	Four channels for an IR transceiver of various wave forms

Interface	Signal	Pin	Function
SPI0/1	SPICLK_out_mux	SPICLK	Support Standard SPI, Dual SPI, QSPI, QPI, OSPI, and OPI that allow connection to external flash and RAM.
	SPICS0_out	SPICS0	
	SPICS1_out	SPICS1	
	SPID_in/_out	SPID	
	SPIQ_in/_out	SPIQ	
	SPIWP_in/_out	SPIWP	
	SPIHD_in/_out	SPIHD	
	SPID4_in/_out	GPIO33	
	SPID5_in/_out	GPIO34	
	SPID6_in/_out	GPIO35	
	SPID7_in/_out	GPIO36	
	SPIDQS_in/_out	GPIO37	
SPI2	FSPICLK_in/_out_mux	Any GPIO pins	Support: • master mode of SPI, Dual SPI, Quad SPI,Octal SPI, QPI, and OPI, and slave mode of SPI, Dual SPI, Quad SPI, and QPI; • connection to external flash, RAM, and other SPI devices; • four modes of SPI transfer format; • configurable SPI frequency; • 64-byte FIFO or DMA buffer.
	FSPICS0_in/_out		
	FSPICS1~5_out		
	FSPID_in/_out		
	FSPIQ_in/_out		
	FSPIWP_in/_out		
	FSPIHD_in/_out		
	FSPIIO4~7_in/_out		
	FSPIDQS_out		
SPI3	SPI3_CLK_in/_out_mux	Any GPIO pins	Support: • master and slave modes of SPI, Dual SPI, Quad SPI, and QPI; • four modes of SPI transfer format; • configurable frequency; • 64-byte FIFO or DMA buffer.
	SPI3_CS0_in/_out		
	SPI3_CS1_out		
	SPI3_CS2_out		
	SPI3_D_in/_out		
	SPI3_Q_in/_out		
	SPI3_WP_in/_out		
	SPI3_HD_in/_out		
Pulse counter	PCNT_SIG_CH0_in0~3	Any GPIO pins	Capture pulse and count pulse edges in seven modes
	PCNT_SIG_CH1_in0~3		
	PCNT_CTRL_CH0_in0~3		
	PCNT_CTRL_CH1_in0~3		

Interface	Signal	Pin	Function
USB OTG	D-	GPIO19 (for internal PHY)	Full-speed USB OTG (USB OTG supports both high-speed on-chip PHY and external PHY)
	D+	GPIO20 (for internal PHY)	
	VP	MTMS (for external PHY)	
	VM	MTDI (for external PHY)	
	RCV	GPIO21 (for external PHY)	
	OEN	MTDO (for external PHY)	
	VPO	MTCK (for external PHY)	
	VMO	GPIO38 (for external PHY)	
USB Serial/JTAG controller	D-	GPIO19 (for internal PHY)	Flash programming and CPU debugging (USB Serial/JTAG controller supports both high-speed on-chip PHY and external PHY)
	D+	GPIO20 (for internal PHY)	
	VP	MTMS (for external PHY)	
	VM	MTDI (for external PHY)	
	OEN	MTDO (for external PHY)	
	VPO	MTCK (for external PHY)	
	VMO	GPIO38 (for external PHY)	
SD/MMC Host Controller	SDHOST_CCLK_out_1~2	Any GPIO pins	Secure Digital (SD) memory version version 3.01 supported
	SDHOST_RST_N_1~2		
	SDHOST_CCMD_OD_PULLUP_EN_N		
	SDIO_TOHOST_INT_out		
	SDHOST_CCMD_in/_out_1		
	SDHOST_CCMD_in/_out_2		
	SDHOST_CDATA_in/_out_10		
	SDHOST_CDATA_in/_out_11		
	SDHOST_CDATA_in/_out_12		
	SDHOST_CDATA_in/_out_13		
	SDHOST_CDATA_in/_out_14		
	SDHOST_CDATA_in/_out_15		
	SDHOST_CDATA_in/_out_16		
	SDHOST_CDATA_in/_out_17		
	SDHOST_CDATA_in/_out_20		
	SDHOST_CDATA_in/_out_21		
	SDHOST_CDATA_in/_out_22		
	SDHOST_CDATA_in/_out_23		
	SDHOST_CDATA_in/_out_24		
	SDHOST_CDATA_in/_out_25		
	SDHOST_CDATA_in/_out_26		
	SDHOST_CDATA_in/_out_27		
	SDHOST_DATA_STROBE_1~2		
	SDHOST_CARD_DETECT_N_1~2		
	SDHOST_CARD_WRITE_PRT_1~2		
	SDHOST_CARD_INT_N_1~2		

Interface	Signal	Pin	Function
MCPWM	PWM0_SYNC0~2_in	Any GPIO pins	Two MCPWM input and output pins. Signals include PWM differential output signals, fault input signals to be detected, input signals to be captured, and external clock synchronization signals
	PWM0_F0~2_in		
	PWM0_CAP0~2_in		
	PWM1_SYNC0~2_in		
	PWM1_F0~2_in		
	PWM1_CAP0~2_in		
	PWM0_out0a		
	PWM0_out0b		
	PWM0_out1a		
	PWM0_out1b		
	PWM0_out2a		
	PWM0_out2b		
	PWM1_out0a		
	PWM1_out0b		
	PWM1_out1a		
	PWM1_out1b		
	PWM1_out2a		
	PWM1_out2b		
TWAI® Controller	TWAI_RX	Any GPIO pins	Compatible with ISO 11898-1 protocol (CAN Specification 2.0). Data rate up to 1 Mbit/s
	TWAI_TX		
	TWAI_BUS_OFF_ON		
	TWAI_CLKOUT		

4. Electrical Characteristics

The values presented in this section are preliminary and may change with the final release of this datasheet.

4.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device.

Table 13: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_CPU, VDD_SPI	Voltage applied to power supply pins per power domain	–0.3	3.6	V
I_{output} *	Cumulative IO output current	—	1500	mA
T_{STORE}	Storage temperature	–40	150	°C

* The chip worked properly after a 24-hour test in ambient temperature at 25 °C, and the IOs in three domains (VDD3P3_RTC, VDD3P3_CPU, VDD_SPI) output high logic level to ground.

4.2 Recommended Operating Conditions

Table 14: Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
VDDA, VDD3P3 VDD3P3_RTC	Voltage applied to power supply pins per power domain		3.0	3.3	3.6	V
VDD_SPI (working as input power supply) [1]	—		1.8	3.3	3.6	V
VDD3P3_CPU [2]	Voltage applied to power supply pin		3.0	3.3	3.6	V
I_{VDD} [3]	Current delivered by external power supply		0.5	—	—	A
T_A	Ambient temperature	ESP32-S3	–40	—	105	°C
		ESP32-S3FN8			85	
		ESP32-S3R2			85	
		ESP32-S3R8			85	
		ESP32-S3R8V			85	

[1] For more information, please refer to Section 2.7 *Power Scheme*.

[2] When VDD_SPI is used to drive peripherals, VDD3P3_CPU should comply with the peripherals' specifications. For more information, please refer to Table 15.

[3] If you use a single power supply, the recommended output current is 500 mA or more.

4.3 VDD_SPI Output Characteristics

Table 15: VDD_SPI Output Characteristics

Symbol	Parameter	Typ	Unit
R_{SPI}	On-resistance in 3.3 V mode	7.5	Ω
I_{SPI}	Output current in 1.8 V mode	40	mA

In real-life applications, when VDD_SPI works in 3.3 V output mode, VDD3P3_CPU may be affected by R_{SPI}. For example, when VDD3P3_CPU is used to drive a 3.3 V flash, it should comply with the following specifications:

VDD3P3_CPU > VDD_flash_min + I_flash_max*R_{SPI}

Among which, VDD_flash_min is the minimum operating voltage of the flash, and I_flash_max the maximum current.

For more information, please refer to section 2.7 *Power Scheme*.

4.4 DC Characteristics (3.3 V, 25 °C)

Table 16: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL}	Low-level input voltage	–0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1]= 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD[1]= 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Internal weak pull-up resistor	—	45	—	kΩ
R_{PD}	Internal weak pull-down resistor	—	45	—	kΩ
V_{IH_nRST}	Chip reset release voltage (CHIP_PU voltage is within the specified range)	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL_nRST}	Chip reset voltage (CHIP_PU voltage is within the specified range)	–0.3	—	0.25 × VDD[1]	V

[1] VDD is the I/O voltage for a particular power domain of pins.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

4.5 ADC Characteristics

Table 17: ADC Characteristics

Symbol	Parameter	Min	Max	Unit
DNL (Differential nonlinearity) [1]	ADC connected to an external 100 nF capacitor; DC signal input;	–4	4	LSB

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Table 17 – cont'd from previous page

Symbol	Parameter	Min	Max	Unit
INL (Integral nonlinearity)	Ambient temperature at 25 °C; Wi-Fi off	–8	8	LSB
Sampling rate	—	—	100	kSPS [2]
Effective Range	ATTEN0	0	950	mV
	ATTEN1	0	1250	mV
	ATTEN2	0	1750	mV
	ATTEN3	0	3100	mV

[1] To get better DNL results, you can sample multiple times and apply a filter, or calculate the average value.

[2] kSPS means kilo samples-per-second.

4.6 Current Consumption

The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on a 100% duty cycle.

Table 18: Wi-Fi Current Consumption Depending on RF Modes

Work Mode [1]	Description		Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, @21 dBm	340
		802.11g, 54 Mbps, @19 dBm	291
		802.11n, HT20, MCS7, @18.5 dBm	283
		802.11n, HT40, MCS7, @18.5 dBm	290
	RX	802.11b/g/n, HT20	95
		802.11n, HT40	97

[1] The CPU work mode: Single core runs 32-bit data access instructions at 80 MHz, the other core is in idle state.

Note that data in Table 19 only applies to ESP32-S3, with no SiP flash or SiP PSRAM co-packaged inside.

Table 19: Current Consumption Depending on Work Modes (except Modem-sleep)

Work mode	Description	Typ	Unit
Light-sleep	—	240	µA
Deep-sleep	RTC memory and RTC peripherals are powered on.	8	µA
Hibernation	RTC memory is powered on. RTC peripherals are powered off.	7	µA
Power off	CHIP_PU is set to low level. The chip is powered off.	1	µA

Table 20: Current Consumption in Modem-sleep Mode

Work mode	Frequency (MHz)	Description	Typ (mA)
Modem-sleep	40	WAITI (Dual core in idle state)	13.2
		Single core running 32-bit data access instructions, the other core in idle state	16.2
		Dual core running 32-bit data access instructions	18.7
		Single core running 128-bit data access instructions, the other core in idle state	19.9
		Dual core running 128-bit data access instructions	23.0
	80	WAITI	22.0
		Single core running 32-bit data access instructions, the other core in idle state	28.4
		Dual core running 32-bit data access instructions	33.1
		Single core running 128-bit data access instructions, the other core in idle state	35.1
		Dual core running 128-bit data access instructions	41.8
	160	WAITI	27.6
		Single core running 32-bit data access instructions, the other core in idle state	39.9
		Dual core running 32-bit data access instructions	49.6
		Single core running 128-bit data access instructions, the other core in idle state	54.4
		Dual core running 128-bit data access instructions	66.7
	240	WAITI	32.9
		Single core running 32-bit data access instructions, the other core in idle state	51.2
		Dual core running 32-bit data access instructions	66.2
		Single core running 128-bit data access instructions, the other core in idle state	72.4
		Dual core running 128-bit data access instructions	91.7

4.7 Reliability

Table 21: Reliability Qualifications

Test Item	Test Conditions	Test Standard
ESD (Electro-Static Discharge Sensitivity)	HBM (Human Body Mode)[1]± 2000 V	JESD22-A114
	CDM (Charge Device Mode)[2]± 1000 V	JESD22-C101F
Latch up	Current trigger ± 200 mA	JESD78
	Voltage trigger 1.5 × VDD_{max}	

[1] JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

[2] JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

4.8 Wi-Fi Radio

Table 22: Wi-Fi Frequency

Parameter	Min (MHz)	Typ (MHz)	Max (MHz)
Center frequency of operating channel	2412	—	2484

4.8.1 Wi-Fi RF Transmitter (TX) Specifications

Table 23: TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	21.0	—
802.11b, 11 Mbps	—	21.0	—
802.11g, 6 Mbps	—	21.0	—
802.11g, 54 Mbps	—	19.0	—
802.11n, HT20, MSC0	—	20.0	—
802.11n, HT20, MSC7	—	18.5	—
802.11n, HT40, MSC0	—	20.0	—
802.11n, HT40, MSC7	—	18.5	—

Table 24: TX EVM Test

Rate	Min (dB)	Typ (dB)	SL[1] (dB)
802.11b, 1 Mbps, @21 dBm	—	–24.5	–10
802.11b, 11 Mbps, @21 dBm	—	–24.5	–10
802.11g, 6 Mbps, @21 dBm	—	–21.5	–5
802.11g, 54 Mbps, @19 dBm	—	–27.5	–25
802.11n, HT20, MSC0, @20 dBm	—	–22.0	–5
802.11n, HT20, MSC7, @18.5 dBm	—	–29.5	–27
802.11n, HT40, MSC0, @20 dBm	—	–22.0	–5
802.11n, HT40, MSC7, @18.5 dBm	—	–29.0	–27

[1] SL stands for standard limit value.

4.8.2 Wi-Fi RF Receiver (RX) Specifications

Table 25: RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	–98.4	—
802.11b, 2 Mbps	—	–95.4	—
802.11b, 5.5 Mbps	—	–93.0	—

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Table 25 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 11 Mbps	—	–88.6	—
802.11g, 6 Mbps	—	–93.2	—
802.11g, 9 Mbps	—	–91.8	—
802.11g, 12 Mbps	—	–91.2	—
802.11g, 18 Mbps	—	–88.6	—
802.11g, 24 Mbps	—	–86.0	—
802.11g, 36 Mbps	—	–82.4	—
802.11g, 48 Mbps	—	–78.2	—
802.11g, 54 Mbps	—	–76.5	—
802.11n, HT20, MSC0	—	–92.6	—
802.11n, HT20, MSC1	—	–91.0	—
802.11n, HT20, MSC2	—	–88.2	—
802.11n, HT20, MSC3	—	–85.0	—
802.11n, HT20, MSC4	—	–81.8	—
802.11n, HT20, MSC5	—	–77.4	—
802.11n, HT20, MSC6	—	–75.8	—
802.11n, HT20, MSC7	—	–74.2	—
802.11n, HT40, MSC0	—	–90.0	—
802.11n, HT40, MSC1	—	–88.0	—
802.11n, HT40, MSC2	—	–85.2	—
802.11n, HT40, MSC3	—	–82.0	—
802.11n, HT40, MSC4	—	–79.0	—
802.11n, HT40, MSC5	—	–74.4	—
802.11n, HT40, MSC6	—	–72.8	—
802.11n, HT40, MSC7	—	–71.4	—

Table 26: Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	5	—
802.11b, 11 Mbps	—	5	—
802.11g, 6 Mbps	—	5	—
802.11g, 54 Mbps	—	0	—
802.11n, HT20, MSC0	—	5	—
802.11n, HT20, MSC7	—	0	—
802.11n, HT40, MSC0	—	5	—
802.11n, HT40, MSC7	—	0	—

Table 27: RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps	—	35	—
802.11b, 11 Mbps	—	35	—
802.11g, 6 Mbps	—	31	—
802.11g, 54 Mbps	—	20	—
802.11n, HT20, MSC0	—	31	—
802.11n, HT20, MSC7	—	16	—
802.11n, HT40, MSC0	—	25	—
802.11n, HT40, MSC7	—	11	—

4.9 Bluetooth LE Radio

Table 28: Bluetooth LE Frequency

Parameter	Min (MHz)	Typ (MHz)	Max (MHz)
Center frequency of operating channel	2402	—	2480

4.9.1 Bluetooth LE RF Transmitter (TX) Specifications

Table 29: Transmitter Characteristics - Bluetooth LE 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	–25.00	0	20.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\lvert f_n \rvert_{n=0,\ 1,\ 2,\ ..k}$	—	2.50	—	kHz
	Max $\lvert f_0 - f_n \rvert$	—	2.00	—	kHz
	Max $\lvert f_n - f_{n-5} \rvert$	—	1.39	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	0.80	—	kHz
Modulation characteristics	$\Delta\ f1_{\text{avg}}$	—	249.00	—	kHz
	Min $\Delta\ f2_{\text{max}}$ (for at least 99.9% of all $\Delta\ f2_{\text{max}}$)	—	198.00	—	kHz
	$\Delta\ f2_{\text{avg}}/\Delta\ f1_{\text{avg}}$	—	0.86	—	—
In-band spurious emissions	±2 MHz offset	—	–37.00	—	dBm
	±3 MHz offset	—	–42.00	—	dBm
	>±3 MHz offset	—	–44.00	—	dBm

Table 30: Transmitter Characteristics - Bluetooth LE 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	–25.00	0	20.00	dBm
	Gain control step	—	3.00	—	dB

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Table 30 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\ 1,\ 2,\ ..k}$	—	2.50	—	kHz
	Max $\|f_0 - f_n\|$	—	1.90	—	kHz
	Max $\|f_n - f_{n-5}\|$	—	1.40	—	kHz
	$\|f_1 - f_0\|$	—	1.10	—	kHz
Modulation characteristics	$\Delta\ f1_{\text{avg}}$	—	499.00	—	kHz
	Min $\Delta\ f2_{\text{max}}$ (for at least 99.9% of all $\Delta\ f2_{\text{max}}$)	—	416.00	—	kHz
	$\Delta\ f2_{\text{avg}}/\Delta\ f1_{\text{avg}}$	—	0.89	—	—
In-band spurious emissions	±4 MHz offset	—	–43.80	—	dBm
	±5 MHz offset	—	–45.80	—	dBm
	>±5 MHz offset	—	–47.00	—	dBm

Table 31: Transmitter Characteristics - Bluetooth LE 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	–25.00	0	20.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\ 1,\ 2,\ ..k}$	—	0.80	—	kHz
	Max $\|f_0 - f_n\|$	—	0.98	—	kHz
	$\|f_n - f_{n-3}\|$	—	0.30	—	kHz
	$\|f_0 - f_3\|$	—	1.00	—	kHz
Modulation characteristics	$\Delta\ f1_{\text{avg}}$	—	248.00	—	kHz
	Min $\Delta\ f1_{\text{max}}$ (for at least 99.9% of all$\Delta\ f1_{\text{max}}$)	—	222.00	—	kHz
In-band spurious emissions	±2 MHz offset	—	–37.00	—	dBm
	±3 MHz offset	—	–42.00	—	dBm
	>±3 MHz offset	—	–44.00	—	dBm

Table 32: Transmitter Characteristics - Bluetooth LE 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	–25.00	0	20.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\|f_n\|_{n=0,\ 1,\ 2,\ ..k}$	—	0.70	—	kHz
	Max $\|f_0 - f_n\|$	—	0.90	—	kHz
	$\|f_n - f_{n-3}\|$	—	0.85	—	kHz
	$\|f_0 - f_3\|$	—	0.34	—	kHz
Modulation characteristics	$\Delta\ f2_{\text{avg}}$	—	213.00	—	kHz
	Min $\Delta\ f2_{\text{max}}$ (for at least 99.9% of all $\Delta\ f2_{\text{max}}$)	—	196.00	—	kHz
In-band spurious emissions	±2 MHz offset	—	–37.00	—	dBm
	±3 MHz offset	—	–42.00	—	dBm
	>±3 MHz offset	—	–44.00	—	dBm

4.9.2 Bluetooth LE RF Receiver (RX) Specifications

Table 33: Receiver Characteristics - Bluetooth LE 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–97.5	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	9	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–3	—	dB
	F = F0 – 1 MHz	—	–3	—	dB
	F = F0 + 2 MHz	—	–28	—	dB
	F = F0 – 2 MHz	—	–30	—	dB
	F = F0 + 3 MHz	—	–31	—	dB
	F = F0 – 3 MHz	—	–33	—	dB
	F > F0 + 3 MHz	—	–32	—	dB
	F > F0 – 3 MHz	—	–36	—	dB
Image frequency	—	—	–32	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–39	—	dB
	F = F_{image} – 1 MHz	—	–31	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	–9	—	dBm
	2003 MHz ~ 2399 MHz	—	–19	—	dBm
	2484 MHz ~ 2997 MHz	—	–16	—	dBm
	3000 MHz ~ 12.75 GHz	—	–5	—	dBm
Intermodulation	—	—	–31	—	dBm

Table 34: Receiver Characteristics - Bluetooth LE 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–93.5	—	dBm
Maximum received signal @30.8% PER	—	—	3	—	dBm
Co-channel C/I	F = F0 MHz	—	10	—	dB
Adjacent channel selectivity C/I	F = F0 + 2 MHz	—	–8	—	dB
	F = F0 – 2 MHz	—	–5	—	dB
	F = F0 + 4 MHz	—	–31	—	dB
	F = F0 – 4 MHz	—	–33	—	dB
	F = F0 + 6 MHz	—	–37	—	dB
	F = F0 – 6 MHz	—	–37	—	dB
	F > F0 + 6 MHz	—	–40	—	dB
	F > F0 – 6 MHz	—	–40	—	dB
Image frequency	—	—	–31	—	dB
Adjacent channel to image frequency	F = F_{image} + 2 MHz	—	–37	—	dB
	F = F_{image} – 2 MHz	—	–8	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	–16	—	dBm
	2003 MHz ~ 2399 MHz	—	–20	—	dBm
	2484 MHz ~ 2997 MHz	—	–16	—	dBm

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Table 34 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	3000 MHz ~ 12.75 GHz	—	–16	—	dBm
Intermodulation	—	—	–30	—	dBm

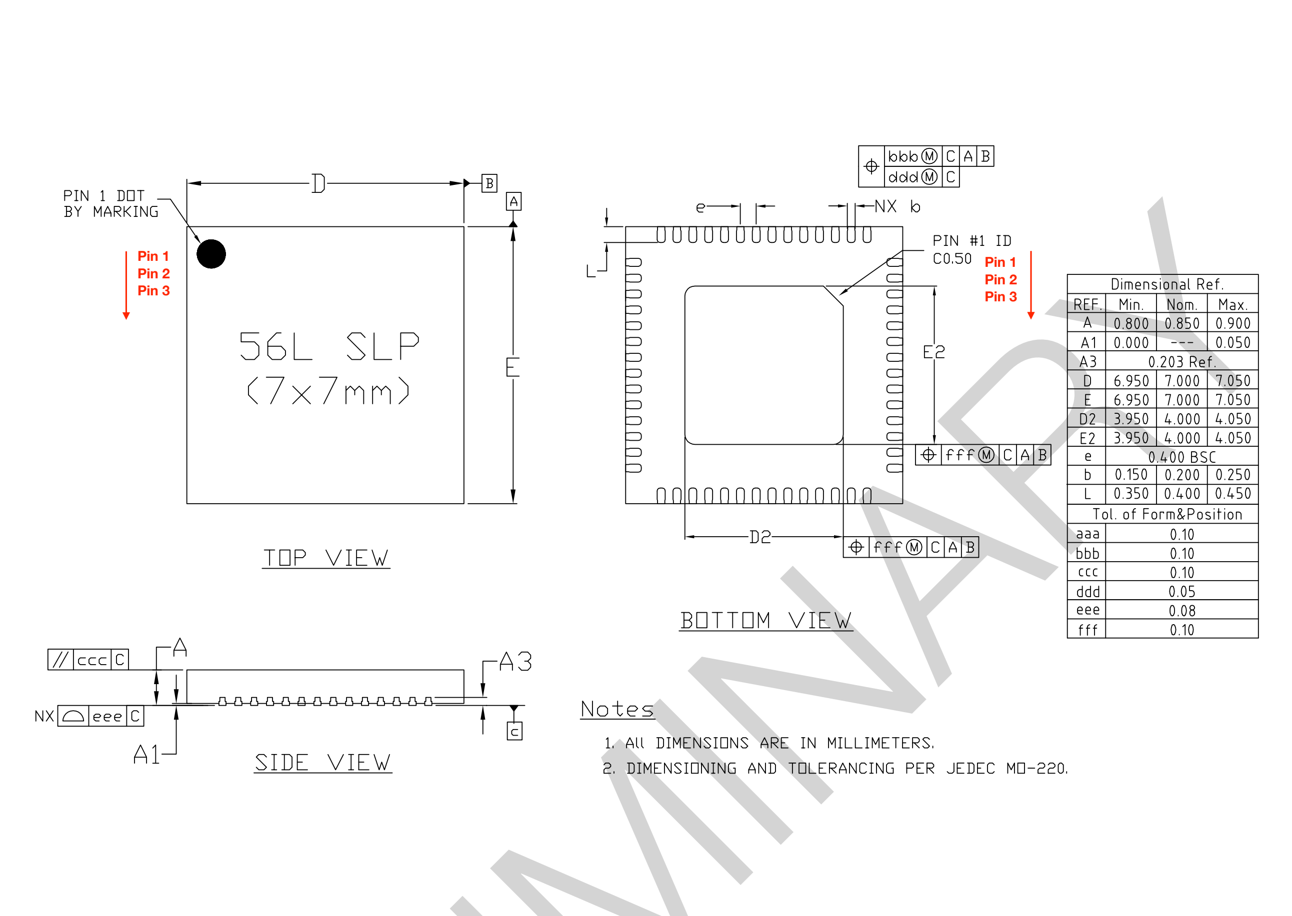
Table 35: Receiver Characteristics - Bluetooth LE 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–104.5	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	6	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–6	—	dB
	F = F0 – 1 MHz	—	–5	—	dB
	F = F0 + 2 MHz	—	–32	—	dB
	F = F0 – 2 MHz	—	–39	—	dB
	F = F0 + 3 MHz	—	–35	—	dB
	F = F0 – 3 MHz	—	–45	—	dB
	F > F0 + 3 MHz	—	–35	—	dB
	F > F0 – 3 MHz	—	–48	—	dB
Image frequency	—	—	–35	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–49	—	dB
	F = F_{image} – 1 MHz	—	–32	—	dB

Table 36: Receiver Characteristics - Bluetooth LE 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–101	—	dBm
Maximum received signal @30.8% PER	—	—	8	—	dBm
Co-channel C/I	F = F0 MHz	—	4	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–5	—	dB
	F = F0 – 1 MHz	—	–5	—	dB
	F = F0 + 2 MHz	—	–28	—	dB
	F = F0 – 2 MHz	—	–36	—	dB
	F = F0 + 3 MHz	—	–36	—	dB
	F = F0 – 3 MHz	—	–38	—	dB
	F > F0 + 3 MHz	—	–37	—	dB
	F > F0 – 3 MHz	—	–41	—	dB
Image frequency	—	—	–37	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–44	—	dB
	F = F_{image} – 1 MHz	—	–28	—	dB

5. Package Information



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	0.000	---	0.050
A3	0.203 Ref.		
D	6.950	7.000	7.050
E	6.950	7.000	7.050
D2	3.950	4.000	4.050
E2	3.950	4.000	4.050
e	0.400 BSC		
b	0.150	0.200	0.250
L	0.350	0.400	0.450
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Figure 8: QFN56 (7×7 mm) Package

Note:

- The pins of the chip are numbered in an anti-clockwise direction from Pin 1 in the top view.
- For information about tape, reel, and product marking, please refer to *Espressif Chip-Packing Information*.

6. Related Documentation and Resources

Related Documentation

- ESP32-S3 Technical Reference Manual – Detailed information on how to use the ESP32-S3 memory and peripherals.
- ESP32-S3 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-S3 into your hardware product.
- *Certificates*
  http://espressif.com/en/support/documents/certificates
- *Documentation Updates and Update Notification Subscription*
  http://espressif.com/en/support/download/documents

Developer Zone

- *ESP-IDF* and other development frameworks on GitHub.
  http://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  http://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  http://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  http://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-S3 Series SoCs* – Browse through all ESP32-S3 SoCs.
  http://espressif.com/en/products/socs?id=ESP32-S3
- *ESP32-S3 Series Modules* – Browse through all ESP32-S3-based modules.
  http://espressif.com/en/products/modules?id=ESP32-S3
- *ESP32-S3 Series DevKits* – Browse through all ESP32-S3-based devkits.
  http://espressif.com/en/products/devkits?id=ESP32-S3
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  http://products.espressif.com/#/product-selector?language=en

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Revision History

Date	Version	Release Notes
2021-10-12	v0.6.1	Updated text description
2021-09-30	v0.6	• Updated to chip revision 1 by swapping pin 53 and pin 54 (XTAL_P and XTAL_N) • Updated Figure 1 • Added CoreMark score in section Features • Updated Section 2.8 • Added data for cumulative IO output current in Table 13 • Added data for Modem-sleep current consumption in Table 20 • Updated data in section 4.6, 4.8, and 4.9 • Updated wording throughout
2021-07-19	v0.5.1	• Added "for chip revision 0" on cover, in footer and watermark to indicate that the current and previous versions of this datasheet are for chip version 0 • Corrected a few typos
2021-07-09	v0.5	Preliminary version

PRELIMINARY

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