Analog Reinvented

SABRE9006A
*Premier*8-Channel Audio DAC
Datasheet

OVERVIEW

The Sabre Premier (SABRE9006A) High Performance Audio DAC is a 24-Bit, 8-channel audio DAC that brings professional, digital audio quality to the consumer home entertainment market. The SABRE9006A is a pin-compatible replacement for the ES9006 and offers significantly improved linearity versus the ES9006.

Using ESS' patented HyperStream® architecture and patented Time Domain Jitter Eliminator, the Sabre Premier Audio DAC delivers studio quality audio with 120dB DNR and –102dB THD+N to digital audio applications such as Blu-ray, SACD, DVD-Audio, DVD, CD, home theatre, set top boxes and digital TV.

The Sabre Premier's flexible input architecture accepts serial 16-24 bit serial PCM data to 192kHz sample rate, 16-24 bit SPDIF data up to 96kHz sampling rate, or DSD data supporting native SACD audio.

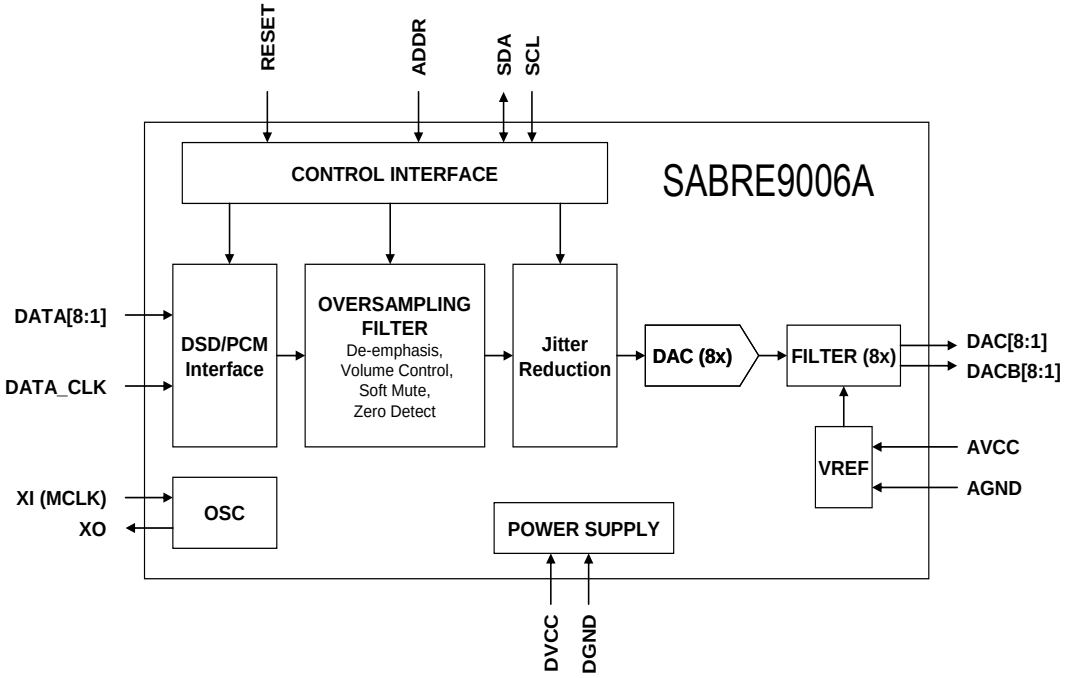
The Sabre Premier DAC sets a new standard for high-quality audio performance in a cost-effective, compact, easy to use form factor for today's most demanding digital audio applications.

FEATURE	DESCRIPTION
PatentedHyperStream®Architecture ○ DNR: +120dB ○ THD+N: –102dB	○ Unprecedented dynamic range and low distortion allowing true reproduction of audio as it is mastered at the recording studio
Patented Time Domain Jitter Reduction	○ Unmatched audio clarity free from input clock jitter allowing simple system design and layout
51-bit Accumulator and 28-bit Processing	○ Distortion free signal processing
Auto-detect PCM/DSD Converter	○ Universal (e.g. DVD/SACD) audio playback
8-channel DAC in 48-LQFP	○ Reduces PCB footprint and simplifies board layout
Low power (100mW for 8 channels)	○ Simplifies power supply design
Universal Digital Input	○ All-digital SPDIF, PCM (I^2S, MSB/LSB justified 16-, 20- or 24-bit) or DSD input
Integrated DSP functions	○ Click-free soft mute and volume control ○ Programmable filter characteristics for PCM/DSD ○ Programmable Zero detect ○ De-emphasis for 32kHz, 44.1kHz, and 48kHz sampling

APPLICATIONS

- Blu-ray players
- SACD / DVD-Audio players
- Audio receivers
- Home theater receivers
- Professional audio equipment

FUNCTIONAL BLOCK DIAGRAM



Migration Notes from ES9006S to SABRE9006AS

Hardware Compatibility from ES9006S to SABRE9006AS

SABRE9006AS parts are 100% pin-compatible to ES9006S parts. No PCB change is necessary.

Software Compatibility from ES9006S to SABRE9006AS

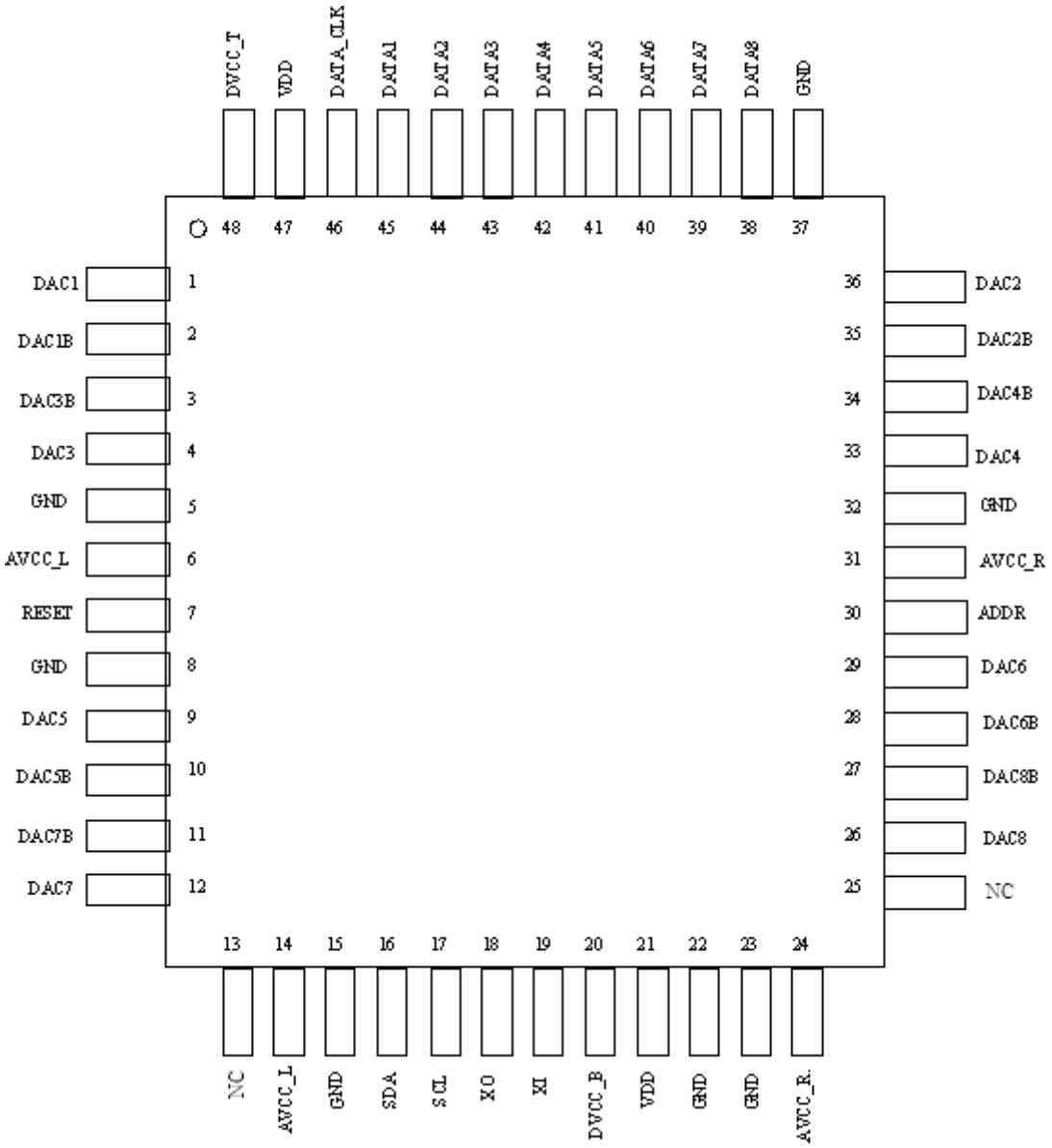
No software modification is required when migrating from ES9006S to SABRE9006AS.

New Functions in SABRE9006AS only

The following functions will by default be inactive after a hardware reset to maintain compatibility with ES9006S. Only customers interested in the new functions need to perform the specific programming to enable them.

Register	New Function (not available in ES9006S)
17	Mode Control for manual input mode selection,auto de-emphasis in SPDIF mode and 128x DPLL bandwidth
27-24	Master Trim
64	Chip ID, Auto-mute status and Lock status
69-66	DPLL_NUM readout
93-70	SPDIF channel status

PIN LAYOUT


DVCC_T
VDD
DATA_CLK
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
DATA8
GND
48
47
46
45
44
43
42
41
40
39
38
37
DAC1
1
DAC1B
2
DAC3B
3
DAC3
4
GND
5
AVCC_L
6
RESET
7
GND
8
DAC5
9
DAC5B
10
DAC7B
11
DAC7
12
36
DAC2
35
DAC2B
34
DAC4B
33
DAC4
32
GND
31
AVCC_R
30
ADDR
29
DAC6
28
DAC6B
27
DAC8B
26
DAC8
25
NC
13
14
15
16
17
18
19
20
21
22
23
24
NC
AVCC_L
GND
SDA
SCL
XO
XI
DVCC_B
VDD
GND
GND
AVCC_R

PIN DESCRIPTIONS

Pin	Name	I/O	Description
1	DAC1	O	Differential Positive Analog Output 1
2	DAC1B	O	Differential Negative Analog Output 1
3	DAC3B	O	Differential Negative Analog Output 3
4	DAC3	O	Differential Positive Analog Output 3
5	GND	-	Ground (Analog)
6	AVCC_L	-	Analog Power (+3.3V) for Left channels
7	RESET	I	Global Reset (Active high)
8	GND	-	Ground (Digital or Analog)
9	DAC5	O	Differential Positive Analog Output 5
10	DAC5B	O	Differential Negative Analog Output 5
11	DAC7B	O	Differential Negative Analog Output 7
12	DAC7	O	Differential Positive Analog Output 7
13	NC	-	No internal connection. May be grounded or connected to VDD if desired
14	AVCC_L	-	Analog Power (+3.3V) for Left channels
15	GND	-	Ground (Analog)
16	SDA	I/O	I^2C Serial Data I/O
17	SCL	I	I^2C Serial Clock Input
18	XO	O	Xtal oscillator output
19	XI (MCLK)	I	Xtal oscillator input (Note: can also just be a clock input)
20	DVCC_B	-	Digital Power (+3.3V) for bottom pad ring of chip
21	VDD	-	Digital Power (+1.2V) for core of chip
22	GND	-	Ground (Digital)
23	GND	-	Ground (Analog)
24	AVCC_R	-	Analog Power (+3.3V) for Right channels
25	NC	-	No internal connection. May be grounded or connected to VDD if desired.
26	DAC8	O	Differential Positive Analog Output 8
27	DAC8B	O	Differential Negative Analog Output 8
28	DAC6B	O	Differential Negative Analog Output 6
29	DAC6	O	Differential Positive Analog Output 6

PIN DESCRIPTIONS (continued)

Pin	Name	I/O	Description
30	ADDR	I	Chip Address Select
31	AVCC_R	-	Analog Power (+3.3V) for Right channels
32	GND	-	Ground (Analog)
33	DAC4	O	Differential Positive Analog Output 4
34	DAC4B	O	Differential Negative Analog Output 4
35	DAC2B	O	Differential Negative Analog Output 2
36	DAC2	O	Differential Positive Analog Output 2
37	GND	-	Ground (Digital)
38	DATA8	I	DSD Data8
39	DATA7	I	DSD Data7
40	DATA6	I	DSD Data6
41	DATA5	I	DSD Data5 OR PCM Data CH7/CH8
42	DATA4	I	DSD Data4 OR PCM Data CH5/CH6
43	DATA3	I	DSD Data3 OR PCM Data CH3/CH4
44	DATA2	I	DSD Data2 OR PCM Data CH1/CH2
45	DATA1	I	DSD Data1 OR PCM Frame Clock OR SPDIF Input
46	DATA_CLK	I	PCM Bit Clock OR DSD Bit Clock
47	VDD	-	Digital Power (+1.2V) for core of chip
48	DVCC_T	-	Digital Power (+3.3V) for top pad ring of chip

Table 1

5V Tolerant Pins

The following pins are 5V tolerant:

- DATA_CLK
- DATA 1-8
- SCL
- SDA
- RESET
- ADDR

FUNCTIONAL DESCRIPTION

NOTATATIONS for Sampling Rates

Mode	fs
DSD	DATA_CLK/64
Serial (PCM) Normal Mode	DATA_CLK/64
SPDIF	SPDIF Sampling Rate

PCM, SPDIF and DSD Pin Connections

The following tables show how the pins are used for PCM and DSD audio formats.

PCM Audio Format

Note: XI clock (MCLK) must be > 192 x fs when using PCM input (normal mode)

Pin Name	Description
DATA1	Frame clock
DATA[2:5]	8-channel PCM serial data
DATA_CLK	Bit clock for PCM audio format

Table 2

SPDIF Audio Formant

Note: XI clock (MCLK) must be > 386 x fs when using SPDIF input

Pin Name	Description
DATA1	SPDIF input

Table 3

DSD Audio Format

Note: XI clock (MCLK) must be > 192 x fs when using DSD input

Pin Name	Description
DATA[1:8]	8-channel DSD data input
DATA_CLK	Bit clock for DSD data input

Table 4

Feature Description

Soft Mute

When Mute is asserted the output signal will ramp to the –∞ level. When Mute is reset the attenuation level will ramp back up to the previous level set by the volume control register. Asserting Mute will not change the value of the volume control register. The total time is 8192/($2^{<Register\#16[2:0]>}$x fs) seconds, where fs = DATA_CLK/64 in PCM serial or DSD modes, or SPDIF sampling rate in SPDIF mode.

AUTOMUTE

AUTOMUTE is used to achieve the absolute maximum signal-to-noise ratio on an idle channel.

- In PCM serial mode, AUTOMUTE will become active once the audio data is continuously below the threshold set by <Register Automute_lev>, for a length of time defined by 2096896/(<Register#9> x DATA_CLK) Seconds.
- In SPDIF mode, the AUTOMUTE will become active once the audio data is continuously below the threshold set by <Register Automute_lev>, for a length of time defined by 2096896/(<Register#9> x (64 x fs) Seconds, where fs is the SPDIF sampling rate.
- In the DSD Mode, AUTOMUTE will become active when any 8 consecutive values in the DSD stream have as many 1's and 0's for a length of time defined by 2096896/(<Register Automute_time> x DATA_CLK) Seconds. The following table summarizes the conditions.

Mode	Detection Condition	Time
PCM	Data is continuously lower than <Register Automute_lev >	2096896/(<Register Automute_time > x DATA_CLK)
SPDIF	Data is continuously lower than <Register Automute_lev >	2096896/(<Register Automute_time > x (64 x fs)) where fs is the SPDIF sampling rate
DSD	Equal number of 1s and 0s in every 8 bits of data	2096896/(<Register Automute_time > x DATA_CLK)

Table5

De-emphasis

The de-emphasis feature is included for audio data that has utilized the 50/15µs pre-emphasis for noise reduction. There are three de-emphasis filters, one for 32kHz, one for 44.1kHz, and one for 48kHz.

Volume Control

Each output channel has its own attenuation circuit. The attenuation for each channel is controlled independently. Each channel can be attenuated from 0dB to –127dB in 0.5dB steps.
Each 0.5dB step transition takes 64 intermediate levels. The result being that the level changes are done using small enough steps so that no switching noise occurs during the transition of the volume control. When a new volume level is set, the attenuation circuit will ramp softly to the new level.

Master Trim

Themaster trim sets the 0dB reference level for the volume control of each DAC. The master trim is programmable via registers 24-27 and is a 32-bit signed number. Therefore it should never exceed 32'h7FFFFFFF (as this is full-scale signed).

PCM Audio Interface Formats

Several interface formats are provided so that direct connection to common audio processors is possible. The available formats and their accompanying diagrams are listed in the following table. The audio interface format can be set by programming the registers.

Format	Description	Figure
0	MSB First, Left Justified, up to 24-bit data	1A
1	I^2S, up to 24-bit data	2A
2	MSB First, Right Justified, 24-bit data	3A
3	MSB First, Right Justified, 20-bit data	3B
4	MSB First, Right Justified, 16-bit data	3C
5	DSD Normal Mode	4A
6	DSD Phase Mode	4B

Table 6

Programmable FIR filter

A two stage interpolating FIR design is used. The interpolating FIR filter is generated using MATLAB, and can then be downloaded using a custom C code.

Example Source Code for Loading a Filter

```
// only accept 128 or 16 coefficients
// Note:  The coefficients must be quantized to 24 bits for this method!
// Note:  Stage 1 consists of 128 values (0-127 being the coefficients)
// Note:  Stage 2 consists of 16 values (0-13 being the coefficients, 14-15 are zeros)
// Note:  Stage 2 is symmetric about coefficient 13.  See the example filters for more information.
byte reg19 = (byte)(coeffs.Count == 128 ? 0 : 128);
for (int i = 0; i < coeffs.Count; i++)
{
// stage 1 contains 128 coefficients, while stage 2 contains 16 coefficients
registers.WriteRegister(19, (byte)(reg26 + i));

// write the coefficient data
    registers.WriteRegister(20, (byte)(coeffs[i] &0xff));
registers.WriteRegister(21, (byte)((coeffs[i] >>8) &0xff));
    registers.WriteRegister(22, (byte)((coeffs[i] >>16) &0xff));

registers.WriteRegister(23, 0x02);// set the write enable bit
}
// disable the write enable bit when’we're done
registers.WriteRegister(23, (byte)(setEvenBit ? 0x04 : 0x00));
```

Audio Interface Formats

Several interface formats are provided so that direct connection to common audio processors is possible. The available formats are shown in the following diagrams. The audio interface format can be set by programming the registers.

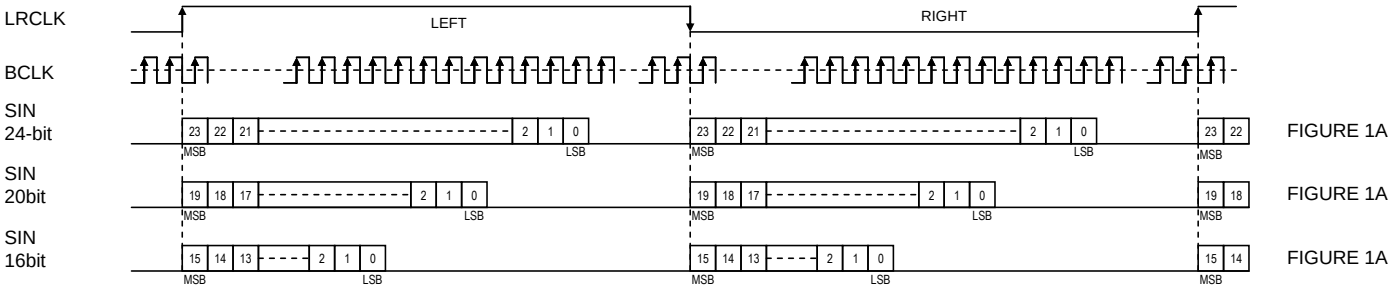


FIGURE 1A

LEFT JUSTIFIED FORMAT

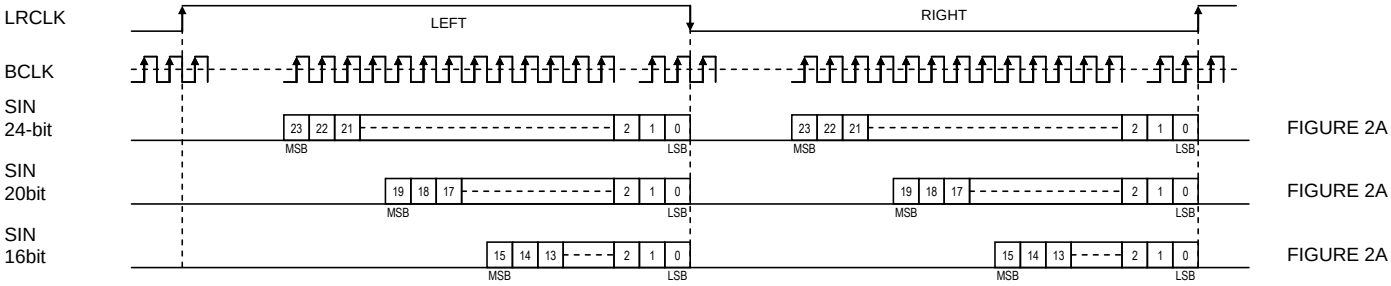


FIGURE 2A

RIGHT JUSTIFIED FORMAT

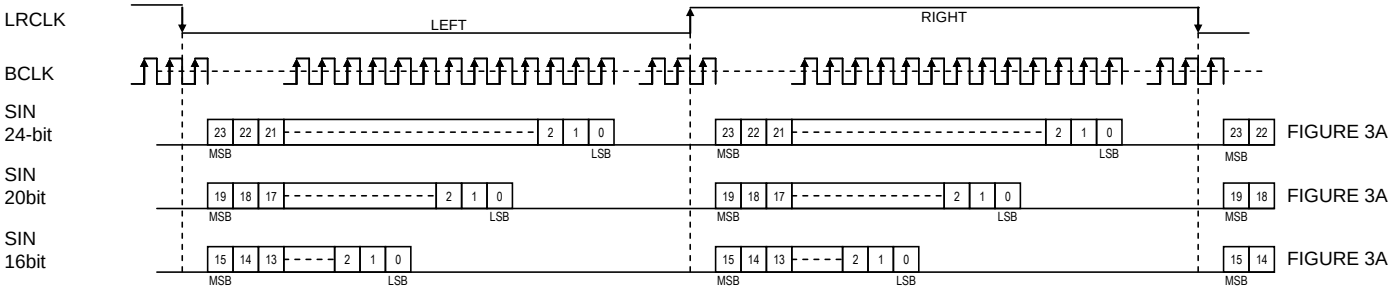


FIGURE 3A

I2S FORMAT

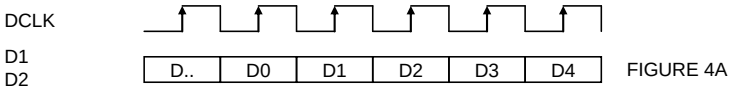


FIGURE 4A

DSD NORMAL MODE

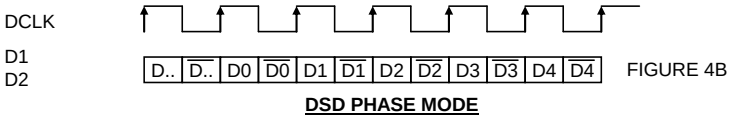


FIGURE 4B

DSD PHASE MODE

System Clock (XI / MCLK)

A system clock is required for proper operation of the digital filters and modulation circuitry.
The system clock must be greater than 192 x fs for SERIAL/DSD inputs, or greater than 386 x fs for SPDIF input.

Data Type	Valid MCLK Frequencies
DSD Data	50MHz > MCLK > 192 x fs , fs = 2.8224MHz/64
Serial Mode	50MHz > MCLK > 192 x fs
SPDIF Data	50MHz > MCLK > 386 x fs

Data Clock

This must be 64 x fs for SERIAL / DSD modes, and is not required for SPDIF mode.

Digital Filters

There are numerous applications for a stereo DAC so for added flexibility; two digital filter settings are possible, sharp roll-off and a slow roll-off for PCM mode. For DSD mode, there is 1 available filter with cutoff at 50kHz.

Serial Control Interface

The registers inside the chip are programmed via an I²C interface. The diagram below shows the timing for this interface.
The chip address can be set to 2 different settings via the “ADDR” pin. The table below summarizes this.

ADDR	CHIP ADDRESS
0	0x90
1	0x92

Table 7

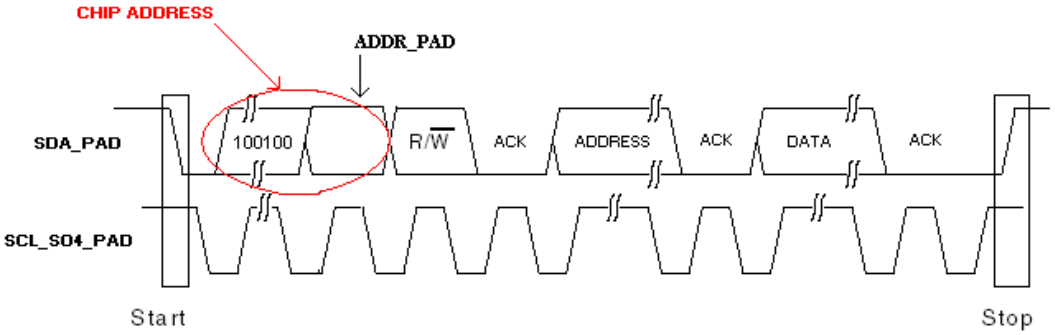


Diagram 1

Notes:

1. The “ADDR” pin is used to create the CHIP ADDRESS. (0x90, 0x92)
2. The first byte after the chip address is the “ADDRESS” this is the register address.
3. The second byte after the CHIP ADDRESSis the “DATA” this is the data to be programmed into the register at the previous “ADDRESS”.
4. Compatible with I²C-bus specification version 2.1 Standard-mode/Fast-mode.

Register Settings:

Register #0: Volume of DAC0 (default = 8'd0)

Volume in dBs = -REG_VALUE/2

Register #1: Volume of DAC1 (default = 8'd0)

Volume in dBs = -REG_VALUE/2

Register #2: Volume of DAC2 (default = 8'd0)

Volume in dBs = -REG_VALUE/2

Register #3: Volume of DAC3 (default = 8'd0)

Volume in dBs = -REG_VALUE/2

Register #4: Volume of DAC4 (default = 8'd0)

Volume in dBs = -REG_VALUE/2

Register #5: Volume of DAC5 (default = 8'd0)

Volume in dBs = -REG_VALUE/2

Register #6: Volume of DAC6 (default = 8'd0)

Volume in dBs = -REG_VALUE/2

Register #7: Volume of DAC7 (default = 8'd0)

Volume in dBs = -REG_VALUE/2

Register #8: Automute_lev (default = 1'b0,7'd104)

[7]: SPDIF_ENABLE.
1'b0 = Use either I²S or DSD input
1'b1 = Use SPDIF input
[6:0]: Auto-mute trigger point in dB = -REG_VALUE

Register #9: Automute_time (default = 8'd4)

Larger REG_VALUE = less time.
Smaller REG_VAULE = longer time.
Time in Seconds = 2096896/(REG_VALUE x DATA_CLK).

Register #10: Mode Control 1 (default = 8'b00000110)

Default is 24-bit,I²S,NO-DEEMP,UNMUTE.
[7:6]: 24-/20-/16-Bit for Serial Data Modes.
- 2'b00 = 24-Bit
- 2'b01 = 20-Bit
- 2'b10 = 16-Bit
- 2'b11 = 24-Bit

[5:4]: LJ/I²S/RJ Serial Data Modes.
- 2'b00 = I²S
- 2'b01 = LJ
- 2'b10 = RJ
- 2'b11 = I²S

[3]: RESERVED
[2]: JITTER_REDUCTION_ENABLE.
- 1'b0 = Bypass and stop JITTER_REDUCTION.
- 1'b1 = Use JITTER_REDUCTION.

[1]: BYPASS_DEEMPHASIS FILTER
- 1'b0 = Use De-emphasize Filter
- 1'b1 = Bypass De-emphasis Filter

[0]: MUTE DACS
- 1'b0 = Unmute All DACs
- 1'b1 = Mute All DACs

Register #11: Mode Control 2 (default = 8'b00000101)

[7:5]: RESERVED.
[4:2]: DPLL BANDWIDTH
- 3'b000 => No Bandwidth

3'b001 => Lowest Bandwidth
- 3'b010 => Low Bandwidth
- 3'b011 => Med-Low Bandwidth
- 3'b100 => Medium Bandwidth
- 3'b101 => Med-High Bandwidth
- 3'b110 => High Bandwidth
- 3'b111 => Highest Bandwidth

[1:0]: DE-EMPHASIS DELECT
- 2'b00 = 32kHz
- 2'b01 = 44.1kHz
- 2'b10 = 48kHz
- 2'b11 = RESERVED

Register #12: Mode Control 3 (default = 8'b00000000)

[7:0]: RESERVED

Register #13: RESERVED (default = 8'b00000000)

[7:0]: RESERVED

Register #14: FIR Rolloff (default = 8'b00000001)

[7:1]: RESERVED
[0]: FIR ROLLOFF SPEED
1'b0 = Slow Rolloff
1'b1 = Fast Rolloff

Register #15: Mode Control 4 (default = 8'b0000000)

[7:0]: RESERVED

Register #16: VOLUME_CONFIG (default = 8'b01111000)

[7]: CHANNEL MAPPING
1'b0 = 8 Channels
1'b1 = 2 Channels

[6:4]: RESERVED

[3]: AUTOMUTE LOOPBACK
1'b0 => Auto-mute condition will not reduce volume to –infinity
1'b1 => Auto-mute condition will reduce volume to –infinity

[2:0]: VOL_RAMP_RATE (Time = 8192/(2^{vrr} x fs)
3'b000 => Time = 8192/(fs)
3'b001 => Time = 4096/(fs)
3'b010 => Time = 2048/(fs)
3'b011 => Time = 1024/(fs)
3'b100 => Time = 512/(fs)
3'b101 => Time = 256/(fs)
3'b110 => Time = 128/(fs)
3'b111 => Time = 64/(fs)

Register #17: Mode Control 4 (default = 8'b00001110)

[7:4]: Reserved

[3:2]: Input_select
2'b00 =>serial
2'b01 =>DSD
2'b10 => auto detect
2'b11 => auto detect (default)

[1]: dpll_bw_128x
1'b1 => Multiply the DPLL BANDWIDTH setting by 128.
1'b0 => Use the DPLL BANDWIDTH setting.

[0]: spfi_auto_deemph
1'b1: Automatically enable the de-emphasis filters depending on the channel status bits
1'b0: Do not automatically enable the de-emphasis filters depending on the channel status bits

Register #19: Programmable Filter Address

8 bit, Read-Write Register, Default = 0x00

Bits	[7]	[6:0]						
Mnemonic	prog_coeff_stage	prog_coeff_addr						
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
[7]	prog_coeff_stage	Selects which stage of the filter to write. 1'b0 = Stage 1 of the oversampling filter (128 coefficients). 1'b1 = Stage 2 of the oversampling filter (16 coefficients)
[6:0]	prog_coeff_addr	Selects the coefficient address when writing custom coefficients for the oversampling filter.

Register #22-20: Programmable Filter Coefficient

8 bit, Read-Write Register, Default = 0x000000

Bits	[23:0]
Mnemonic	prog_coeff
Default	24'd0

Bit	Mnemonic	Description
[23:0]	prog_coeff	A 24-bit filter coefficient that will be written to address 'prog_coeff_addr'.

Register #23: Programmable Filter Control

8 bit, Read-Write Register, Default = 0x00

Bits	[7:3]					[2]	[1]	[0]
Mnemonic	reserved *					even_stage2_coeff	prog_coeff_we	prog_coeff_en
Default	0	0	0	0	0	0	0	0

Bit	Mnemonic	Description
[7:3]	reserved *	
[2]	even_stage2_coeff	Sets the type of symmetry of the stage 2 programmable filter. 1'b0 = Uses a sine symmetric filter (27 coefficients). 1'b1 = Uses a cosine symmetric filter (28 coefficients).
[1]	prog_coeff_we	1'b0 = Disable writing to the custom filter coefficients. 1'b1 = Enable writing to the custom filter coefficients. Note: When set to 1'b1 the custom filter will be bypassed regardless of the state of register 21[0].
[0]	prog_coeff_en	1'b0 = Use one of the built-in oversampling filters. 1'b1 = Use the custom oversampling filter. Note: The custom filter is not programmed to anything on reset, valid coefficients must be written to the filter before enabling.

* All Reserved Bits in Register #23 must be set to the indicated logic level to ensure correct device operation.

Notes: even_stage2_coeff sets the type of symmetry used by the second stage filter. The actual RAM is 16 coefficients, but only the first 14 coefficients are used when applying the oversampling filter. The first 14 coefficients are mirrored using either sine or cosine symmetry, resulting in a filter length of either 27 or 28 taps. This means that the second stage RAM should only contain half of the impulse response of the second stage filter, and the impulse peak value will be contained in the 14th coefficient. Also note that, due to the symmetry of the filter, only linear phase filters may be used in the second stage

Register #27-24: Master Trim (default = 32'h7FFFFFFF)

This is a 32 bit value that sets the 0dB level for all volume controls. This is a signed number, so it should never exceed 32'h7fffffff (which is 2^{31} - 1). Register 27contains the MSBs, Register 24 contains the LSBs.

Register #64: DAC Status

[7:5]: Chip_id
Returns 3'd4 (SABRE9006A)

[3:2]: Reserved

[1]: Automute_status
1'b1 => Auto-mute condition is active.
1'b0 => Auto-mute condition is inactive.

[0]: Lock_status
1'b1 => The Jitter Eliminator is locked to an incoming signal.
1'b0 => The Jitter Eliminator is not locked to an incoming signal.

Register #69-66: DPLL_NUM

32-bit, Read-Only Register. Register 69 contains the MSBs, Register 66 contains the LSBs

This is a read-only 32-bit value that can be used to calculate the sample rate. The sample rate (F_{in}) can be calculated using: $F_{in} = (DPLL\_NUM \times F_{MCLK}) / 2^{32}$.

Register #93-70

Register 93 contains the MSBs, Register 70 contains the LSBs. Format is [191:0]

These registers allow read back of the SPDIF channel status. The status definition is different for the consumer configuration and professional configuration. Please refer to the following two tables for details.

SPDIF CHANNEL STATUS - Consumer configuration

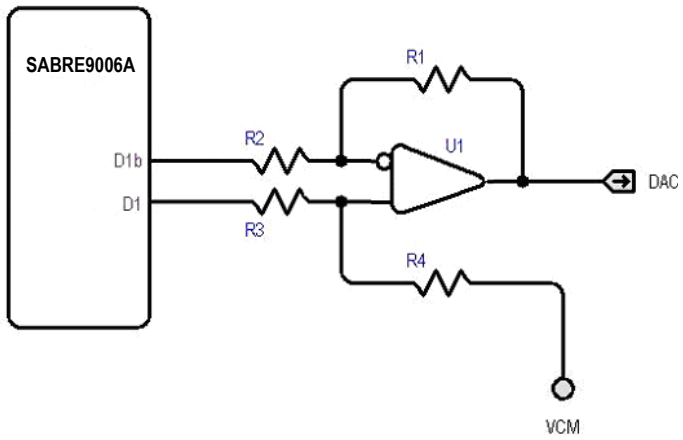
Address Offset	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	Reserved	Reserved	0:2Channel 1:4Channel	Reserved	0:No-Preemph 1:Preemph	0:CopyRight 1:Non-CopyRight	0:Audio 1:Data	**0:Consumer** 1:Professional
1	Category Code 0x00: General 0x01:Laser-Optical 0x02:D/D Converter 0x03:Magnetic 0x04:Digital Broadcast 0x05:Musical Instrument 0x06:Present A/D Converter 0x08:SolidState Memory 0x16:Future A/D Converter 0x19:DVD 0x40:Experimental							
2	Channel Number 0x0:Don't Care 0x1:A (Left) 0x2:B (Right) 0x3:C 0x4:D 0x5:E 0x6:F 0x7:G 0x8:H 0x9:I 0xA:J 0xB:K 0xC:L 0xD:M 0xE:N 0xF:O				Source Number 0x0:Don't Care 0x1:1 0x2:2 0x3:3 0x4:4 0x5:5 0x6:6 0x7:G 0x8:8 0x9:9 0xA:10 0xB:11 0xC:12 0xD:13 0xE:14 0xF:15			
3	Reserved	Reserved	Clock Accuracy 0x0:Level 2 +-1000ppm 0x1:Level 1 +-50ppm 0x2:Level 3 variable pitch shifted		Sample Frequency 0x0:44.1k 0x2:48k 0x3:32k 0x4:22.05k 0x6:24k 0x8:88.2k 0xA:96k 0xC:176.4k 0xE:192k			
4	Reserved	Reserved	Reserved	Reserved	Word Length: If Word Field Size=0 |If Word Field Size = 1 000=Not indicated |000=Not indicated 100 = 23bits |100 = 19bits 010 = 22bits |010 = 18bits 110 = 21bits |110 = 17bits 001 = 20bits |001 = 16bits 101 = 24bits |101 = 20bits			Word Field Size 0:Max 20bits 1:Max 24bits
5-23	Reserved							

SPDIF CHANNEL STATUS - Professional configuration

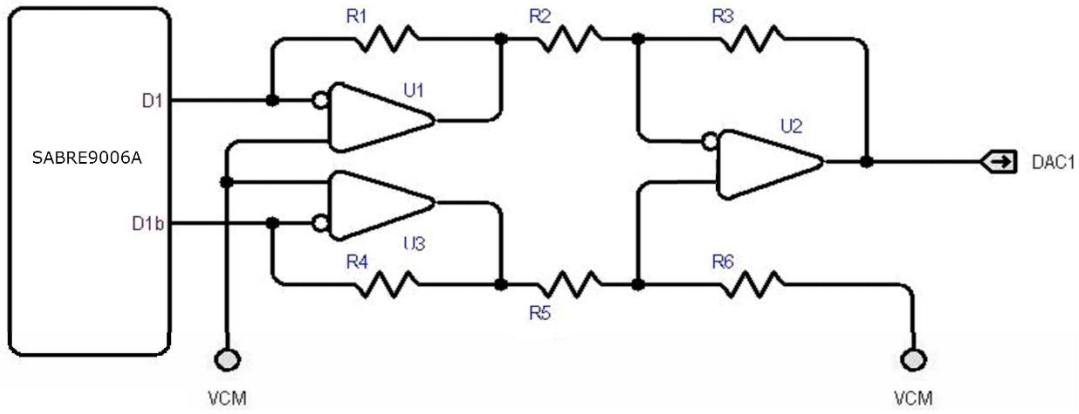
Address Offset	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	sampling frequency: 00: not indicated (or see byte 4) 10: 48 kHz 01: 44.1 kHz 11: 32 kHz		lock: 0: locked 1: unlocked	emphasis: 000: Emphasis not indicated 001: No emphasis 011: CD-type emphasis 111: J-17 emphasis			0:Audio 1:Non-audio	0:Consumer **1:Professional**
1	User bit management: 0000: no indication 1000: 192-bit block as channel status 0100: As defined in AES18 1100: user-defined 0010: As in IEC60958-3 (consumer)				Channel mode: 0000: not indicated (default to 2 channel) 1000: 2 channel 0100: 1 channel (monophonic) 1100: primary / secondary 0010: stereo 1010: reserved for user applications 0110: reserved for user applications 1110: SCDSR (see byte 3 for ID) 0001: SCDSR (stereo left) 1001: SCDSR (stereo right) 1111: Multi-channel (see byte 3 for ID)			
2	alignment level: 00: not indicated 10: –20dB FS 01: –18.06dB FS		Source Word Length: If max =20-bits | If max=24-bits 000=Not indicated | 000=Not indicated 100 = 23-bits | 100 = 19-bits 010 = 22-bits | 010 = 18-bits 110 = 21-bits | 110 = 17-bits 001 = 20-bits | 001 = 16-bits 101 = 24-bits | 101 = 20-bits		Use of aux sample word: 000: not defined, audio max 20-bits 100: used for main audio, max 24-bits 010: used for coord, audio max 20-bits 110: reserved			
3	Channel identification: if bit 7 = 0 then channel number is 1 plus the numeric value of bits 0-6 (bit reversed). if bit 7 = 1 then bits 4–6 define a multi-channel mode and bits 0–3 (bit reversed) give the channel number within that mode.							
4	fs scaling: 0: no scaling 1: apply factor of 1 / 1.001 to value		Sample frequency (fs): 0000: not indicated 0001: 24kHz 0010: 96kHz 1001: 22.05kHz 1010: 88.2kHz 1011: 176.4kHz 0011: 192kHz 1111: User defined		Reserved		DARS (Digital audio reference signal): 00: not a DARS 01: DARS grade 2 (±10ppm) 10: DARS grade 1(±10ppm) 11: Reserved	
5	Reserved							
6-9	Alphanumerical channelorigin: four-character label using 7-bit ASCIIwith no parity. Bits 55, 63, 71, 79 = 0.							
10-13	Alphanumerical channeldestination: four-character label using 7-bit ASCIIwith no parity. Bits 87, 95, 103, 111 = 0.							
14-17	Local sample addresscode: 32-bit binary number representingthe sample count of the first sampleof the channel status block.							
18-21	time of day code: 32-bit binary number representingtime of source encoding in samplessince midnight							
22	reliability flags 0: data in byte range is reliable 1: data in byte range is unreliable							
23	CRCC 00000000: not implemented X: error check code for bits 0–183							

APPLICATION DIAGRAMS

Differential Voltage Mode



Differential Current Mode



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Storage temperature	–65°C to +105°C
Voltage range for 5V tolerant pins	–0.5V to +5.5V
Voltage range for all other pins	–0.5V to (DVCC_T+0.5V) or –0.5V to (DVCC_B+0.5V)

WARNING: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	0°C to 70°C
Θjmax	TjMax	125°C
θja	Tja	60°C/W
θjc	Tjc	17°C/W
Digital core supply voltage	VDD	1.2V ± 5%, 23mA nominal (Note 1)
Digital power supply voltage	DVCC_T, DVCC_B	3.3V ± 5%, 9mA nominal (Note 1)
Analog power supply voltage	AVCC_L, AVCC_R	3.3V ± 5%, 16mA nominal (Note 1)

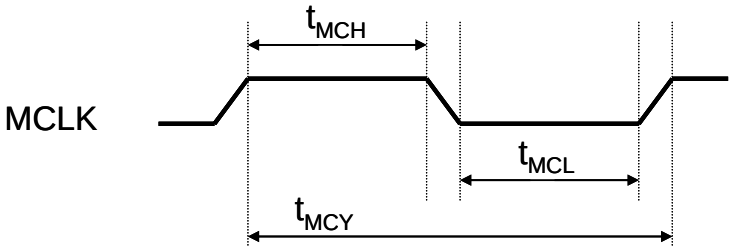
Note

1) fs =48kHz, MCLK=40MHz, I^2S input, output unloaded

DC ELECTRICAL CHARACTERISTICS

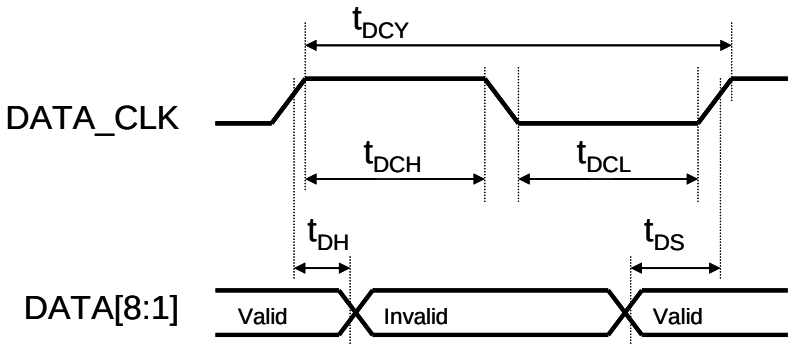
SYMBOL	PARAMETER	MIN	MAX	UNIT	COMMENTS
V_{IH}	High-level input voltage	2.0	DVCC_T or DVCC_B	V	All inputs TTL levels except CLK and 5V tolerant input pins
		2.0	5.5	V	All 5V tolerant inputs
V_{IL}	Low-level input voltage	–0.3	0.8	V	All input TTL levels except CLK
V_{CLKH}	CLK high-level input	2.0	DVCC_B+0.25	V	TTL level input
V_{CLKL}	CLK low-level input	–0.3	0.8	V	
V_{OH}	High-level output voltage	3.0		V	I_{OH} = 1mA
V_{OL}	Low-level-output voltage		0.45	V	I_{OL} =4mA
I_{LI}	Input leakage current		±15	µA	
I_{LO}	Output leakage current		±15		
C_{IN}	Input capacitance		10	pF	fc = 1MHz
C_O	Input/output capacitance		12		
C_{CLK}	CLK capacitance		20	pF	fc = 1MHz

MCLK Timing



Parameter	Symbol	Min	Max	Unit
MCLK pulse width high	T_{MCH}	6		ns
MCLK pulse width low	T_{MCL}	6		ns
MCLK cycle time	T_{MCY}	20		ns
MCLK duty cycle		45:55	55:45	

Audio Interface Timing



Parameter	Symbol	Min	Max	Unit
DATA_CLK pulse width high	t_{DCH}	20		ns
DATA_CLK pulse width low	t_{DCL}	20		ns
DATA_CLK cycle time	t_{DCY}	60		ns
DATA_CLK duty cycle		45:55	55:45	
DATA set-up time to DATA_CLK rising edge	t_{DS}	2		ns
DATA hold time to DATA_CLK rising edge	t_{DH}	2		ns

ANALOG PERFORMANCE

Test Conditions (unless otherwise stated)

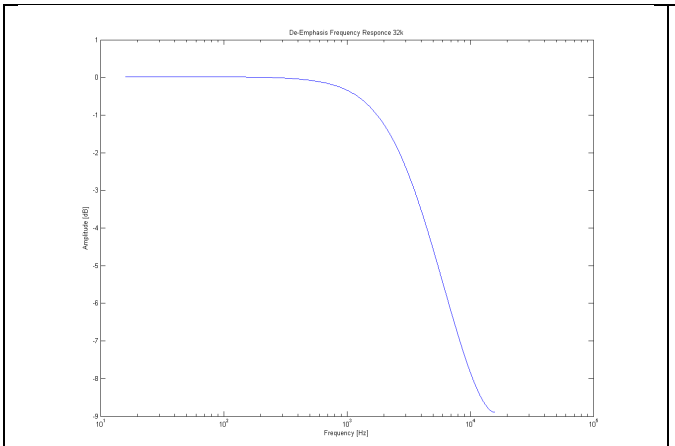
1. T_A=25°C, AVCC=3.3V, DVCC=1.2V, fs =44.1kHz, MCLK=27MHz and 24-bit data
2. SNR/DNR: A-weighted over 20Hz-20kHz in averaging mode
3. THD+N: un-weighted over 20Hz-20kHz bandwidth

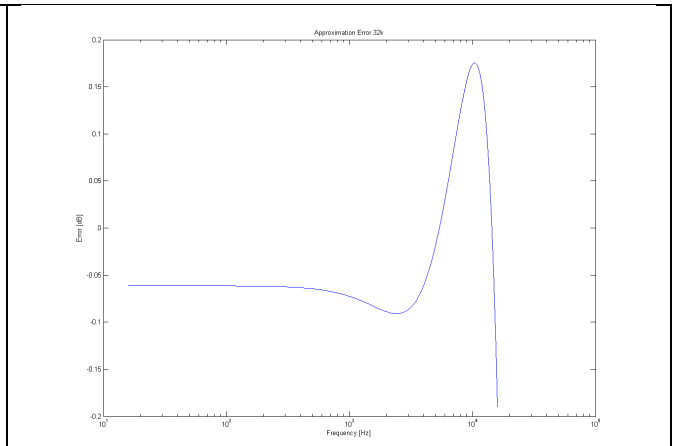
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				24		Bits
MCLK (Note: fs=DATACLK/64 in DSD mode)		Serial/DSD in	192		4096	fs
		SPDIF in	386		4096	fs
DYNAMIC PERFORMANCE						
DNR		–60dBFS		120		dB-A
THD+N		0dBFS		–102		dB
PCM sampling frequency (fs)					200	kHz
ANALOG OUTPUT						
Differential (+ or –) voltage output range		Full-scale out		3.05 (0.924 x AVCC)		Vp-p
Differential (+ or –) voltage output offset		Bipolar zero out		1.65 (AVCC/2)		V
Differential (+ or –) current output range (Note *1)		Full-scale out		3.656		mAp-p
Differential (+ or –) current output offset (Note *1)		Bipolar zero out to virtual ground at voltage Vg (V)		2.112 – 1000 x Vg/ 834		mA
Digital Filter Performance						
De-emphasis error					±0.2	dB
Mute Attenuation				127		dB
PCM Filter Characteristics (Sharp Roll Off)						
Pass band		±0.0dB			0.454fs	Hz
		–3dB			0.49fs	Hz
Stop band		<–100dB	0.546fs			Hz
Group Delay				35/fs		s
PCM Filter Characteristics (Slow Roll Off)						
Pass band		±0.05dB			0.308fs	Hz
		–3dB			0.454fs	Hz
Stop band		<–100dB	0.814fs			Hz
Group Delay				6.25/fs		s
DSD Filter Characteristics						
Pass band		–3dB		1.1338fs		Hz
Stop band attenuation				18		dB/oct

Note

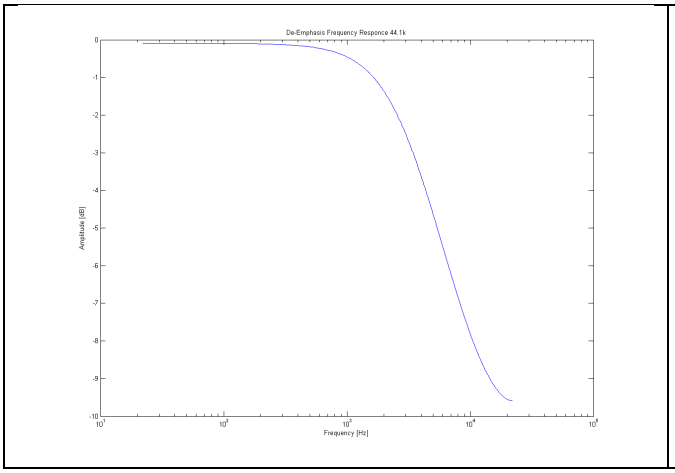
*1. Differential (+ or –) current output is equivalent to a differential (+ or –) voltage source in series with an 834Ω±11% resistor. The differential (+ or –) voltage source has a peak-to-peak output range of (0.924 x AVCC) = 3.05V and an output offset of (AVCC/2) = 1.65V.

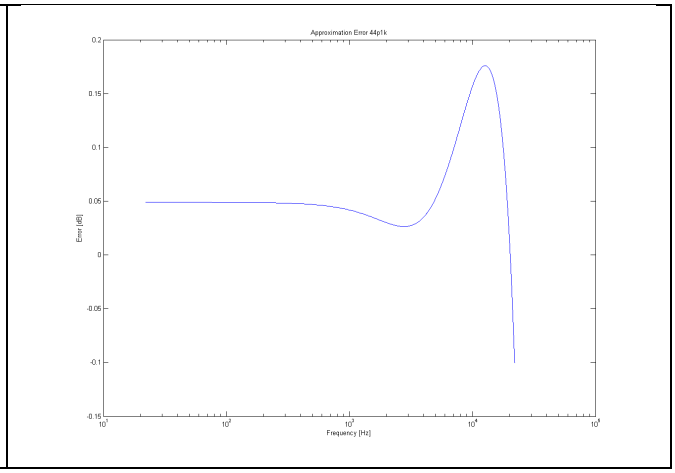
PCM DE-EMPHASIS FILTER RESPONSE (32kHz)



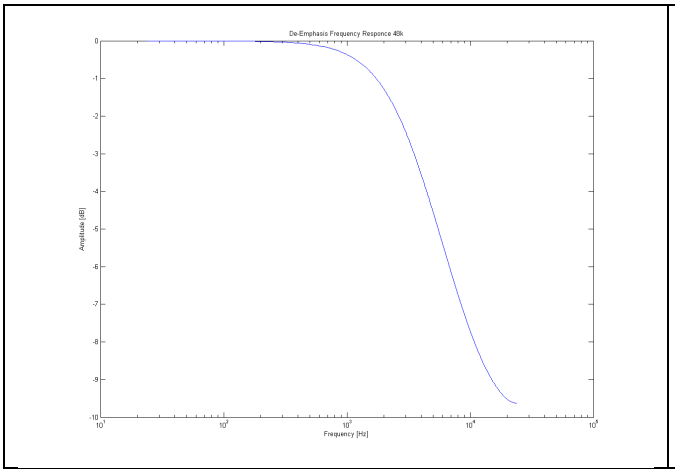


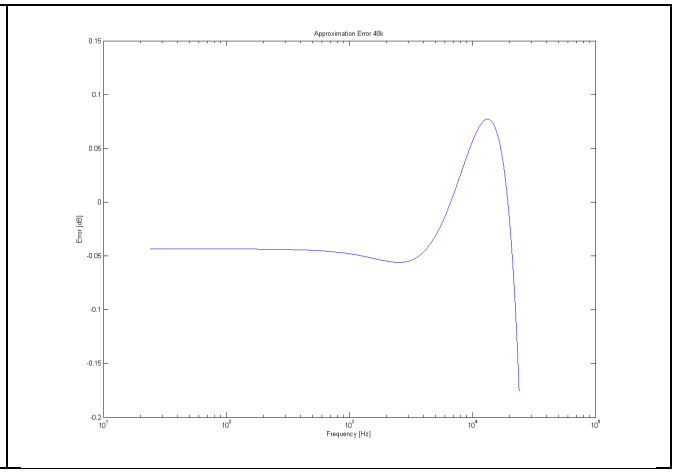
PCM DE-EMPHASIS FILTER RESPONSE (44.1kHz)



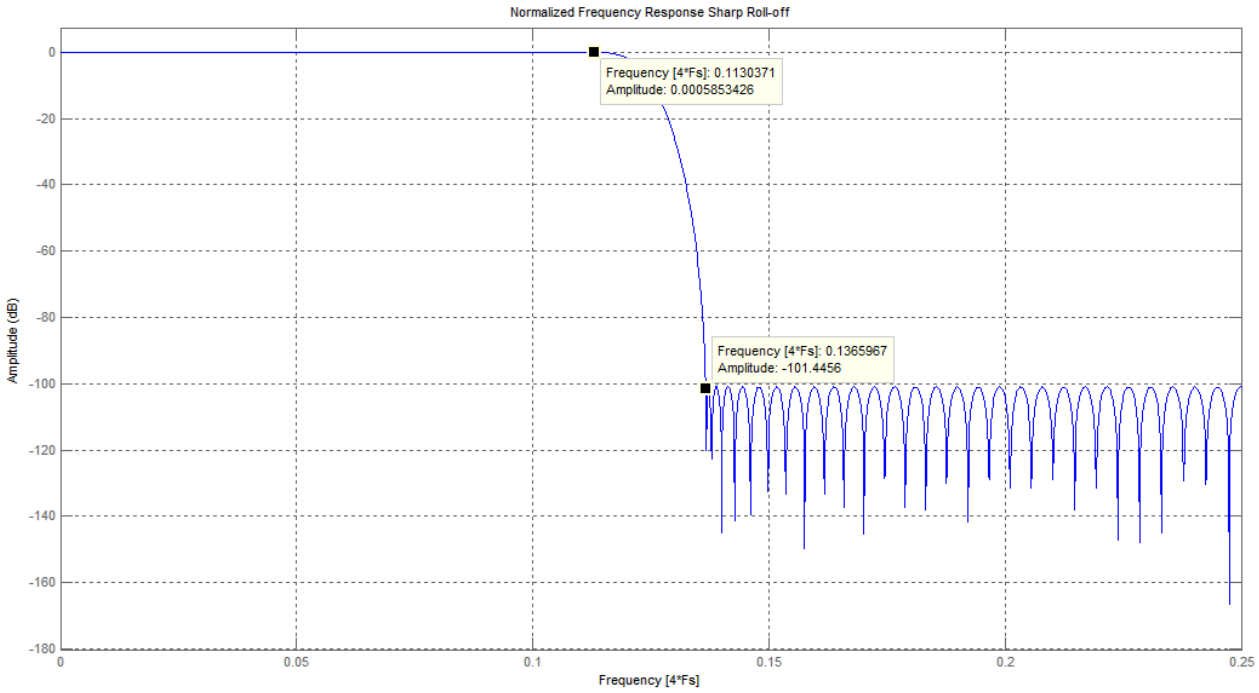


PCM DE-EMPHASIS FILTER RESPONSE (48kHz)

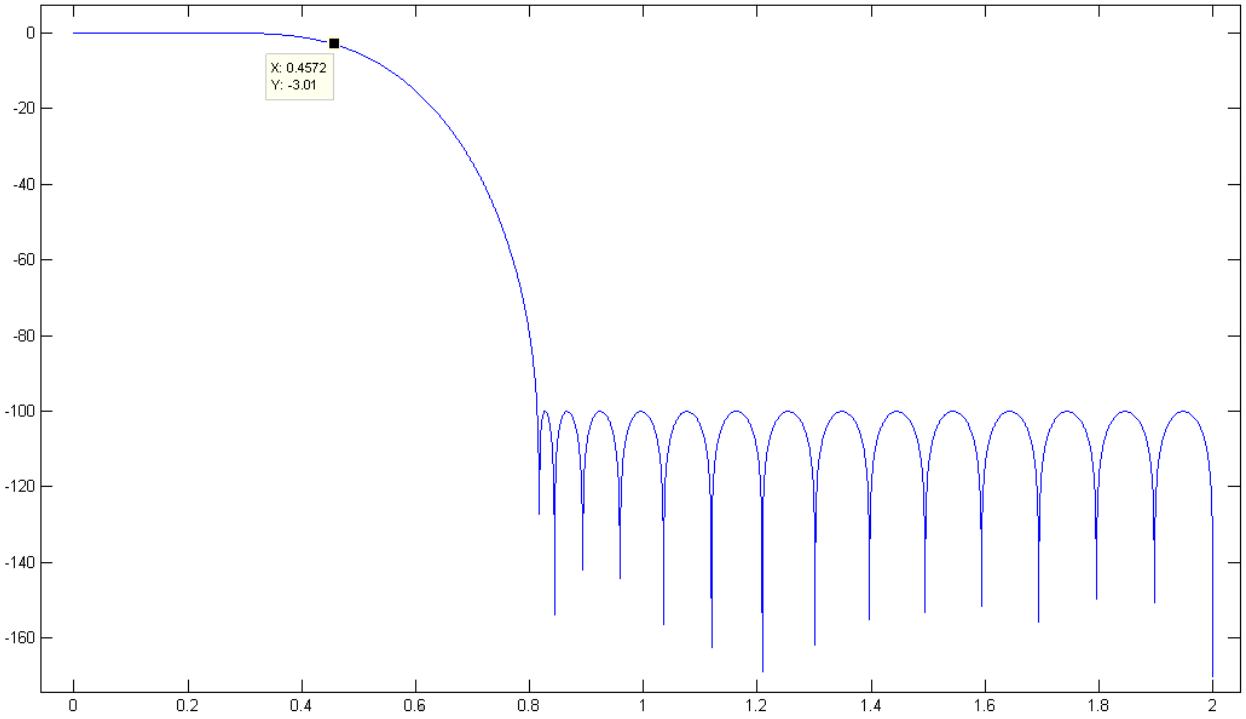




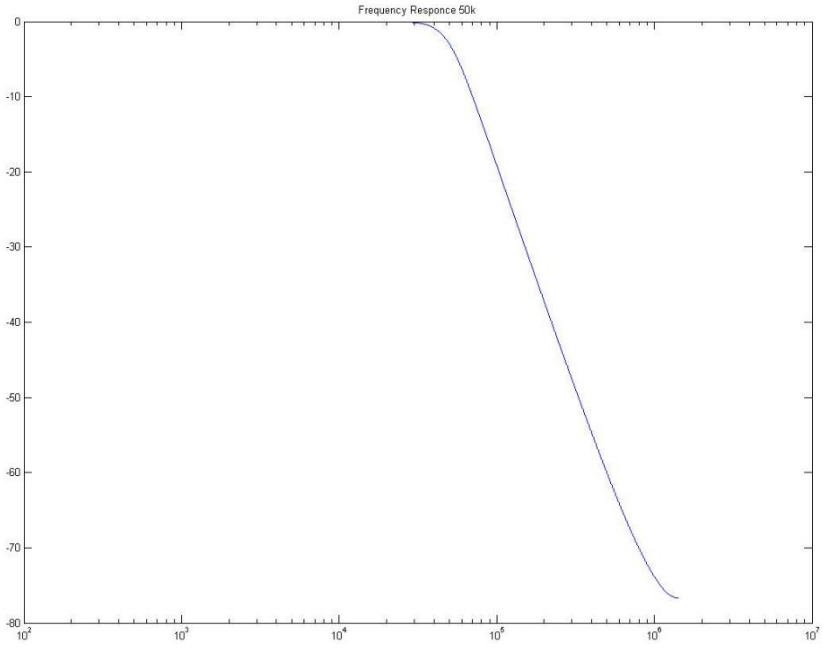
PCM SHARP ROLL-OFF FILTER RESPONSE



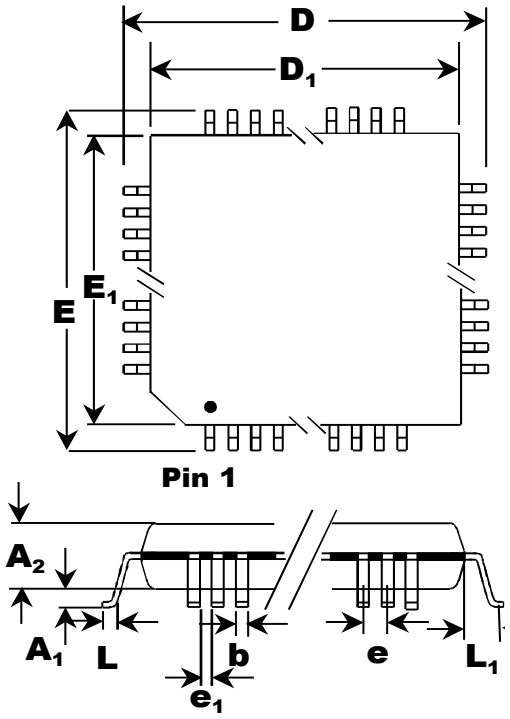
PCM SLOW ROLL-OFF FILTER RESPONSE



DSD FILTER RESPONSE



48-Pin LQFP Mechanical Dimensions



		MILLIMETERS		
Symbol	Description	Min.	Nom.	Max.
D	Lead-to Lead, X-axis	8.75	9.00	9.25
D1	Package's Outside, X-axis	6.90	7.00	7.10
E	Lead-to Lead, Y-axis	8.75	9.00	9.25
E1	Package's Outside, Y-axis	6.90	7.00	7.10
A1	Board Standoff	0.05	0.10	0.15
A2	Package Thickness	1.35	1.40	1.45
b	Lead Width	0.17	0.20	0.27
e	Lead Pitch		0.50 BSC	
e_1	Lead Gap	0.23	0.30	0.33
L	Foot Length	0.45	0.60	0.75
L1	Lead Length		1.00	
	Co-planarity			0.102
	Foot Angle	0°		7°
	No. of Leads in X-axis		12	
	No. of Leads in Y-axis		12	
	No. of Leads Total		48	
	Package Type		LQFP	

Reflow Process Considerations

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor you need to consider.

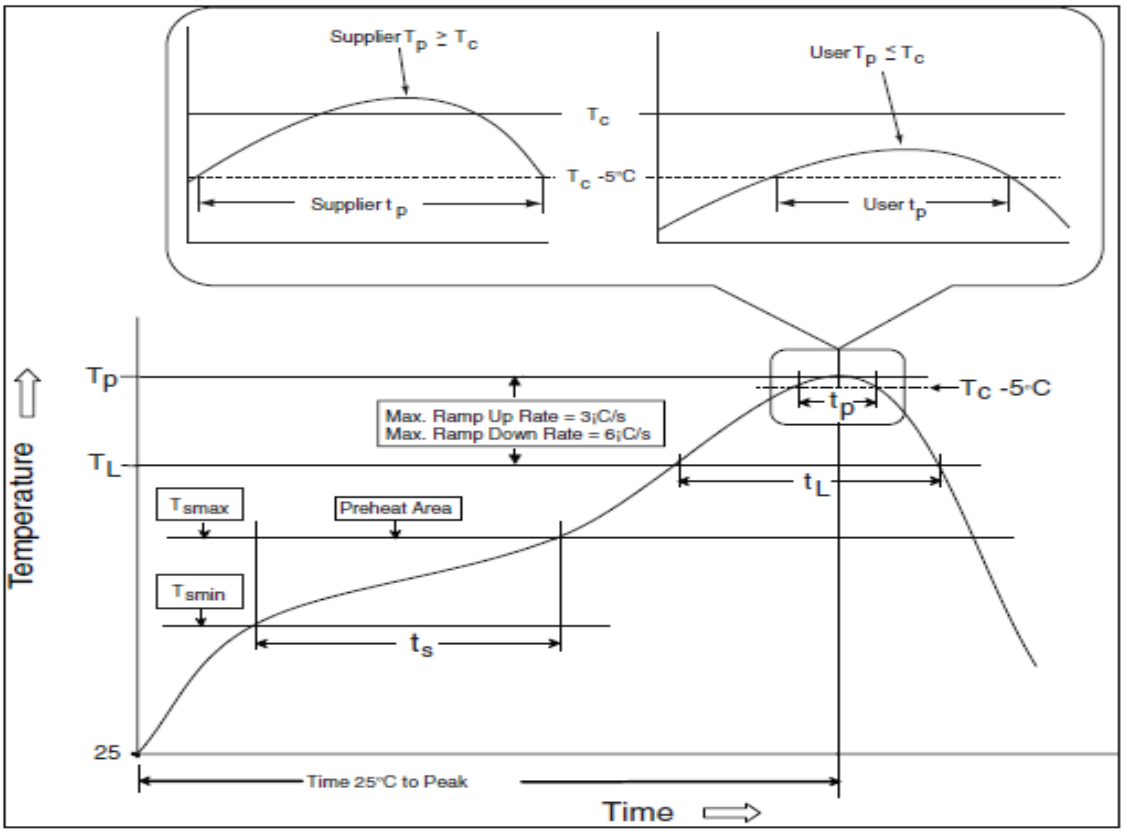
The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size *(Table RPC-2)*. This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits *(Table RPC-2)*.

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

Figure RPC-1. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)



Note: Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual Soldering:

Allowed with maximum temperature of 350 degrees Centigrade for no longer than 3 seconds.

Table RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C/second max.
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of thespecifiedclassification temperature(Tc), see Figure RPC-1	30* seconds
Ramp-down rate (Tp to TL)	°C/second max.
Time 25 °C to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp **shall** be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile **shall** be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.
For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

Note 3: All components in the test load **shall** meet the classification profile requirements.

Table RPC-2 Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm - 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or non-integral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

ORDERING INFORMATION

Part Number	Description	Package
SABRE9006AS	Sabre Premier 8-channel Audio DAC	48-pin LQFP

The letter S at the end of the part number identifies the package type LQFP

Revision History

Revision	Date	Notes
0.1	May 20 2014	Initial version
0.2	July 22, 2014	Updated ESS' FAX number.Added medical usage legal disclaimer. Page 17, corrected polarity of U2 on differential current mode circuit
0.3	August 20, 2014	Pins 13 & 25 changed from VDD to NC. Pins 21 & 47 remain as VDD pins
0.4	September 16, 2014	Updated DAC output resistance from 781.25Ω to 834Ω±11%
0.5	January 22, 2015	Updated formatting and corrected typos.
0.6	April 14, 2015	Corrected formulae in Analog Performance Table. Updated ESS' address and phone number.
0.61	April 30, 2015	Updated the product overview on cover page.
0.7	May 26, 2015	Corrected Master Trim register addresses. Added programmable FIR function.
0.71	May 27, 2015	Added note that pins 13 & 25 can be connected to VDD or GND if desired.
0.8	February 18, 2016	Corrected typical differential output current range from 3.903 mAp-p to 3.656 mAp-p
0.9	November 28, 2017	Remove ESS logo from pin diagram
1.0	January 15, 2019	Added Tja and Tjc values for recommended operation conditions.
1.1	September 12, 2019	Changed Hyperstream™ to Hyperstream®
1.2	May 4, 2020	Update register 16: volume config

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