5A, I²C Controlled Output Synchronous Step-Down Converter

DESCRIPTION

The ETA355E is a high-efficiency, DC-to-DC step-down switching regulator, capable of delivering 5A load, up to 6.5A of pulse load. It integrates an I²C interface that dynamically scales the output voltages on demand. The DCDC control block belongs to a new breed of high frequency synchronous Step-Down converter that combines the advantages of voltage mode control and Constant-On-Time control. Its adaptive Constant-On-Time control dynamically changes switch on time to achieve a constant switching frequency. It does not have the minimum on-time constrain normally a fixed-frequency current mode Step-down requires, allowing it to go down to very low duty ratio without affecting loop stability. The voltage mode nature also provides a more superior load transient response and a seamless transition from PFM to PWM modes. Cycle-by-cycle current limit provides output short-circuit protection and an input OVP function guards ETA355E against possible input voltage surge. ETA355E is housed in a 2mm x 1.6mm CSP-20 Package.

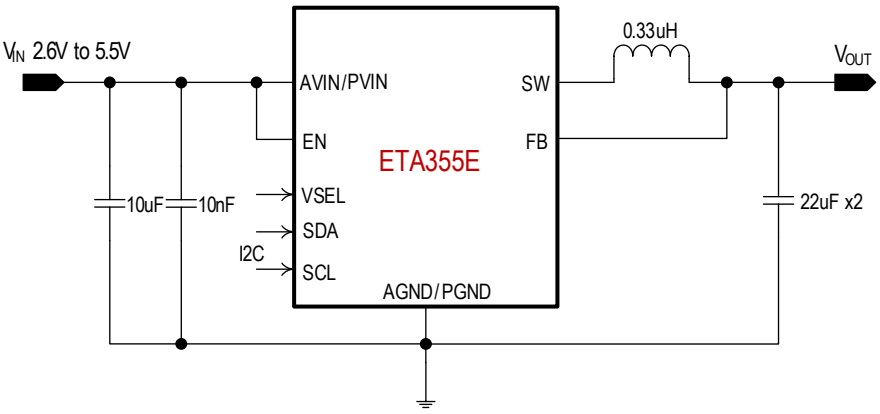
FEATURES

- I²C Dynamic Output Control
- Synchronous High Efficiency up to 95%
- Fast load transient response
- Capable of Delivering 5A
- Pulse Current capability 6.5A
- Input OVP at 6.2V
- No External Schottky Diode Needed
- Thermal shutdown and UVLO
- CSP-20 (4x5) package

APPLICATIONS

- ARM based CPUs
- Smart Phone
- Tablet, MID
- Smart Set-Top Box, OTT

TYPICAL APPLICATION

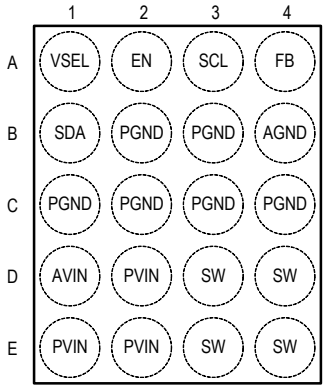


Typical Application Circuit

ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA355ECSU	CSP-20 (4x5)	355E YWWL(Date Code)	3000

PIN CONFIGURATION



Top View

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

VIN Voltage .....–0.3V to 6.0V
All Other Pin Voltage .....VIN–0.3V to VIN+0.3V
SW to ground current.....Internally limited
Operating Temperature Range .....–40°C to 85°C
Storage Temperature Range .....–55°C to 150°C
Thermal Resistance Θ_{JA}
CSP4x5-20.....35 ..... °C/W
Lead Temperature (Soldering,10sec) .....260°C
ESD HBM (Human Body Mode) 2KV
ESD MM (Machine Mode) 200V

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, unless otherwise specified. Typical values are at TA = 25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		2.5		5.5	V
Input UVLO	Rising, Hysteresis=350mV		2.35	2.54	V
Input OVP Shutdown	Rising Threshold		6.15		V
	Falling Threshold	5.5	5.85		
Input Supply Current	I_{OUT} =0,PFM Mode, Device Not Switching		55	100	μA
Input Shutdown Current	EN=GND		0.1	10	μA
	EN=VIN, BUCKEN=0		3.5	10	μA
Thermal Shutdown	Rising, Hysteresis =20°C		155		°C
DC/DC converter					
Default Output Voltage	VSEL=0, default bit 10011110	0.88	0.9	0.92	V
	VSEL=1, default bit 01101000		0		V
Load Regulation			0.5		%/A
Line Regulation	V_{IN} =3V to 4V		0.04		%/V
Switching Frequency		1.56	2	2.25	MHz
Maximum Duty Cycle			100		%
PMOS Switch On Resistance	I_{SW} =500mA		40		mΩ
NMOS Switch On Resistance	I_{SW} =500mA		15		mΩ
High Side PMOS Switch Current Limit			8		A
Maximum Output Current Limit			6		A
Short Circuit Hiccup mode off time	EN=VIN		20		ms
Output Discharge Pull-down			1000		Ω

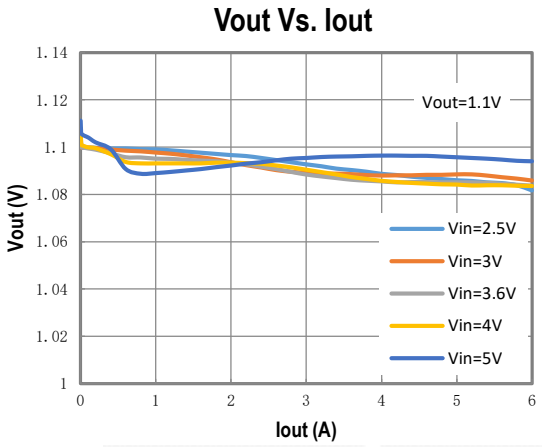
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
EN, VSEL					
Input Low Voltage				0.4	V
Input High Voltage		1.2			V
EN shutdown deglitch time	Blanking Time from EN=0 to chip shutdown		800		ns
Input Current				1	µA
I²C Control					
SCL Clock Frequency			400		KHz
SDA Setup Time			100		ns
SDA hold time			50		ns
Input Low Voltage				0.4	V
Input High Voltage		1.2			V

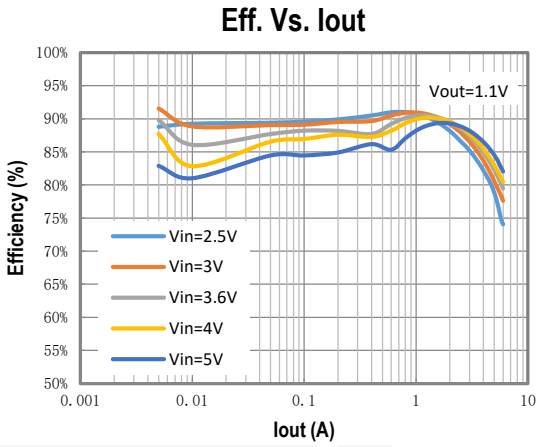
PIN DESCRIPTION

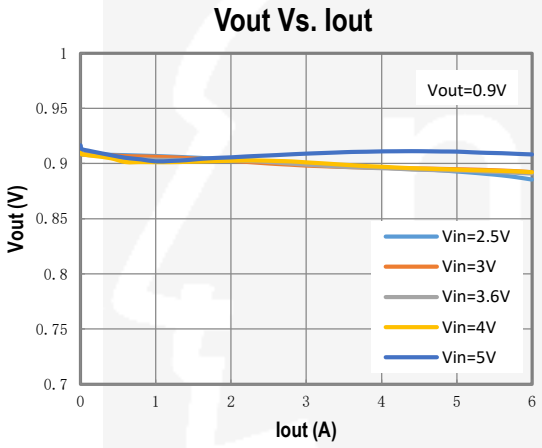
PIN #	NAME	DESCRIPTION
A1	VSEL	Output voltage and mode selection pin
A2	EN	Chip enable control pin, pull high to turn the chip on
A3	SCL	Clock pin for I²C interface
A4	FB	Feedback Input pin, connect to the output capacitor thru a trace.
B1	SDA	Data IO pin for I²C interface
B2, B3, C1, C2, C3, C4	PGND	Power ground for large switching current
B4	AGND	Analog ground, for internal control circuit
D1	AVIN	Analog supply for internal control circuit
D2, E1, E2	PVIN	Power supply for large switching current
D3, D4, E3, E4	SW	Switching node, to connect a 0.33-0.47uH inductor

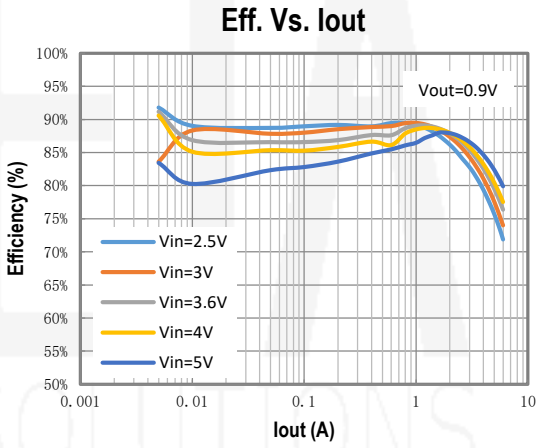
TYPICAL CHARACTERISTICS

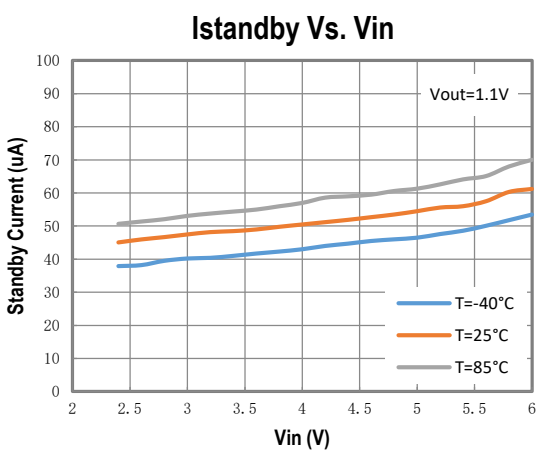
(Typical values are at T_A = 25°C unless otherwise specified.)

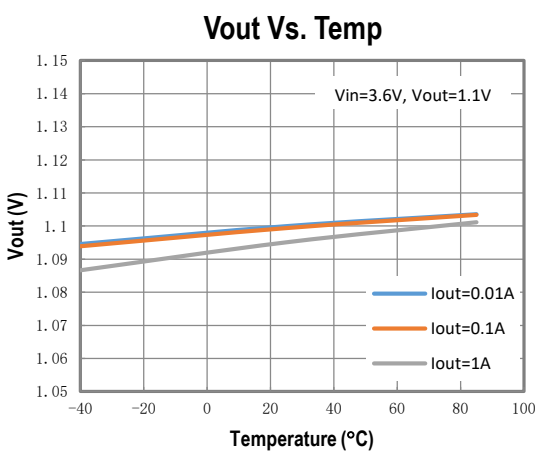








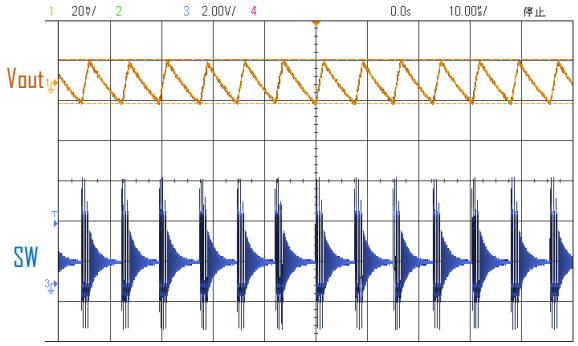




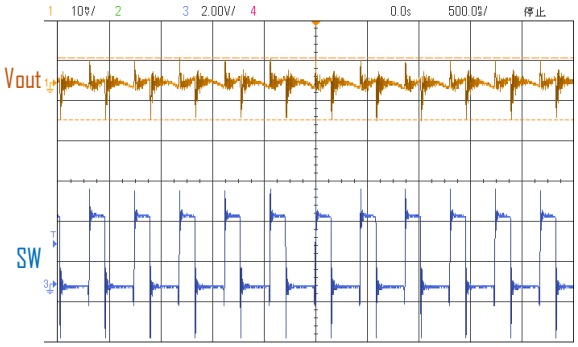
TYPICAL CHARACTERISTICS cont'

(Typical values are at T_A = 25°C unless otherwise specified.)

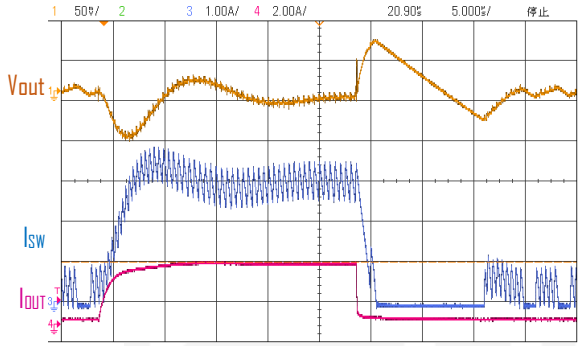
Switching Waveform: V_{IN}=3.6V, Vout=1.15V, I_{OUT}=100mA



Switching Waveform: V_{IN}=3.6V, Vout=1.15V, I_{OUT}= 3A



Load Transient Respond: Vin=3.6V, Vout=1.15V, I_{OUT}=0.3 – 3A



FUNCTIONAL DECRIPTIONS

The ETA355E is a high-efficiency, DC-to-DC step-down switching regulator, capable of delivering 5A load, up to 6.5A of pulse load. It integrates an I²C interface that dynamically scales the output voltages on demand. The I²C interface can also program the ramp rate output voltage changes and enable or disable the regulator.

DCDC Control scheme

ETA355E uses an adaptive Constant-On-Time control scheme that the ON time is dynamically adjusted according to VIN and VOUT so to achieve a nearly constant switching frequency. This control scheme provides simpler compensation and superior transient response over traditional constant frequency current mode control, while still maintaining the advantage of switching at a constant frequency at about 2MHz. It also provides a seamless transition from PFM to PWM that normally a constant frequency current mode control scheme is hard to achieve. Further mode, because it is a COT control scheme, the system can achieve high step-down ratio at ease, because lower constrain on the minimum on- time requirement existing in constant frequency scheme.

Current Limit and Short-Circuit protection

ETA355E employs a cycle-by-cycle peak current limit and it also has a hiccup mode that protects the circuit during dead-short condition. When the dead-short condition is removed, the IC goes back to normal operation.

Enable and Soft-start

ETA355E has an internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the I soft-start circuitry slowly ramps up current available at SW.

EN logic low level that sustains shorter than 500ns, won't shutdown IC.

Table 1

Pins		BITS		
EN	VSEL	BUCK_EN0	BUCK_EN1	OUTPUT
0	X	X	X	OFF
1	0	0	X	OFF
1	0	1	X	ON
1	1	X	0	OFF
1	1	X	1	ON

ETA355E keeps the output voltage setting that was programmed in the previous EN=High cycle when EN is toggled low. So when EN is pulled high again, the output voltage is the same as previous on cycle.

When Out_dis bit in addr 02h is enabled(logic high) and EN pin or BUCK_ENx is low, a load is connected from V_{out} to GND to discharge output capacitor.

Output voltage programming

Vout=0.6V+10mV*B<5:0>(Addr 00h/01h)

VSEL pin=0, Addr 00h controls Vout setting; VSEL pin=1, Addr 01h controls Vout setting. The IC works in forced PWM mode when MODEx=1; it can operate in auto PFM mode when the load is light and MODEx=0.

Transition Slew Rate

When transitioning a low to high voltage, the slew rate of the IC can be programmed using the SLEW BITS.

Table 2.

Decimal	SLEW<2:0>	Slew Rate	
0	000	64	mV/us
1	001	32	mV/us
2	010	16	mV/us
3	011	8	mV/us
4	100	4	mV/us
5	101	2	mV/us
6	110	1	mV/us
7	111	0.5	mV/us

For output voltage transition from high to low, the discharging speed depends on output load. So in light load, if a faster transition speed is needed, one can set B3(addr 02h)=0. This brings the IC into the forced PWM mode, thereby helping V_{OUT} discharging. For even faster slew setting, B6(Addr 00/01h) can be set to 1 to keep the IC in forced PWM longer for V_{OUT} discharging.

UVLO and Thermal Shutdown

If IN drops below UVLO threshold, the UVLO circuit inhibits switching. Once IN rises above ULVO threshold, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J= +155°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

REGISTER DESCRIPTIONS

ETA355E DEVICE ADDRESS: C0

Table 3.

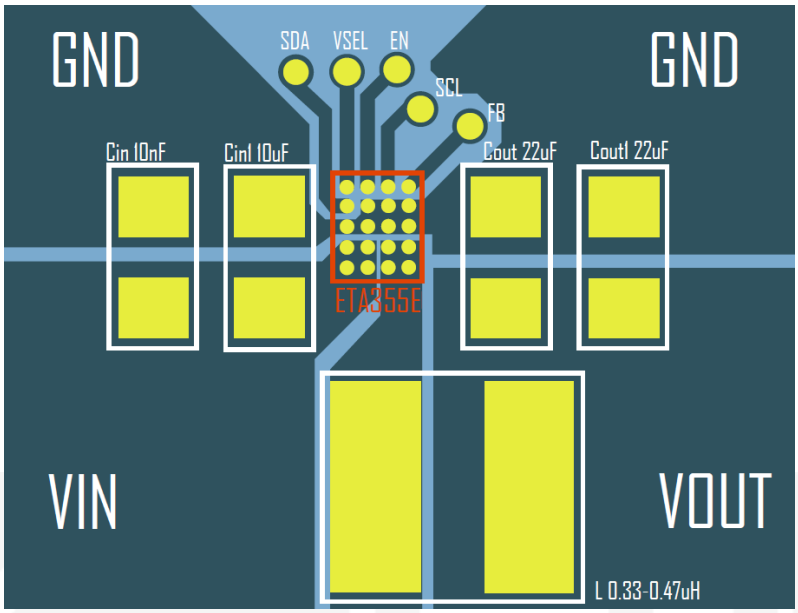
Addr		B7	B6	B5	B4	B3	B2	B1	B0
00h	Name	BUCK_EN0	MODE0	VSEL0<5>	VSEL0<4>	VSEL0<3>	VSEL0<2>	VSEL0<1>	VSEL0<0>
		Software enable See table 1.	PWM/PFM Select ①	VSEL=0,V_{OUT} set by VSEL0<5:0>					
	Default	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0**
	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
01h	Name	BUCK_EN1	MODE1	VSEL1<5>	VSEL1<4>	VSEL1<3>	VSEL1<2>	VSEL1<1>	VSEL1<0>
		Software enable See table 1.	PWM/PFM Select ①	VSEL=1,V_{OUT} set by VSEL1<5:0>					
	Default	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**0**
	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
02h	Name	Out_dis	SLEW<2>	SLEW<1>	SLEW<0>	DVSMODE	Reserved	Reserved	Reserved
		Output discharge enable	SLEW<2:0>: set Slew Rate of V_{OUT} transition See table 2.			Mode when V_{OUT} transition			
	Default	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
03h	Name	VENDOR<2>	VENDOR<1>	VENDOR<0>	PGOOD	DIE_ID<3>	DIE_ID<2>	DIE_ID<1>	DIE_ID<0>
		VENDOR<2:0>: Specify the IC Vendor			②	DIE_ID<3:0>: IC TYPE=0xE			
	Default	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0**
	Access	R	R	R	R	R	R	R	R

Note:

①MODEx=0, auto PFM during light load; MODEx=1, forced PWM mode.
②PGOOD=1 indicates the output voltage level established.

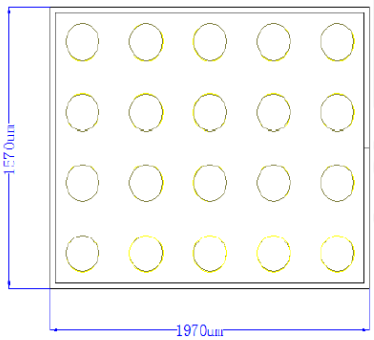
PCB GUIDELINE

A recommended PCB layout is shown below. The input capacitor has to be placed as close to the ETA355E as possible.

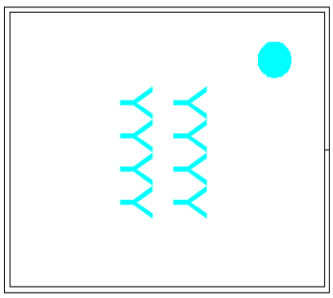


PACKAGE OUTLINE

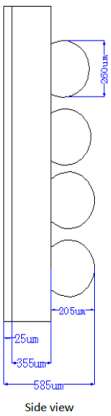
Package: CSP-20 (4x5)



Bottom View



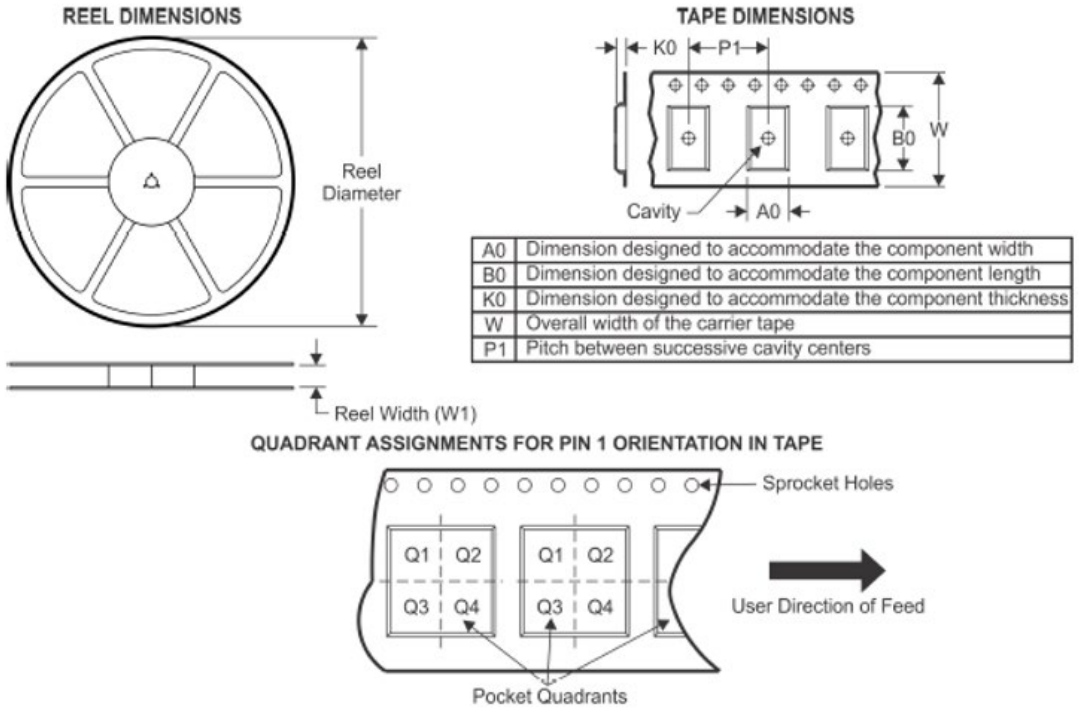
Top View



Side view

Parameter	Min	Normal	Max
	Millimeters		
Package body dimension X	1.95	1.97	1.99
Package body dimension Y	1.55	1.57	1.59
Package Height	0.555	0.585	0.615
SI thickness	0.3425	0.355	0.3675
Bump Height	0.185	0.205	0.225
Bump Diameter	0.24	0.26	0.28
Total Ball Count Per Die	/	20	/
Ball Pitch X axis (min)	/	0.4	/
Ball Pitch Y axis (min)	/	0.4	/

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ETA355ECSU	CSP-20	20	3000	178	9.5	1.69	2.19	0.68	4	8	Q1

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