

18V, 3A, High Efficiency Synchronous Step-Down Converter

DESCRIPTION

ETA8113 is a wide input range, high-efficiency and high frequency DC-to-DC step-down switching regulator, capable of delivering up to 3A of output current. It adopts an Adaptive COT control scheme that enables very fast transient response and provides a very smooth transition when the output varies from light load to heavy load. During light load, ETA8113 goes into a PFM mode that saves switching loss achieving high efficiency. The adaptive COT control also maintains a constant switching frequency across line and load. An OVP function protects the IC itself and its downstream system against input voltage surges. With this OVP function, the IC can stand off input voltage as high as 19V, making it an ideal solution for industrial applications such as LCD TV, Set Top Box, Portable TV, etc. ETA8113 is available in SOT23-6 package.

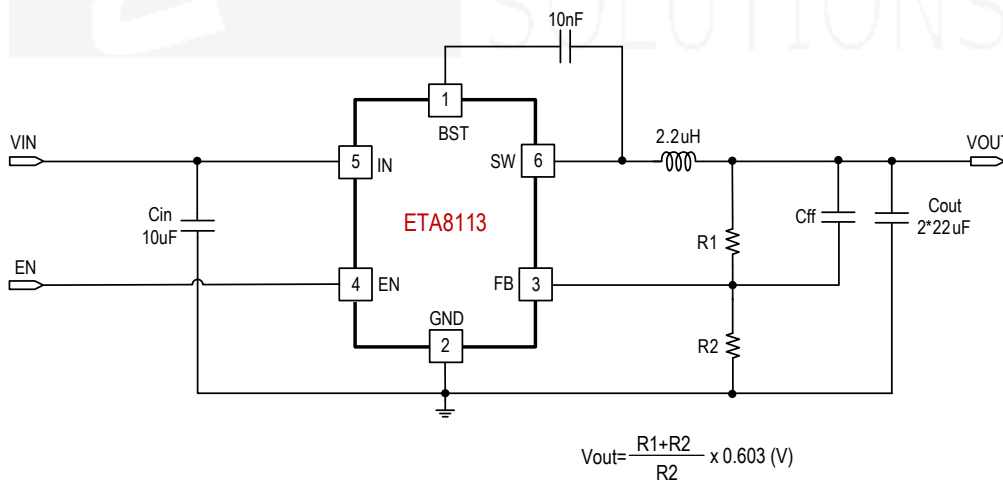
FEATURES

- ◆ Wide Input Range: 4.5V-18V
- ◆ Adaptive COT Control
- ◆ Ultra-Fast Load Transient Response
- ◆ High Efficiency PFM Mode at Light Load
- ◆ High Efficiency Synchronous Operation
- ◆ No Load IQ 177uA
- ◆ Low R_{dson} Internal Power FETs
- ◆ Capable of Delivering 3A
- ◆ No External Compensation Needed
- ◆ Thermal Shutdown and UVLO
- ◆ Available in SOT23-6 Package

APPLICATIONS

- ◆ LCD TV
- ◆ Set Top Box
- ◆ xDSL Modem

TYPICAL APPLICATION

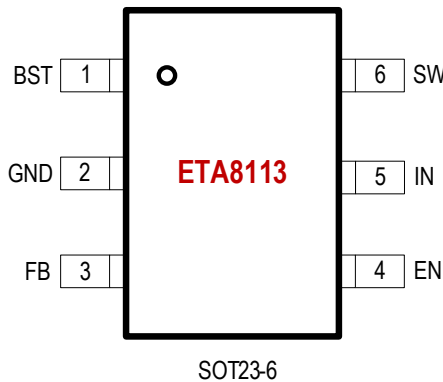


* R2 has to be between 1KOhm to 20KOhm

ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA8113S2G	SOT23-6	DuYW	3000

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

IN,EN Voltage	-0.3V to 19V
SW Voltage.....	-0.3V ⁽¹⁾ to 19V ⁽²⁾
BST Voltage	-0.3V to SW+6V
FB Voltage	-0.3V to 6V
Junction Temperature	150°C
Storage Temperature Range	-55°C to 150°C
Thermal Resistance	θ_{JA} θ_{JC}
JESD51-3 ⁽³⁾	180.....90..... °C/W
EVB ⁽⁴⁾80.....30..... °C/W
Power Dissipation ⁽⁵⁾	1.5W
Lead Temperature (Soldering 10sec)	260°C

Note:

- (1) -5V for <10nS.
- (2) 23V for <10nS.
- (3) These values are calculated in accordance with JESD51-3 and simulated on a JEDEC board, they are only valid for comparison between different packages, cannot be used for thermal design.
- (4) Measured on 1OZ two-layer ETA evaluation board ,TA=25°C; the top of SOT23-6 package is the position where θ_{JC} measured.
- (5) Power Dissipation is calculated by $PD=(T_{jmax}-T_a)/\theta_{JA}$.

Recommended Operating Conditions

(Note: The device is not guaranteed to function outside its operating conditions.)

Ambient Temperature Range	-40°C to 85°C
Junction Temperature Range	-40°C to 125°C

ELECTRICAL CHARACTERISTICS

($V_{IN} = 12V$, $V_{OUT} = 3.3V$, unless otherwise specified. Typical values are at $T_A = 25^\circ C$.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range		4.5		18	V
Input UVLO	Rising, Hysteresis=320mV		4.05		V
Input OVP	Rising, Hysteresis=0.9V		19		V
Input Supply Current	$V_{FB}=0.65V$, no switching		177		μA
Input Shutdown Current			7	14	μA
FB Voltage		0.593	0.603	0.612	V
FB Input Current			0	1	μA
Output Voltage Range		0.603		5.5	V
Switching Frequency			500		kHz

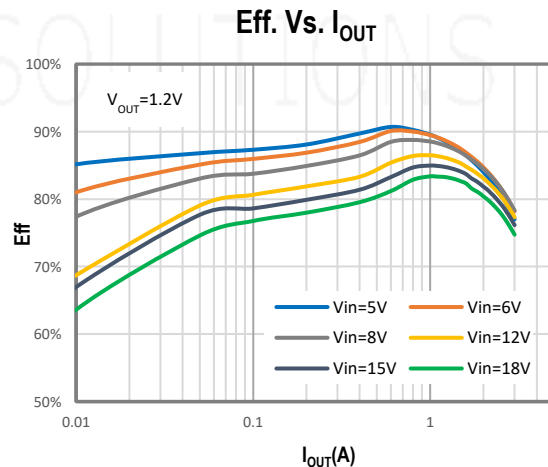
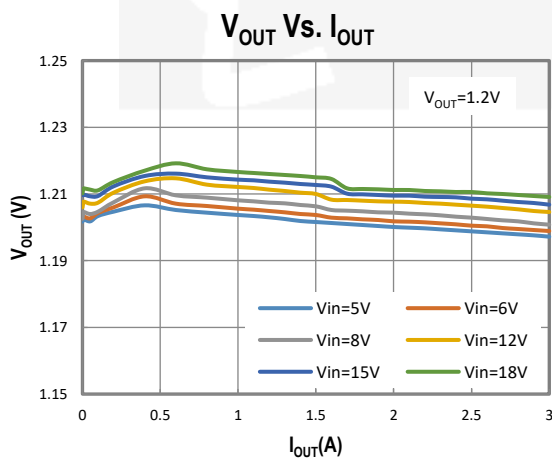
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Duty Cycle			97		%
Short Circuit Hiccup Time	On Time		2		mS
	Off Time		6		mS
Soft Start Time			1		mS
FB Hiccup Threshold			0.4		V
High Side Switch On Resistance			83		mΩ
Low Side Switch On Resistance			50		mΩ
High Side Current Limit		3.53	4.7	5.87	A
SW Leakage Current	IN=SW=12V			10	μA
EN Rising Threshold	Rising	1	1.2	1.4	V
EN Falling Threshold	Falling	0.9	1.1	1.3	V
EN Input Current	V _{EN} =2V		2	6	uA
Thermal Shutdown	Rising, Hysteresis =36°C		150		°C

PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	BST	Bootstrap pin. Connect a 10nF capacitor from this pin to SW
2	GND	Ground
3	FB	Feedback Input. Connect an external resistor divider from the output to FB and GND to set V _{OUT}
4	EN	Enable pin for the IC. Drive this pin high to enable the part, low or floating to disable.
5	IN	Supply Voltage. Bypass with a 10μF ceramic capacitor to GND
6	SW	Inductor Connection. Connect an inductor Between SW and the regulator output.

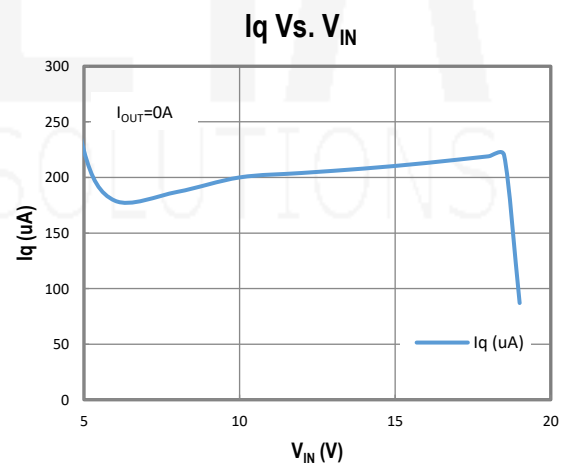
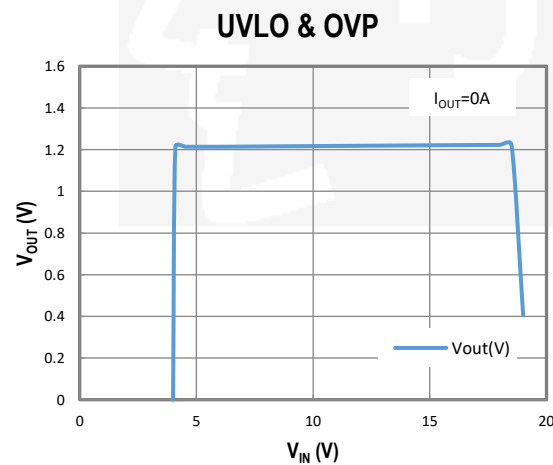
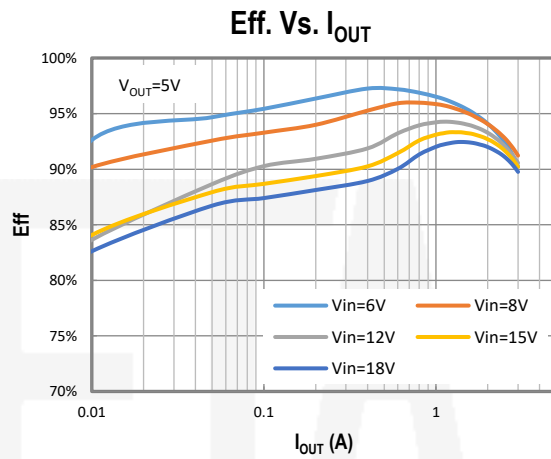
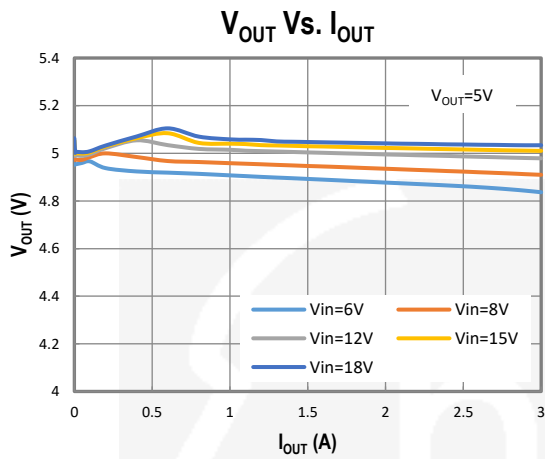
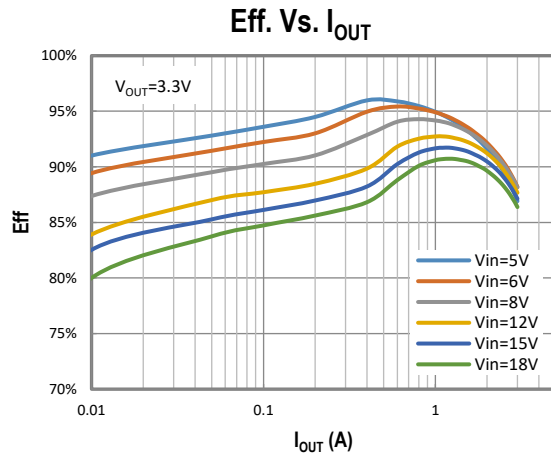
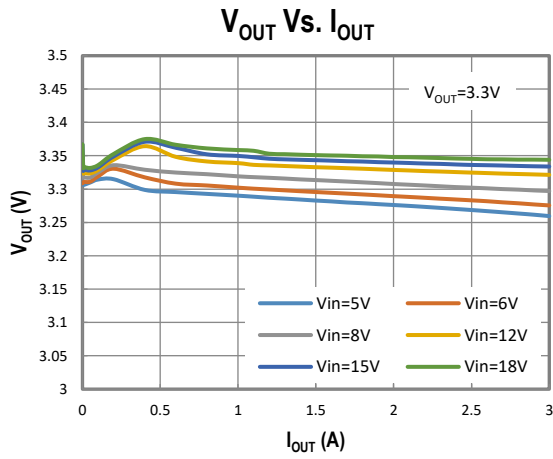
TYPICAL CHARACTERISTICS

(Typical values are at TA = 25°C unless otherwise specified.)



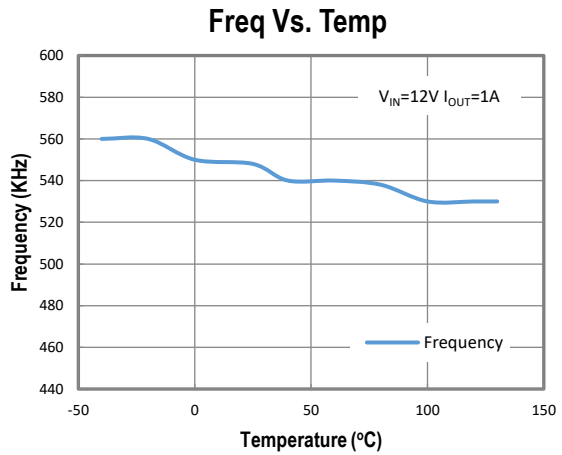
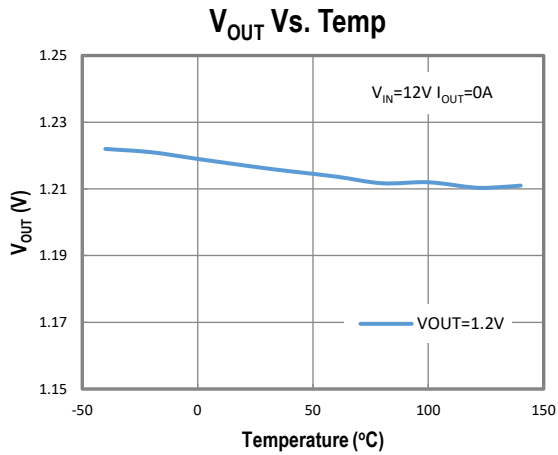
TYPICAL CHARACTERISTICS Cont'd

(Typical values are at TA = 25°C unless otherwise specified.)

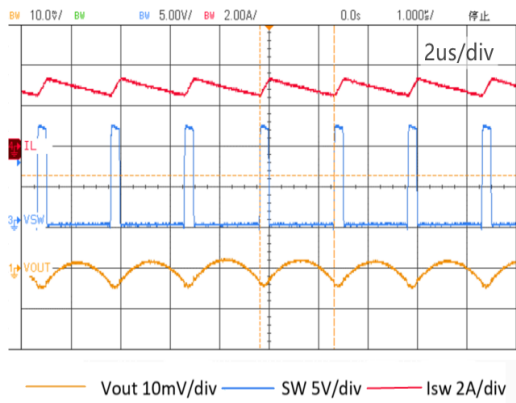


TYPICAL CHARACTERISTICS Cont'd

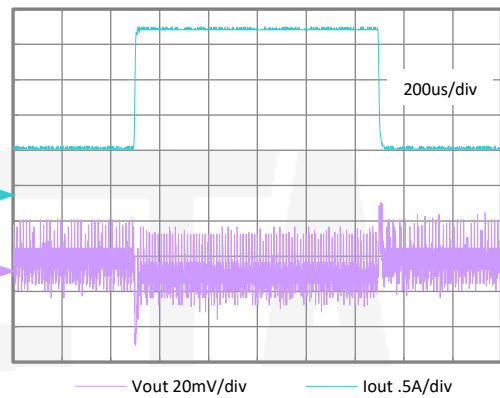
(Typical values are at TA = 25°C unless otherwise specified.)



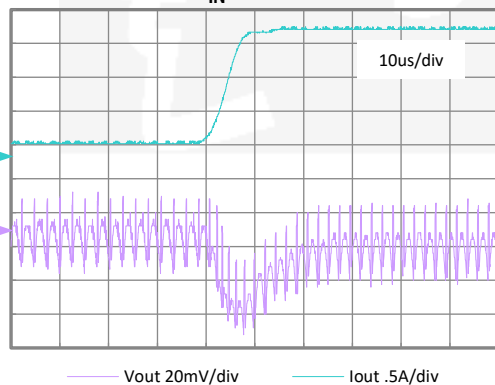
Waveform 1.2V/3A V_{IN}=12V



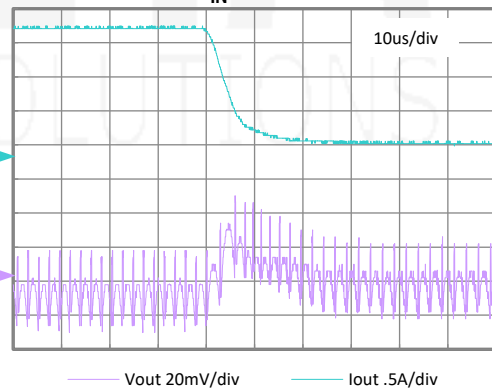
1.2V Load Step 0.3A-2A-0.3A V_{IN}=12V



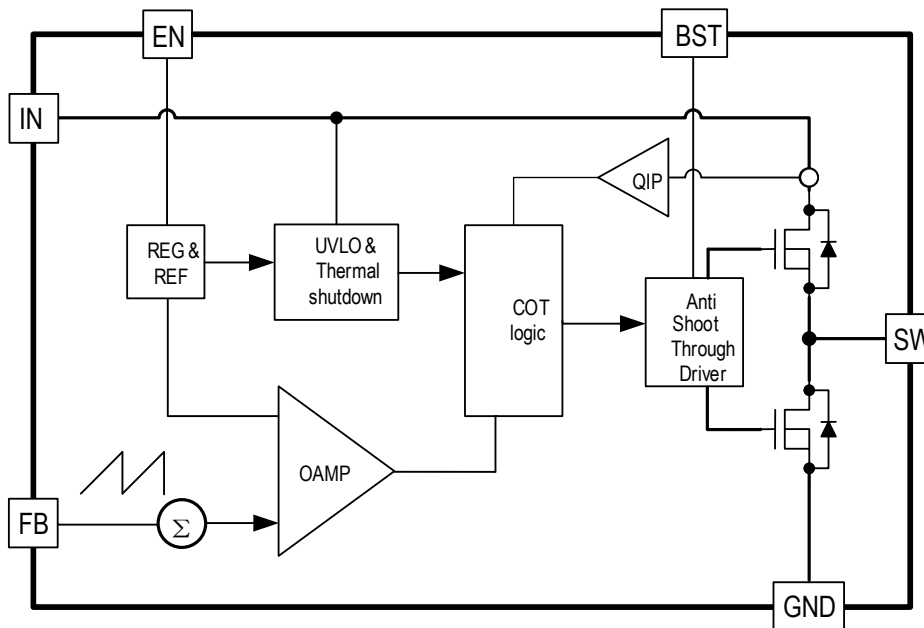
1.2V Load Step rising 0.3A-2A V_{IN}=12V



1.2V Load Step falling 2A-0.3A V_{IN}=12V



FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The ETA8113 is a synchronous buck regulator ICs that integrates the adaptive COT control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss.

ETA8113 is a wide input range, high-efficiency and high frequency DC-to-DC step-down switching regulator, capable of delivering up to 3A of output current. It adopts an Adaptive COT control scheme that enables very fast transient response and provides a very smooth transition when the output varies from light load to heavy load. It compares the sum of the FB voltage and a ripple voltage that mimics the voltage due to the output ESR and capacitance. The constant-on-time timer varies with line to achieve relative constant switching frequency across line.

Light Load Operation

Traditionally, a fixed constant frequency PWM DC-DC regulator always switches even when the output load is small. When energy is shuffling back and forth through the power MOSFET, power is lost due to the finite $R_{ds(on)}$ of the MOSFET and parasitic capacitances. At light load, this loss is prominent and efficiency is therefore very low. ETA8113 goes into a power save mode during light load, thereby extending the range of high efficiency operation.

Enable

EN is a digital control pin that turns the ETA8113 on and off. Drive EN High to turn on the regulator, drive it Low to turn it off. An internal $1M\Omega$ resistor from EN pin to GND allows EN to float to shut down the chip. Connecting the EN pin through a pull up resistor or shorted EN to IN will automatically turn on the chip whenever plug in IN.

Over Current Protection and Hiccup

ETA8113 has a cycle-by-cycle over current limit for when the inductor current peak value is over the set current limit threshold. When the output voltage drop until FB falls below UV threshold (0.4V), the ETA8113 will enter hiccup mode. It will turn off the chip immediately for 6mS. After that, it will try to re-starts as

normal for 2mS. After 2mS, if FB is still below UV threshold, then the chip enters hiccup mode again. If FB is higher than UV threshold, it will enter the normal mode.

Over-Temperature Protection

Thermal protection disables the output when the junction temperature rises to approximately 150°C, allowing the device to cool down. When the junction temperature cools to approximately 110°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

APPLICATION INFORMATION

External Output Voltage Setting

In external Output Voltage Setting Version selected, the ETA8113 regulator is programmed using an external resistor divider. The output voltage is calculated using below equation.

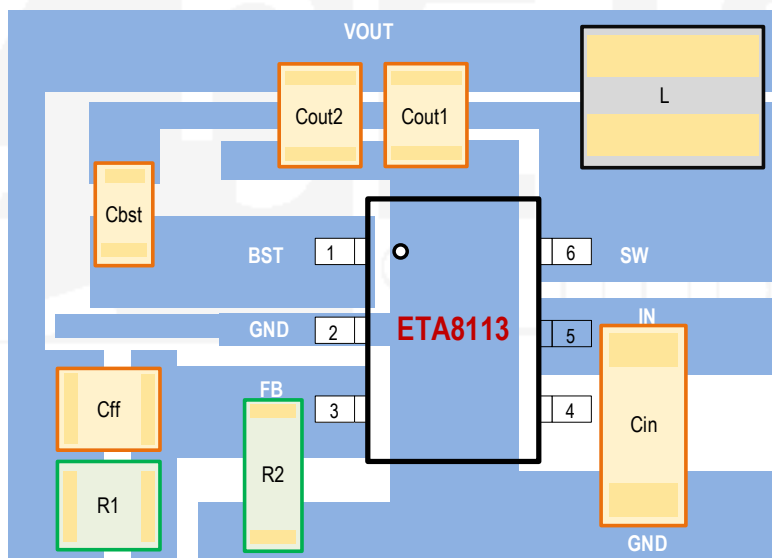
$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

Where: $V_{REF} = 0.603V$ typically (the internal reference voltage)

Resistors R2 has to be between 1KOhm to 20KOhm and thus R1 is calculated by following equation.

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2$$

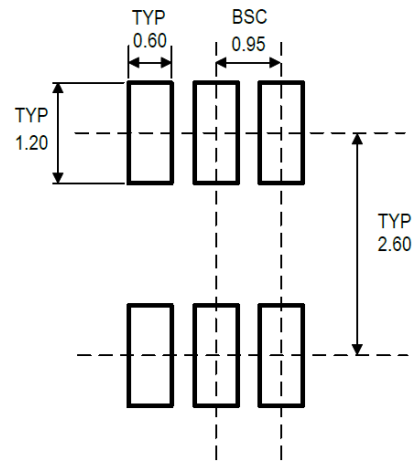
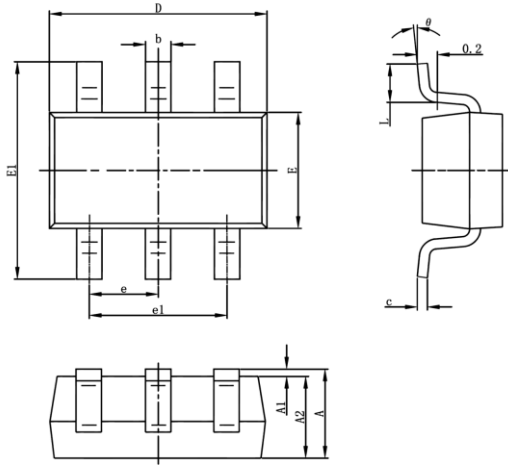
PCB LAYOUT GUIDE



Cin is always placed close to VIN and GND pins ;GND trace must be routed underneath the IC body for better Cin and FB Resistor connection; Shield FB node from SW node by GND trace

PACKAGE OUTLINE

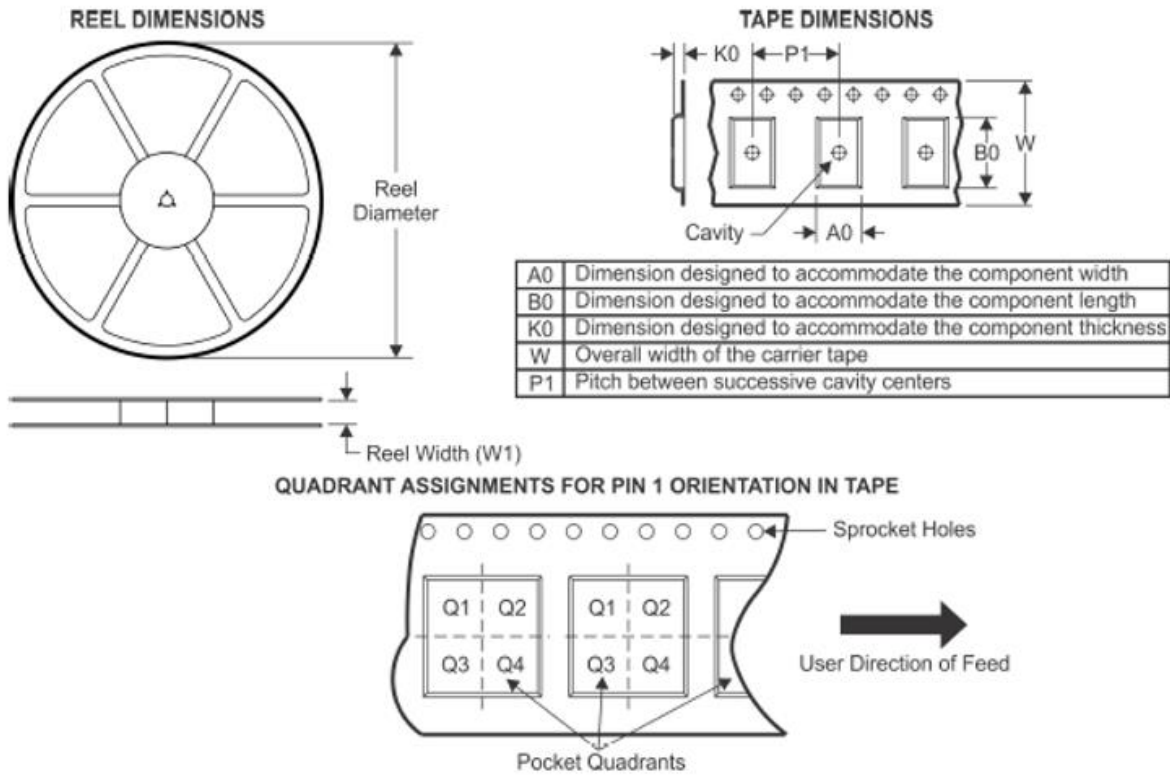
Package: SOT23-6



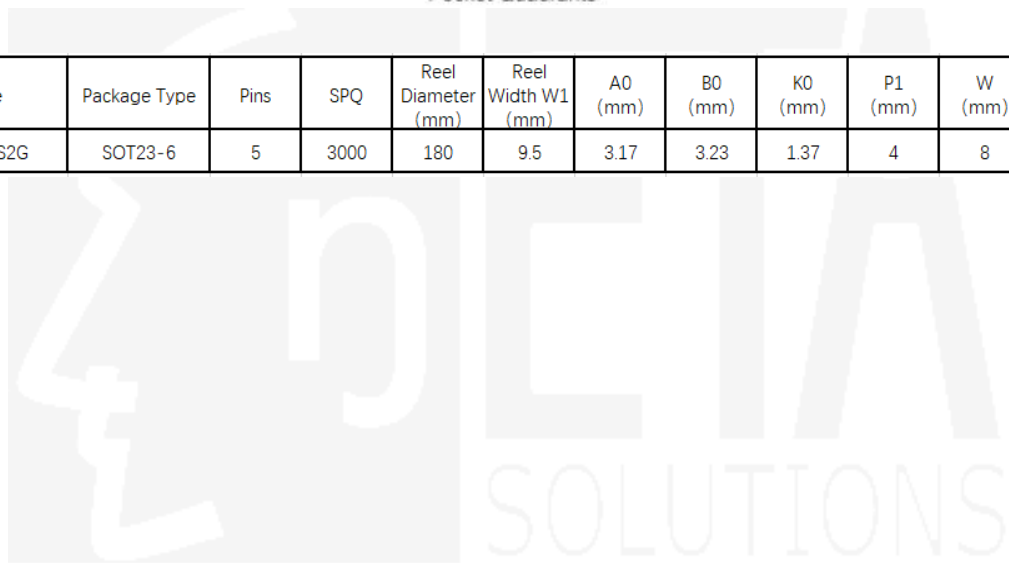
RECOMMENDED LAND PATTERN

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ETA8113S2G	SOT23-6	5	3000	180	9.5	3.17	3.23	1.37	4	8	Q3



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