



Eternal Semiconductor Inc.

EV3415

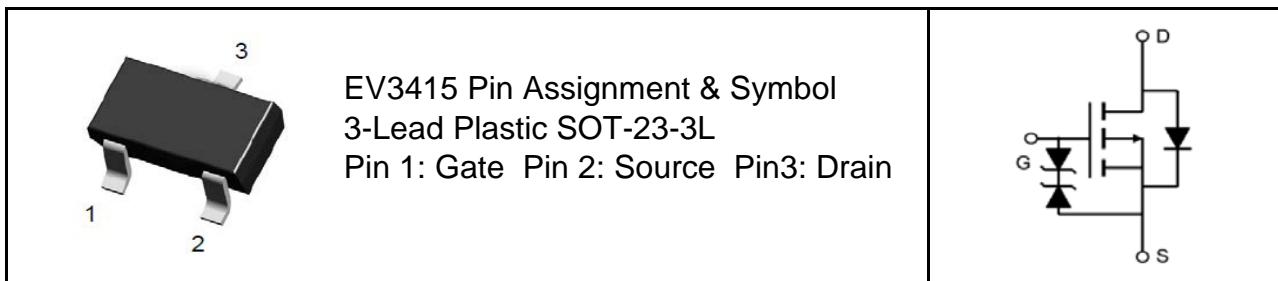
P-Channel Enhancement-Mode MOSFET (-20V, -4.0A)

PRODUCT SUMMARY

V_{DSS}	I_D	$R_{DS(on)}$ (mΩ) Typ.
-20V	-4.0A	34 @ $V_{GS} = -4.5$ V, $I_D = -4$ A
		44 @ $V_{GS} = -2.5$ V, $I_D = -4$ A
		55 @ $V_{GS} = -1.5$ V, $I_D = -2$ A

Features

- Super high dense cell trench design for low RDS(on)
- Rugged and reliable
- SOT-23-3L package
- ESD
- Lead (Pb) -free and halogen-free



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	± 8	V
I_D	Drain Current (Continuous)	-4	A
I_{DM}	Drain Current (Pulsed) ^a	-30	A
P_D	Total Power Dissipation @ $T_A = 25^\circ\text{C}$	1.4	W
I_S	Maximum Diode Forward Current	2	A
T_j, T_{stg}	Operating Junction and Storage Temperature Range	-55 to +150	°C
R_{QJA}	Thermal Resistance Junction to Ambient (PCB mounted) ^b	100	°C/W

a: Repetitive Rating: Pulse width limited by the maximum junction temperature.

b: 1-in² 2oz Cu PCB board



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Electrical Characteristics ($T_A=25^\circ\text{C}$, unless otherwise noted)

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
• Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}}=-20\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{\text{GS}}=\pm 8\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
• On Characteristics						
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=-250\mu\text{A}$	-0.45	-0.55	-1	V
$R_{\text{DS(on)}}$	Drain-Source On-State Resistance	$V_{\text{GS}}=-4.5\text{V}, I_{\text{D}}=-4\text{A}$	-	34	43	$\text{m}\Omega$
		$V_{\text{GS}}=-2.5\text{V}, I_{\text{D}}=-4\text{A}$	-	44	54	
		$V_{\text{GS}}=-1.8\text{V}, I_{\text{D}}=-2\text{A}$	-	50	60	
• Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{\text{DS}}=-10\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	-	950	-	PF
C_{oss}	Output Capacitance		-	165	-	
C_{rss}	Reverse Transfer Capacitance		-	120	-	
• Switching Characteristics						
Q_g	Total Gate Charge	$V_{\text{DS}}=-10\text{V}, I_{\text{D}}=-1\text{A}, V_{\text{GS}}=-4.5\text{V}$	-	12	-	nC
Q_{gs}	Gate-Source Charge		-	10	-	
Q_{gd}	Gate-Drain Charge		-	19	-	
$t_{\text{d(on)}}$	Turn-on Delay Time	$V_{\text{DD}}=-10\text{V}, R_{\text{L}}=15\Omega, I_{\text{D}}=1\text{A}, \text{VGEN}=-4.5\text{V}, RG=10\Omega$	-	12	-	nS
t_r	Turn-on Rise Time		-	10	-	
$t_{\text{d(off)}}$	Turn-off Delay Time		-	19	-	
t_f	Turn-off Fall Time		-	25	-	
• Drain-Source Diode Characteristics						
V_{SD}	Drain-Source Diode Forward	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=-1\text{A}$	-	-	-1	V

Note: Pulse Test: Pulse Width $\leq 300\text{us}$, Duty Cycle $\leq 2\%$



Switching Test Circuit and Swithching Waveforms



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Typical Characteristics Curves ($T_A=25^\circ\text{C}$, unless otherwise note)

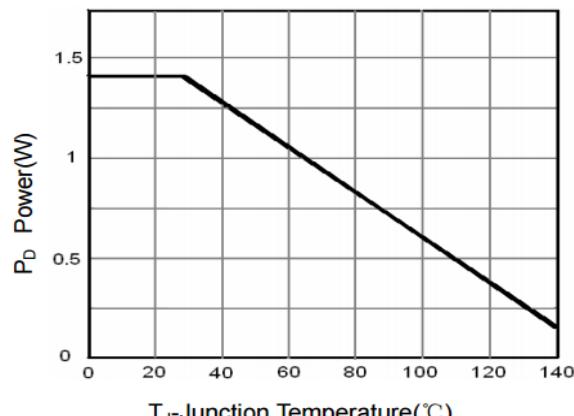


Figure 1 Power Dissipation

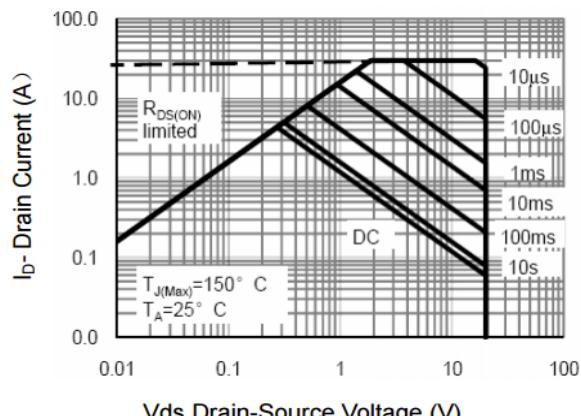


Figure 2 Safe Operation Area

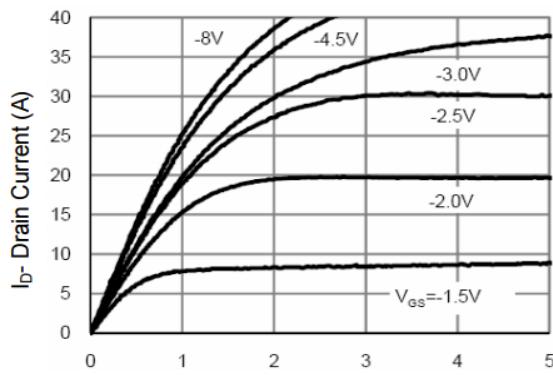


Figure 3 Output Characteristics

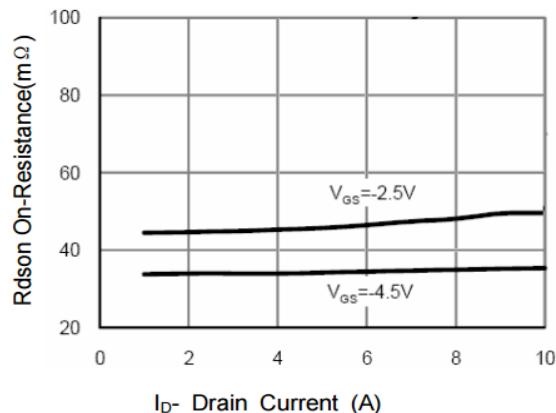


Figure 4 Drain-Source On-Resistance

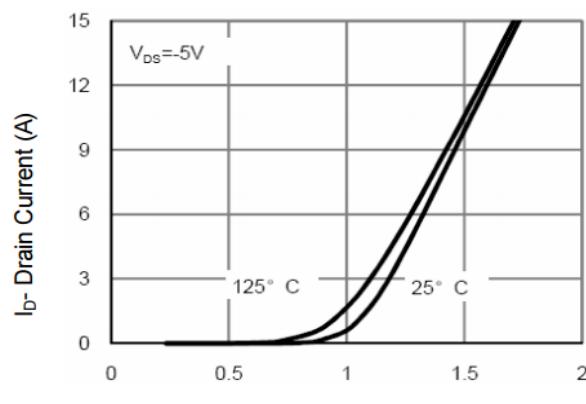


Figure 5 Transfer Characteristics

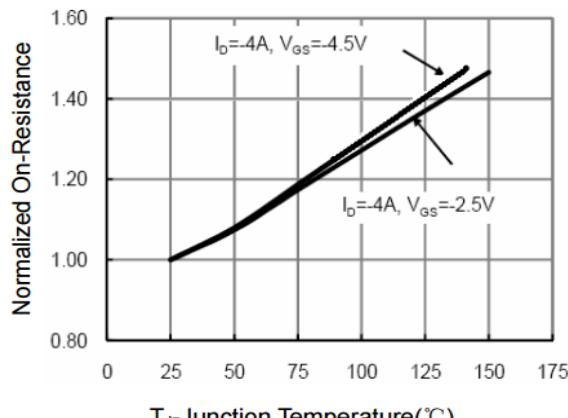


Figure 6 Drain-Source On-Resistance

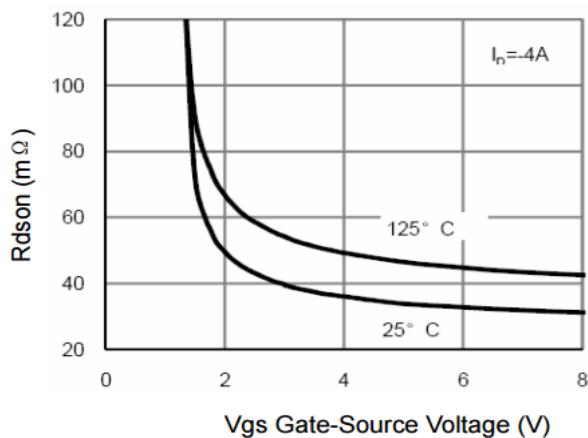


Figure 7 Rdson vs Vgs

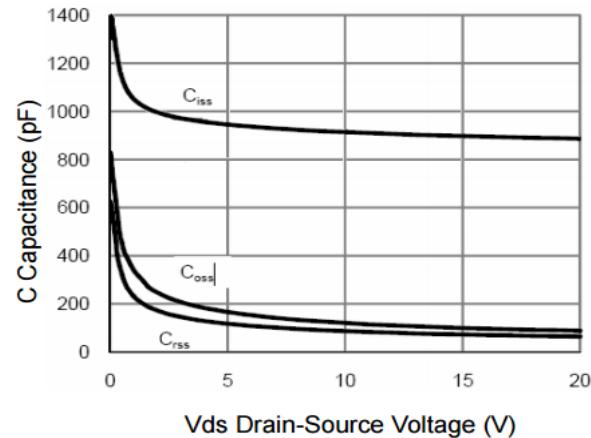


Figure 8 Capacitance vs Vds

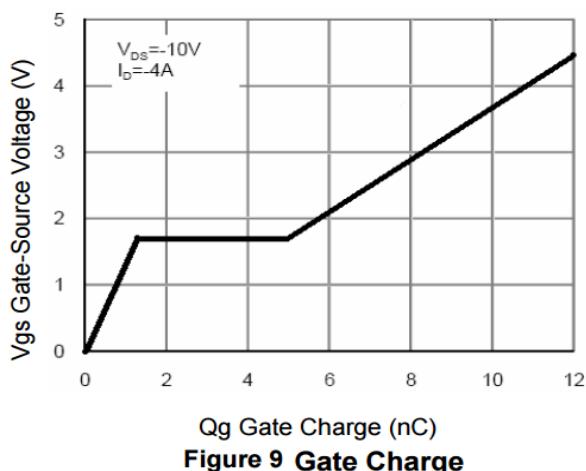


Figure 9 Gate Charge

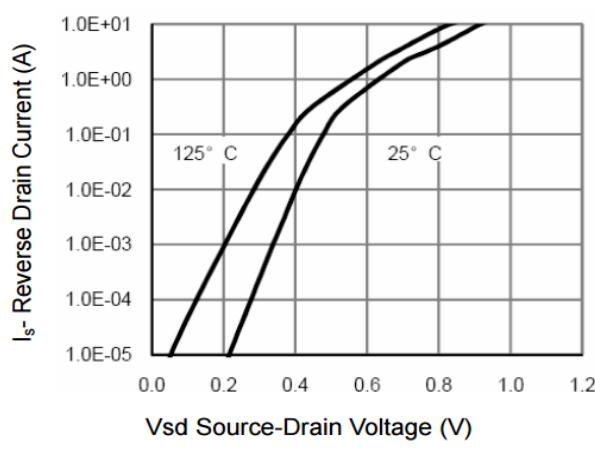


Figure 10 Source- Drain Diode Forward

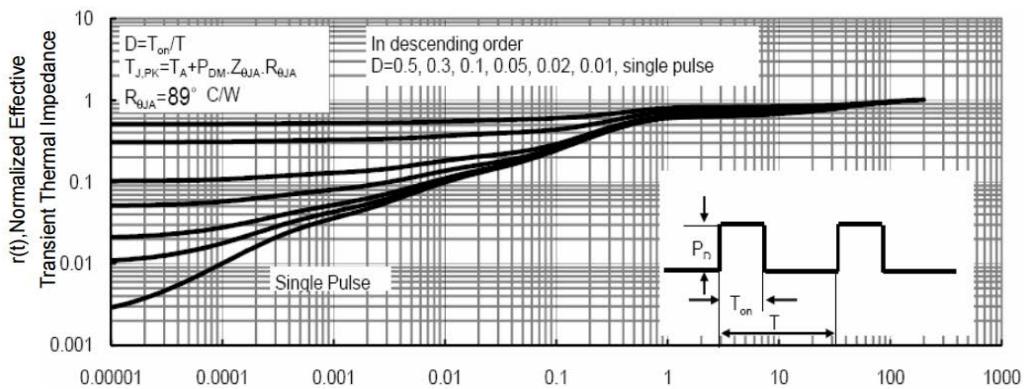


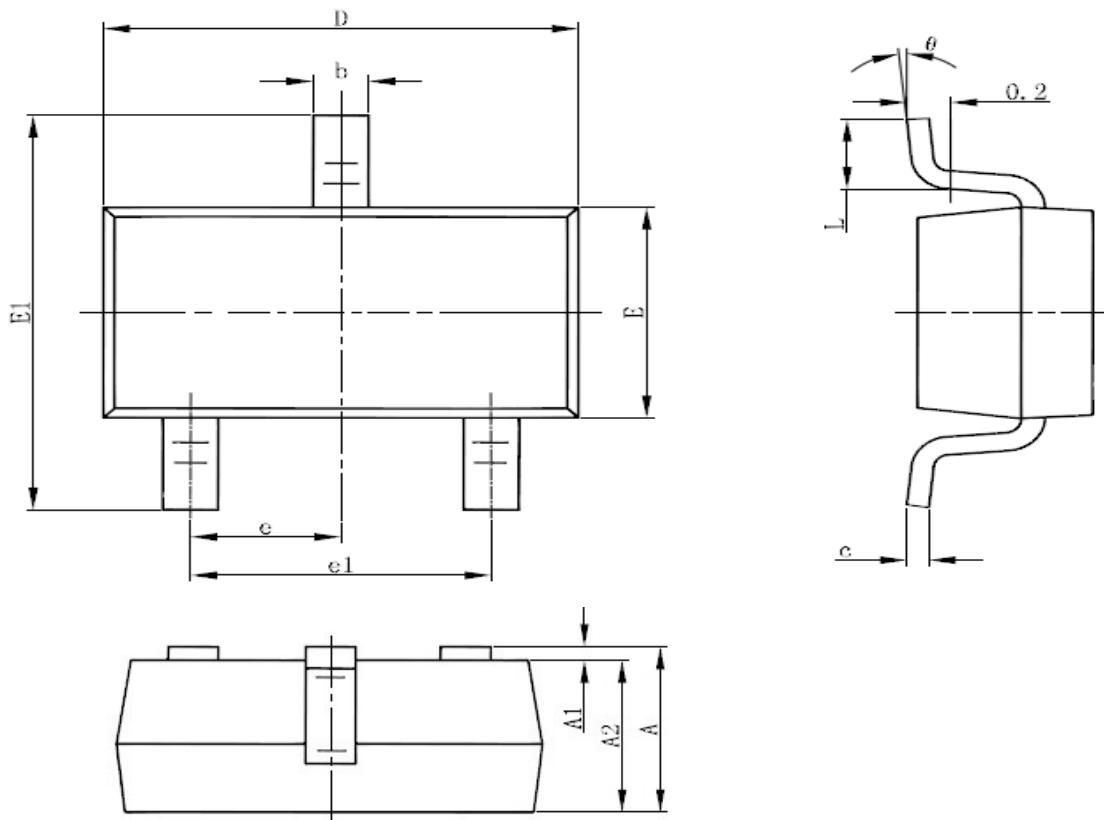
Figure 11 Normalized Maximum Transient Thermal Impedance



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SOT23-3L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.850	1.250	0.033	0.049
A1	0.000	0.100	0.000	0.004
A2	0.7	1.150	0.028	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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