

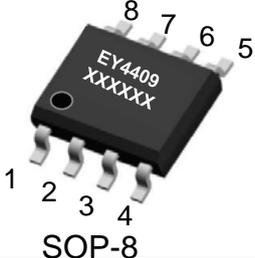
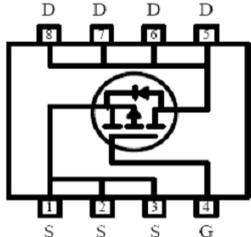
P-Channel Enhancement-Mode MOSFET (-30V, -14A)

PRODUCT SUMMARY

V_{DSS}	I_D	$R_{DS(on)}$ (m Ω)TYP
-30V	-14A	10@ $V_{GS} = -10V, I_D = -14A$
		18@ $V_{GS} = -4.5V, I_D = -8A$

Features

- Advanced Trench Process Technology
- High Density Cell Design for Ultra Low On-Resistance
- Fully Characterized Avalanche Voltage and Current
- -5V Logic Level Control
- Lead (Pb) -free and halogen-free

 <p>8 7 6 5 EY4409 XXXXXX 1 2 3 4 SOP-8</p>	 <p>D D D D S S S G</p>	<p>Pin1/2/3: Source Pin4: Gate Pin5/6/7/8: Drain</p>	<p>TOP Marking</p>
			<p>EY4409 part number XXXXXX ID CODE</p>

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current (Continuous)	-14	A
I_{DM}	Drain Current (Pulsed) ^a	-56	A
P_D	Total Power Dissipation @ $T_A = 25^\circ\text{C}$	3.0	W
E_{AS} ^b	Avalanche Energy, Single pulse ($L = 0.3\text{mH}$)	81	mJ
I_S	Maximum Diode Forward Current	-3	A
T_j, T_{stg}	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
R_{QJA}	Maximum Junction-to-Ambient ($t \leq 10\text{s}$) ^c	24	$^\circ\text{C/W}$
	Maximum Junction-to-Ambient (Steady State) ^c	40	$^\circ\text{C/W}$

a: Repetitive Rating: Pulse width limited by the maximum junction temperature.

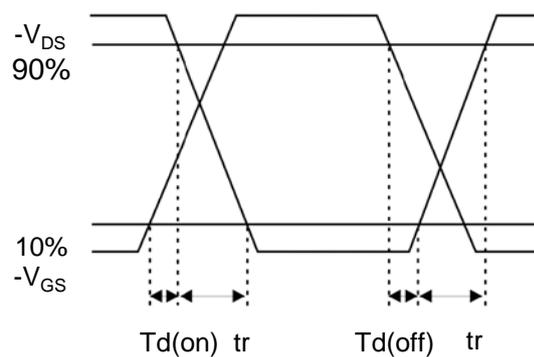
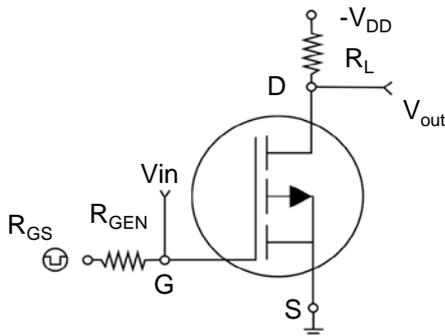
b: Surface Mounted on 1in² pad area, $t < 10\text{sec}$.

c: 1-in² 2oz Cu PCB board

Electrical Characteristics ($T_A=25^\circ\text{C}$, unless otherwise noted)

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
• Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
• On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.9	-2.5	V
$R_{DS(on)}$	Drain-Source On-State Resistance	$V_{GS}=-10V, I_D=-14A$	-	10	13	m Ω
		$V_{GS}=-4.5V, I_D=-8A$	-	18	21	
• Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	-	3320	-	PF
C_{oss}	Output Capacitance		-	395	-	
C_{rss}	Reverse Transfer Capacitance		-	245	-	
• Switching Characteristics						
Q_g	Total Gate Charge	$V_{DS}=-15V, I_D=-5.3A, V_{GS}=-10V$	-	39	-	nC
Q_{gs}	Gate-Source Charge		-	7	-	
Q_{gd}	Gate-Drain Charge		-	11	-	
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=-15V, R_L=5\Omega, I_D=-3A, V_{GEN}=-10V, R_G=6\Omega$	-	15	-	nS
t_r	Turn-on Rise Time		-	33	-	
$t_{d(off)}$	Turn-off Delay Time		-	67	-	
t_f	Turn-off Fall Time		-	21	-	
• Drain-Source Diode Characteristics						
V_{SD}	Drain-Source Diode Forward	$V_{GS}=0V, I_S=-2.0A$	-	-	-1.3	V

Note: Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$



Switching Test Circuit and Switching Waveforms

Typical Characteristics Curves (Ta=25°C, unless otherwise note)

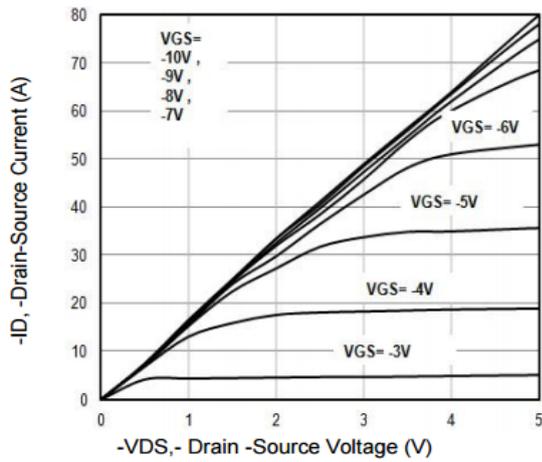


Fig1. Typical Output Characteristics

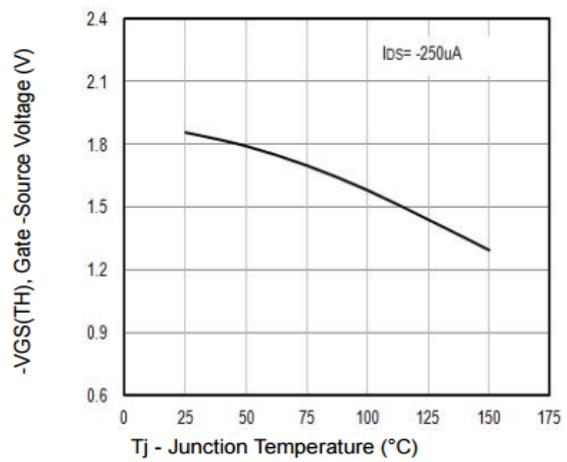


Fig2. -VGS(TH) Gate -Source Voltage Vs. Tj

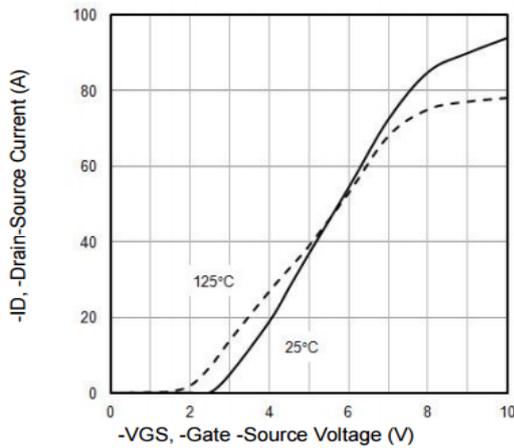


Fig3. Typical Transfer Characteristics

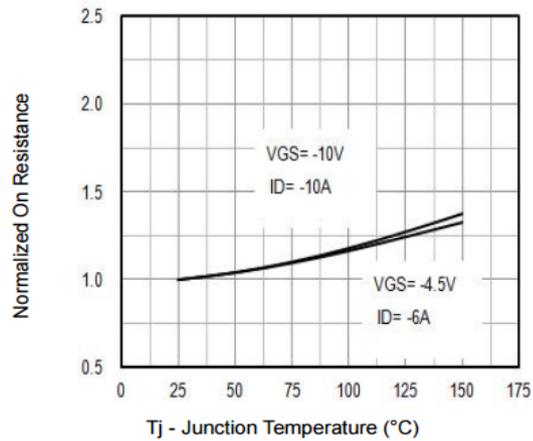


Fig4. Normalized On-Resistance Vs. Tj

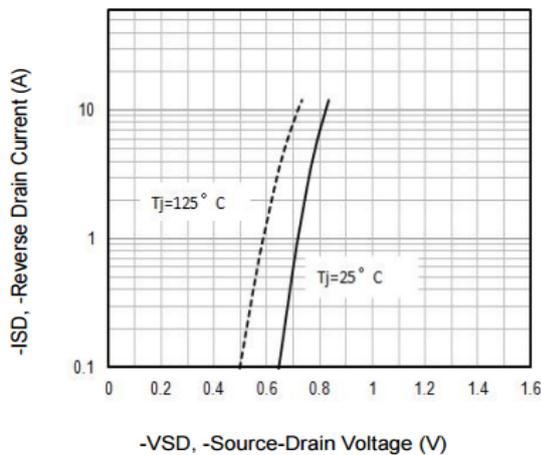


Fig5. Typical Source-Drain Diode Forward Voltage

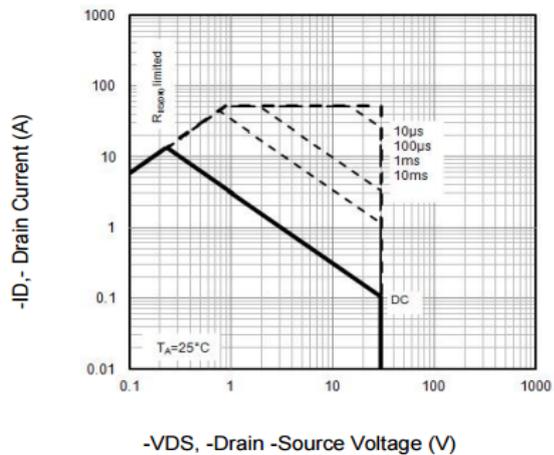


Fig6. Maximum Safe Operating Area

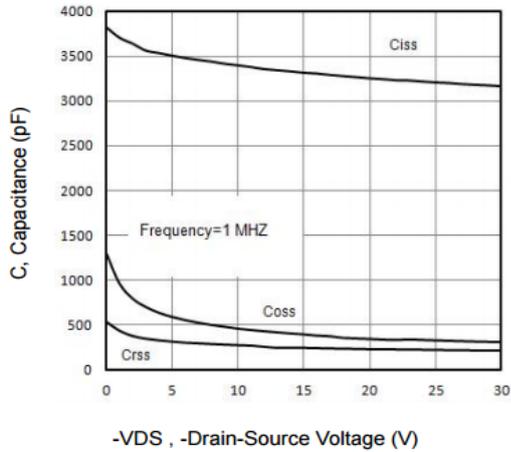


Fig7. Typical Capacitance Vs. Drain-Source Voltage

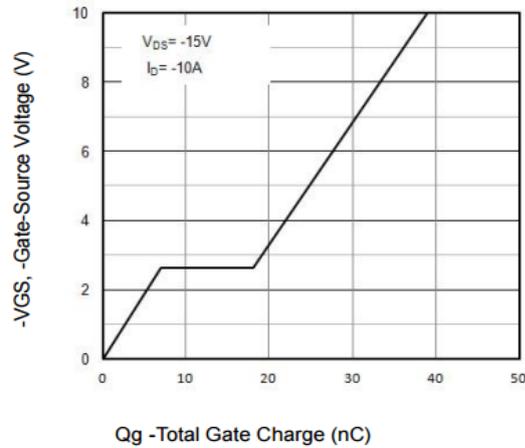


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

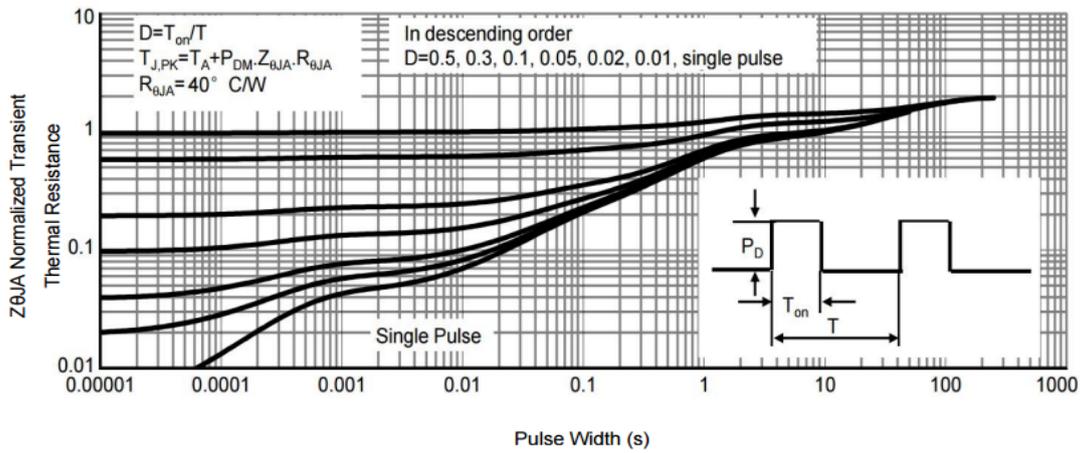
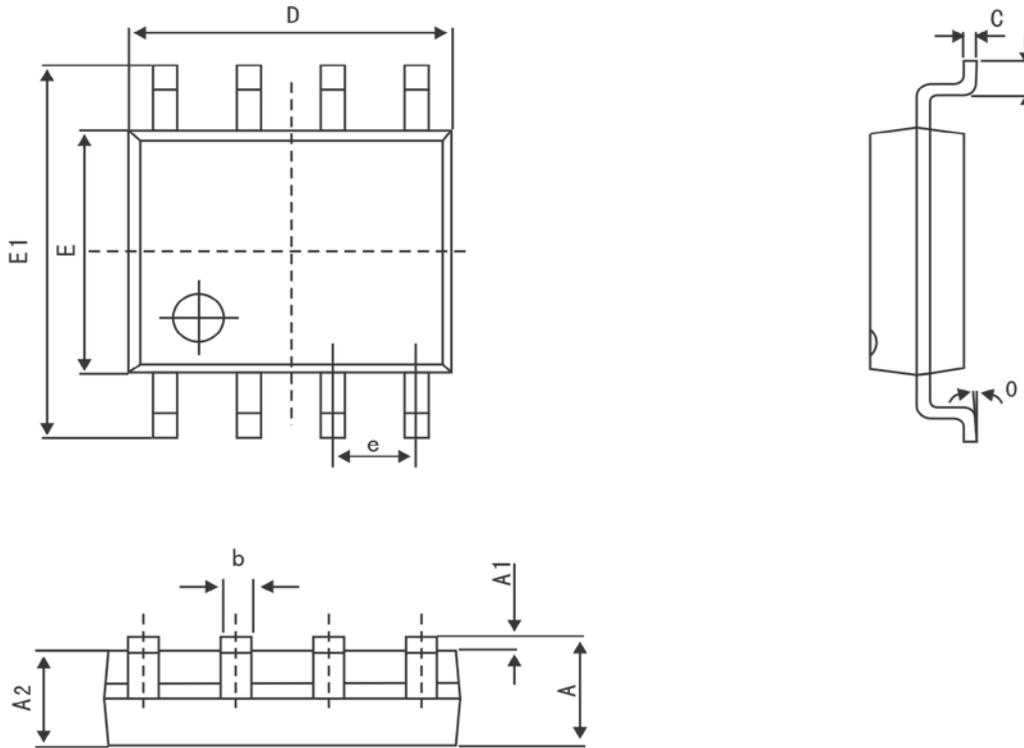


Fig9. Normalized Maximum Transient Thermal Impedance

SOP-8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters (MM)		Dimensions In Inches (MIL)	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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